CMOS Imager with Embedded Analog Early Image processor

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We are presenting an integrated elementary-feature tracking system. Real-time tracking is the core of a variety of computationally-intensive applications such as autonomous navigation (machine vision, robots, docking...), object avoidance or intercept, recognition (tracking of eyes, nose...).

While high-speed imagers are being developed, providing low-noise imagery at high speed, and processing the image at a high update rate required in autonomous navigation or object-avoidance scenarios remain a challenge. One approach to enable such a system is to carry out early image processing at the focal-plane to reduce the data-set, thereby saving precious transmission and computation bandwidth and power.

A single-chip system combining an Active Pixel Sensor (APS) imager an with an early-image processor has been developed. The early-image processor consists of correlator circuits to identify in real-time possible areas of interest. The correlator finds a match between a small (7x7 pixel) target template (representing a filter corresponding to image texture identification, e.g. difference of gaussian) and the image. Correlation values higher than a threshold can be used to identify regions of interest, and can be downloaded to the off-chip processor for closed-loop tracking and control, or can be used to refresh the template and use it for on-chip high-speed tracking (See Figure 1 and Figure 2). Depending upon application, it is possible to configure the system for only early-image processing or complete close-loop tracking.

A proof-of-concept imager with embedded early processor equipped with a fixed correlation core was fabricated and tested. It consists of a 64×64 pixels current-mode imager, as shown in fig. 3, to drive the current-mode correlators. In this configuration, a 100μA current flow down the pixel column is provided by a current mirror above the imager. During the light exposure, the photodiode capacitance accumulates charges that bias the gate of Tc. When the pixel is selected by opening Tsel, part of the current flow is re-routed to Ground through Tc, proportional to the gate voltage of Tc, hence of the light intensity. This design being non-linear is very sensitive to slight variations, both of fabrication parameters (transistor threshold voltages, matching...) and operating stability (light intensity...).

The heart of the early-processor is the correlation to perform at every frame between the imager and the template. The operation to perform is: $C=\sum_{i=1}^{7}\sum_{j=1}^{7}\left(I_{i,j}\cdot T_{i,j}\right)$, where $I_{i,j}$ is the image pixel and $T_{i,j}$ is the corresponding template pixel. Since the template is 7×7 large, the correlation is performed on a window that size.

We implemented this multiplier/accumulator as a set (7×7=49) multiplying Digital to Analog Converter (MDAC) units. The current from the imager acts as a reference current and the bits from the digital template as the value to convert (see figure 4). The amplification occurs in binary-scaled current mirrors selected by the bits of the template. The eight bits are split in two blocks of fours, sent to current mirrors scaled 1-1, 1-2, 1-4 and 1-8 and dumped into the accumulating capacitor for a different period of time. The output current from the lower bits charge the capacitor for 50ns and the upper bits for 800ns (16× longer). Each row result is stored in a capacitor so it can be used to be added up with the next row and reconstruct the correlation over the 7×7 pixels window.

A voltage-mode circuit was also studied. It allowed the use of better-quality voltage-mode pixels but called for binary-scaled capacitors in lieu of transistors as well as one operational amplifier for each correlator unit. The result was a much larger design that wouldn't be appropriate for scaling up to using larger format imagers.

Figure 5 shows images taken with the 64×64 imager of the chip presented here. The large fixed pattern noise (~5%) was corrected through off-chip dark-frame and flat field compensation. Better quality image can be obtained on future version by either implementing those on-chip or using a voltage-mode pixel design.

The more important feature, the correlator, shows very good performances at speeds exceeding 100fps. Figure 6 shows an example of correlation. The measured response is very close to the expected triangle for the correlation of two squares.

This design is intended to be scalable in order to place a number of units under a large imager (25 under a 1k×1k imager). This next step would allow tracking inside a sub-window of the imager.

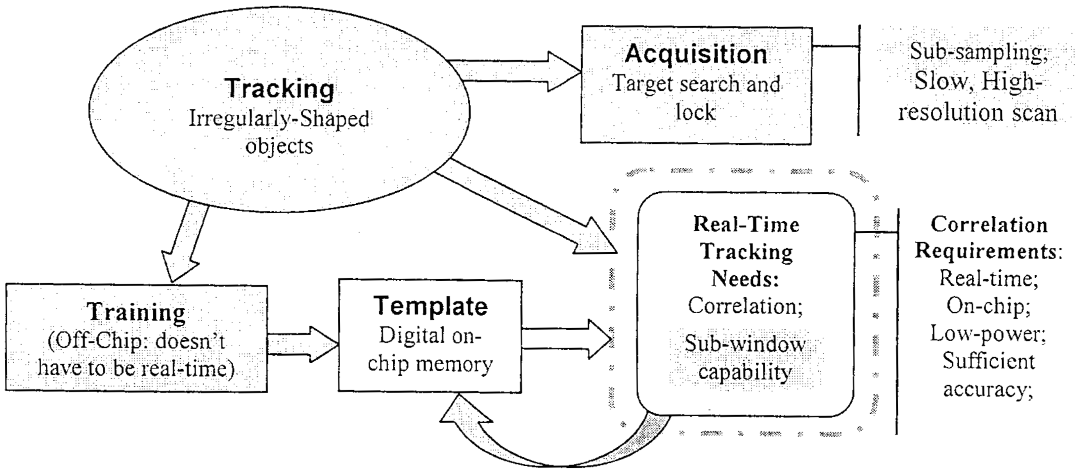

Figure 1: **System architecture**
The clear areas show the features implemented in the test chip.

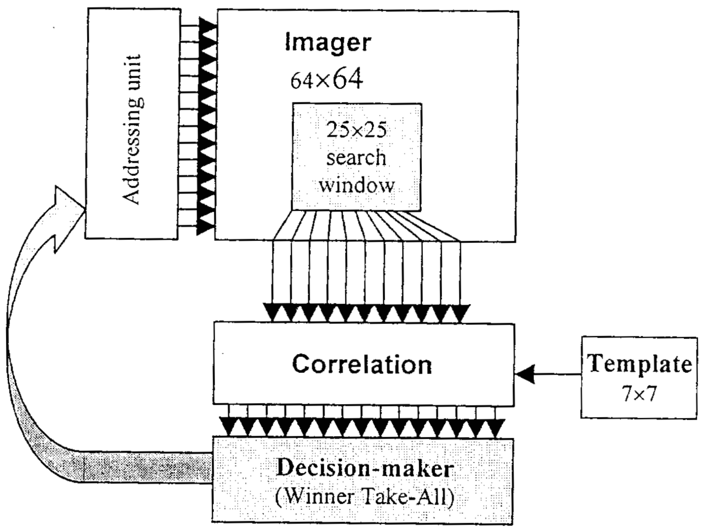

Figure 2: System block diagram

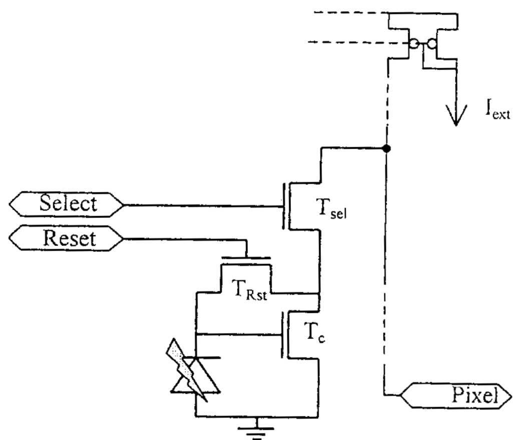

Figure 3: Pixel design

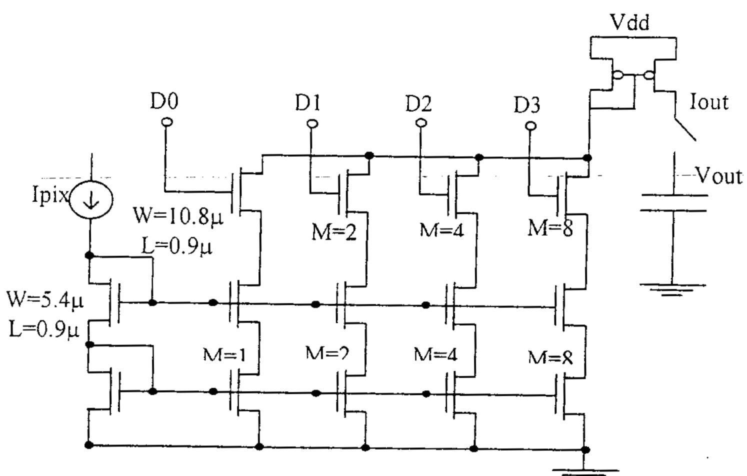

Figure 4: **Correlator Block**
First four bits of a single pixel correlation unit

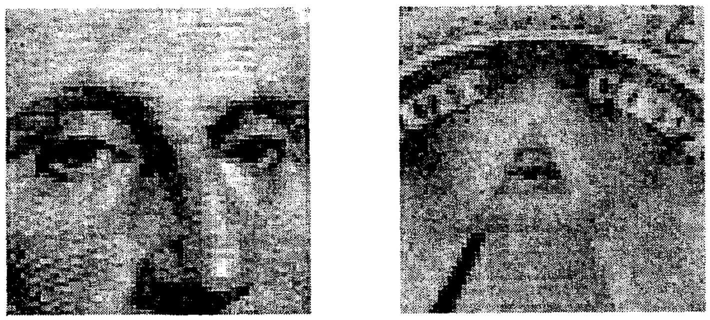

Figure 5: Sample images
From the 64×64 pixels current-mode imager

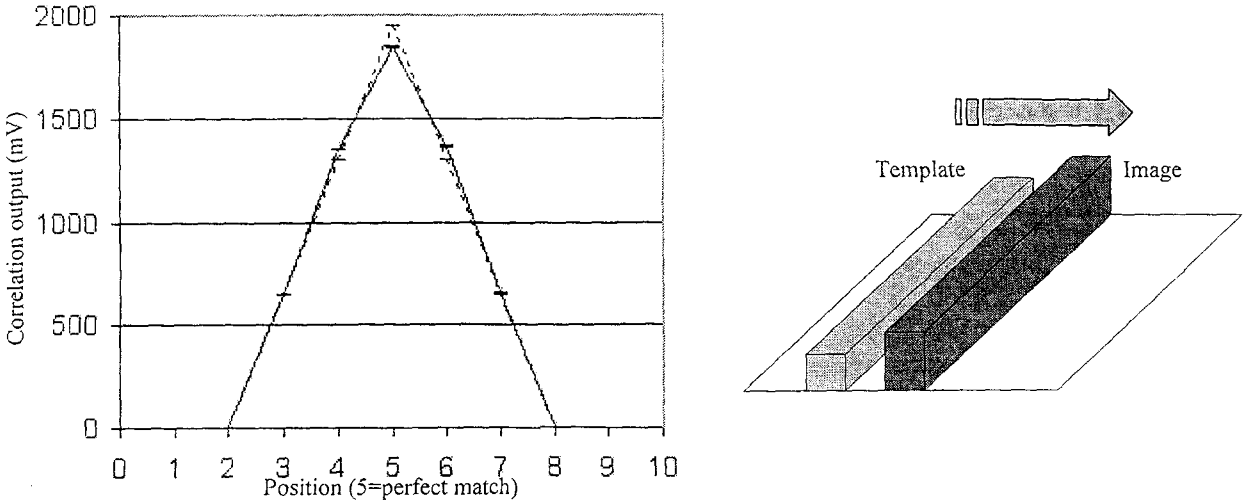

Figure 6: Correlation of two squares
Expected response (dashed line) and measured (solid line)

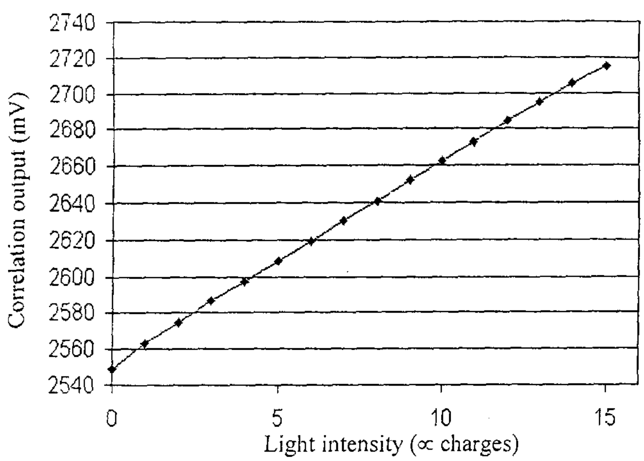

Figure 7: Correlation linearity
Flat template and image of varying intensity.

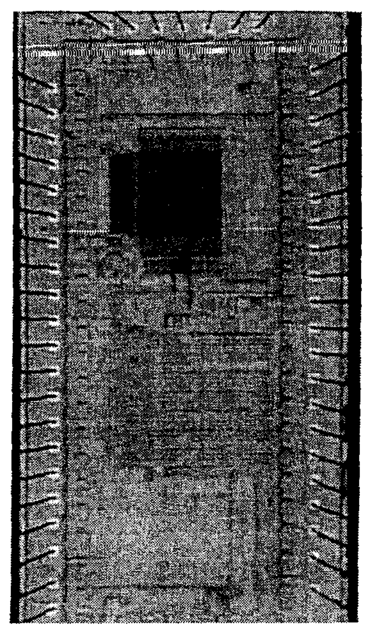

Figure 8: Photograph of the die