Total Dose, Single Event Effect and Radiation Induced Single Cell Failures in Advanced Flash Memories

Duc Nguyen and Leif Scheick
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California 91109

Abstract
We compare radiation effects on the highest density multi-level cell NOR and single-level cell NAND flash memories to the previous generations. Total ionization dose (TID) test results show unexpected failure modes.

INTRODUCTION

Digital audio or Motion Picture Expert Group Layer 3 (MP3) recorders gradually have replaced the old mechanical cassette recorders with the help of advanced non-volatile memory technology. One of the many members of the non-volatile class of memory devices is the flash memory family. Basically flash memories can retain stored data for many years in the absence of applied power. Two basic structures have been used commercially to produce flash memories. The NOR structure provides direct access to individual cells at the expense of cell areas because of the need for contacts at each drain and source connections. The NAND structure is more compact since it does not provide contacts to individual source and drain regions. Memory cells in the NAND structure require reading and writing through the other cells in the stack, an architecture that results in inherently slower cell access. To build the flash memory cell, an isolated polysilicon floating gate capable of storing electrons was inserted between the gate, source, and drain of a single transistor. Data can be interpreted as "0" when charges (electrons) are placed in the floating gate. When electrons are removed from the floating gate, data become "1". The configuration is known as single level or one-bit-per-cell storage since the read-out data can be identified either as "1" or "0". In terms of cell threshold voltage, a sense-amp circuitry recognizes "1" optimally at the level of 2.7 volts and "0" at 5.7 volts as shown in figure 1a. In order to obtain higher density, flash memory structures have been scaled down in size. But the scaling process reached its limitation at cell size of 0.13μm[1]. Another limitation is the operating voltage range, channel hot electron injection devices (NOR structure) require 10 to 12V while the Fowler Nordheim tunneling devices (NAND structure) need 18 to 20V for program and erase. Instead of scaling, an alternate method of storing more than one bit per cell (or multi-level charge storage) provides a new solution. Figure 1 shows threshold voltage distributions for single and multi-level storage methods [2]. To recognize the four states "11", "10", "01", and "00" within the 6 volt-range, the control and verify circuitry to inject charge must have the finer resolution than the sensing circuitry of single level storage.

TEST DEVICES

The NAND-based Toshiba 1Gigabit flash parts organized as 528bytes x 32 pages x 8192 blocks. Programmed and read data are transferred between the 528-byte static register and the memory cell array in 528-byte increments. During read mode, the page can be cut into three sections by the use of an internal pointer. A page can also be divided into up to 3 segments during the partial

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page program. The erase operation is implemented in block increments. The serial read cycle is 50ns and the access time of cell array to register is 25 microseconds. Toshiba flash was based on the 0.16 micron process.

The Intel 3 Volt-Synchronous StrataFlash 256Mbit devices provide the highest density NOR-based flash memory available commercially with two-bit per cell capability. It has 3 different read modes: asynchronous (120ns), page (25ns), and burst or synchronous (13ns). The Intel device supports three different programming choices: word programming, write buffer programming, and Buffered Enhanced Factory Programming or Buffered-EEP. The Intel part was built on the 0.18 micron process technology.

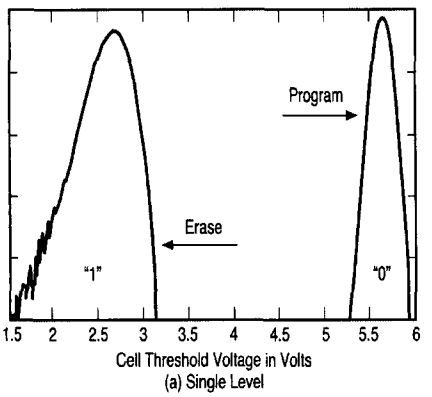

Figure 1a: Graph illustrating cell threshold voltage range in volts for a single level NAND flash memory device. To erase the cell or remove charges from the floating gate, the sense amp will interpret cell data as "1". To program the cell or inject charges to the floating gate, stored data will be read out as "0" by the sensing circuitry. The safeguard-band range for distinguishing between the logic "1" and the logic "0" is more than 2 volts.

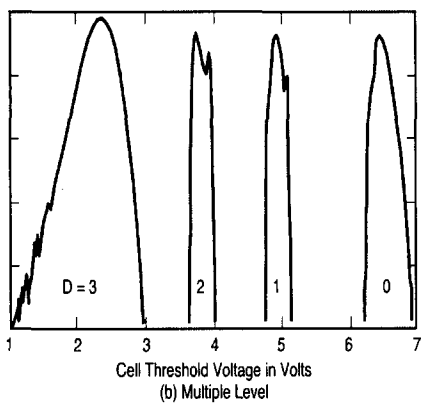

Figure 1b: Four different humps present threshold levels of four states in a 2-bit per cell NOR flash memory device. Data "11" (or D=3) can be understood as both bits are erased. When both bits are programmed, the threshold voltage should be in the 6.2 to 7 volt range. The same sensing scheme designed for read operation also is implemented in program circuitry to deliver the right levels for the two bits in the cell.

SEE

The overall operation of flash memories requires many clock cycles and commands just like the operation of most microprocessors because of the complex architectures, such as internal state machine, write buffer, and registers. Single event upsets occurred in the state machine and registers are very difficult to categorize and interpret because of the many different internal operating conditions. These upsets will mostly interrupt the intended operation and locked it into an unexpected event. The events can be classified as single event functional interrupt (SEFI) [3][4]. Complex functional errors when mixed with memory errors during operations would prevent correct measurements of the cross-section. The selected DUTs were programmed with all zeros (the charge states in all memory cells) and were tested in vacuum during read operations, using ions with LET values from 3.3 to 30 MeV-cm^2/mg. Some tests were performed at 30°, 45°, and 60° angles to increase the effective LET. Figures 2 and 3 compare the cross-sections of a 128Mb with cross-sections of 1 Gb single-level NAND flash memory type. The cross-section difference of the 128Mb and 1Gb is in the order of 10 in magnitude. Figure 4 displays the cross-section of the write errors for the 1 Gb flash memory.

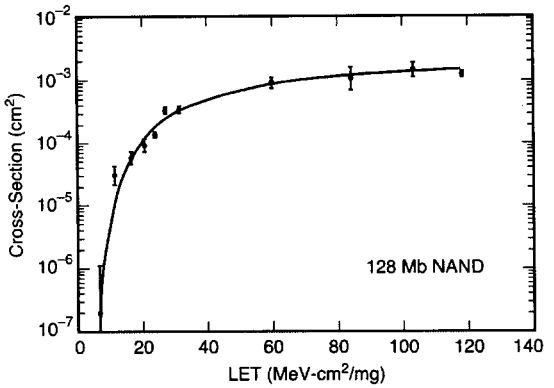

Figure 2: Single event upset cross-section for the 528-byte read buffer of the 128 Mb NAND flash memory

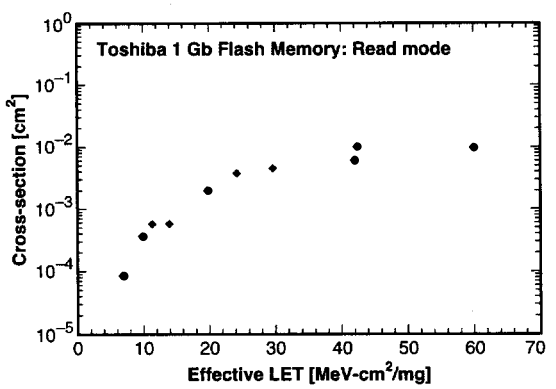

Figure 3: Cross-section of the 1Giga-bit NAND flash memory during read mode

Similar tests will be performed on the multi-level Intel 256-Mb flash memory devices.

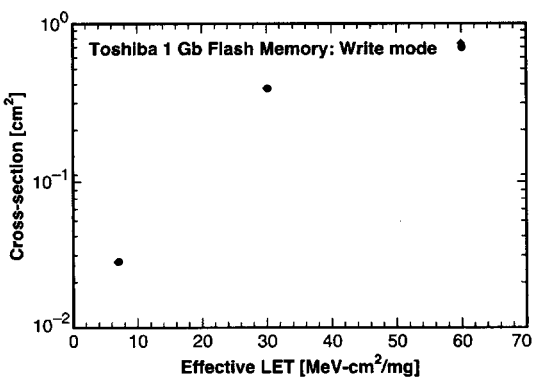

Figure 4: Cross-section of the 1 Giga-bit NAND flash memory during write mode

TID

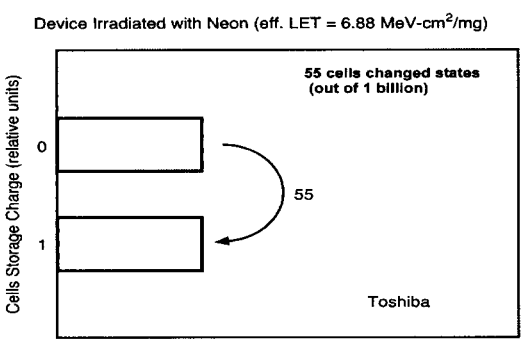

Figure 5: Single event read errors for the Toshiba 1Gb flash memory. The 55 cells changed states from "0" to "1" few days later after tested for upsets during the write operation.

Total dose tests were done using the JPL cobalt-60 facility at the dose rate of 25 rad(Si) per second with a series of 2 and 4 krad(Si) steps at 25 degree C. Measurements of stand-by current were made after each irradiation step with the Advantest test system. The Toshiba flash memories were erased, then programmed with zeros, and read to validate stored data before irradiated. After each irradiation, the stored pattern (all zeros) were checked. The devices were erased again to ensure the working condition of its internal state machine. The all zeros pattern was written to the parts and re-verified before the irradiation process repeats until failures of read, erase and write operation were encountered. The charge pump circuits of lower density NAND flash memory devices have been cited as the main cause of the erase and write failures at around 8 to 14 krad(Si) in previous publications [5][6]. However, the Toshiba 1Gb flash memories had read errors at 14 krad(Si) as shown in figure 6. There are two possibilities in Toshiba 1Gb read errors. Most sense-amps need to differentiate the cell threshold voltage around 1 to 7 volts. So for a 3.3 volt flash memory part, the charge pump circuit requires to generate a higher voltage level, but still less than the 12 or 20 volts necessary for the erase operation in NOR and NAND process, respectively. So the charge pump remains a primary cause of the read errors. Sense-amps may be damaged at 14 krad(Si).

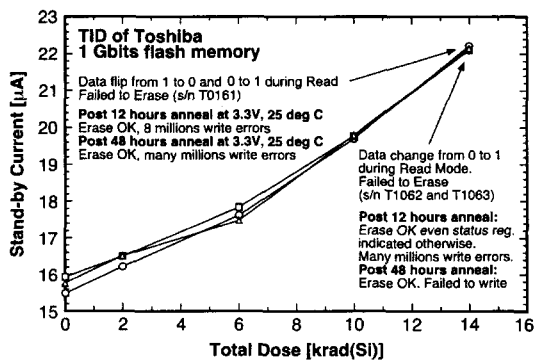

Figure 6: Read errors were observed at a low total dose. Lower density NAND flash memories had no read errors at 14 krad(Si).

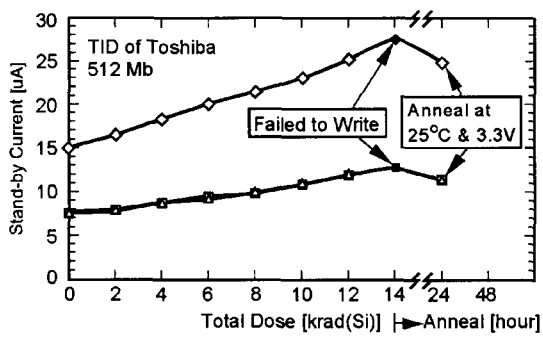

Figure 7: The 512 Mb NAND flash memories failed to write at 14 krad(Si)

CONCLUSIONS

Higher density flash memories inherited larger cross-sections in both read and write operations. They also experienced early read failures at a lower total dose. The sensing circuitry implemented in the multi-level flash memories takes more area due to the adding threshold reference levels. To compensate for additional sense-amps, cell sizes of multi-level flash devices have to be scaled down very close to the limitation. Different non-volatile memory has been researched, and the future replacement of flash memory parts will be closer with the introduction of 4-Mbit ovonic unified memory.

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