# Single-Event Upset in Advanced Commercial Power PC Microprocessors

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Abstract
Single-event upset from heavy ions in measured for advance commercial microprocessors, comparing upset sensitivity in registers and d-cache for several generations of devices. Multiple-bit upsets and asymmetry in registers upset cross sections are also discussed.

## I. Introduction

Commercial microprocessors with the PowerPC architecture are now available that use partially depleted silicon-on-insulator (SOI) processes to improve performance. SOI technology has potential advantages for single-event upset (SEU) compared to CMOS bulk counterparts because, from a fundamental standpoint, charge collection is limited to the shallow depth of the silicon film. However, a recent study of first-generation SOI microprocessors from two different manufacturers showed that although the cross section was lower than for processors with bulk/epitaxial substrates, the threshold LET was very nearly the same [1].

An early study of charge collection by Massengill, *et al.* [2] as well as more recent work on the sensitivity of SOI structures to neutrons and alpha particles [3,4] have shown that charge multiplication by the parasitic bipolar structure increases the collected charge by as much as a factor of ten compared to charge deposited by the primary particle interaction. That mechanism is the likely reason for the low threshold LET of commercial SOI processors. Although manufacturers consider atmospheric radiation effects in their designs [5,6], the relatively low charge produced by alpha particles and neutrons is roughly equivalent to an LET of 2 MeV-cm$^2$/mg. Thus, hardening efforts by manufacturers are relatively ineffective in improving radiation hardness in the more severe environments in space.

Upsets in the L1 cache – a 256-kbit *d*-cache and 256-kbit *i*-cache for the latest PowerPC devices - are the largest contribution to upset rates for most applications of unhardened commercial processors. The sensitivity of the cache to SEUs and multiple-bit upsets (MBUs) is of great concern for microprocessors in space. This paper examines single-event upset in advanced commercial microprocessors, comparing upset sensitivity in registers and the d-cache for several generations of devices (*the i-cache was not evaluated*). Multiple-bit upsets and asymmetry in register and cache upset cross sections are also discussed. Initial results are presented for bulk processors with 0.22 and 0.20 μm feature size from two manufacturers, as well as SOI processors with feature sizes of 0.18 and 0.13 μm. New results for the next generation of SOI PowerPC microprocessors will be included in the final paper.

## II. Experimental Procedure

### A. Device Descriptions

The Motorola 7455 and IBM 750FX are the first generation of the PowerPC family to be fabricated with SOI technology. They use partially depleted technology without body ties. The Motorola device has a feature size of 0.18 μm with a silicon film thickness of 110 nm and internal core voltage of 1.6 V. The IBM part is fabricated with a more scaled process, using a feature size of 0.13 μm, silicon film thickness of 117 nm and core voltage of 1.4 V [7]. Both devices are packaged with "bump bonding" in flip-chip BGA packages.

A more advanced version from Motorola, with a feature size of 0.13 μm, has been announced, with first delivery in March. Radiation test results for that device will be included in the full paper. This will provide a direct comparison of the effects of scaling and process changes for current SOI processes with regard to radiation hardness for devices from a single manufacturer.

### B. Experimental Methods

Radiation testing was done at the Texas A&M cyclotron, irradiating devices from the back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. The Motorola SOI processors were mechanically thinned. Details of the testing, ion energies, and the method used to correct for LET are described in [1,8].

Register and cache tests were done with special "tight loop" software that continually interrogated stored bits during each beam run. The details relating to those evaluations are the focus of the present paper. Global malfunctions (hangs and crashes), as well as the results

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of functional tests of the microprocessors at maximum operating speed were discussed previously in [1,8].

## III. Test Results

### A. Motorola Processors

Register Tests

Fig.1 displays results of cross section measurements for the Motorola SOI PowerPC (7455) Registers (sum of FPR, GPR, and SPR) for "0" to "1" and "1" to "0" transitions. Note the pronounced asymmetry in the response. The threshold LET for "0" to "1" transitions is about 6 MeV-cm$^2$/mg, about a factor of six higher than for transitions in the opposite direction. The cross section for the two logic directions is also different.

That asymmetry was barely evident in register tests of the Motorola G4 processor, with bulk substrate, as shown

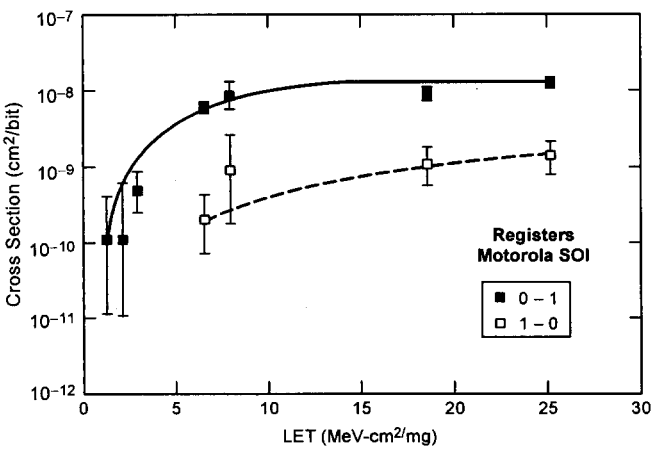


Fig. 1. Heavy-ion cross-sections for registers (FPR+GPR+SPR) of the Motorola SOI PowerPC for "1" to "0" and "0" to "1" upsets.

in Figure 2. Note that exactly the same test approach was used for both types of processors. The saturated cross section of the SOI processor is about $10^{-8}$ cm$^2$/bit, about an order of magnitude lower than that of CMOS epi PowerPC (G4), which has nearly the same feature size as that of the SOI version. Similar differences in cross section between SOI and bulk technology devices were reported in References 9 and 10.

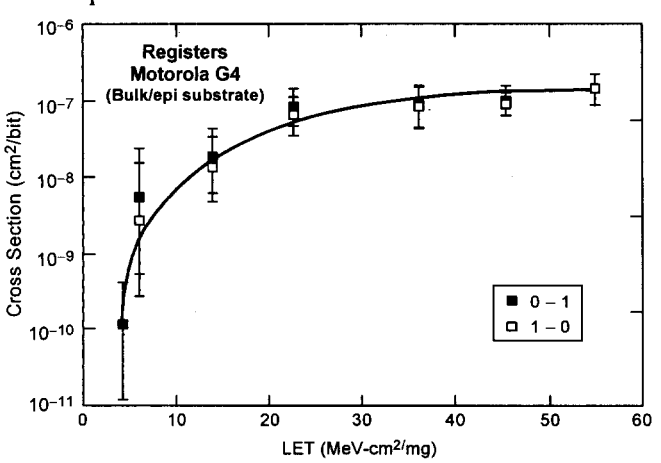


Fig. 2. Heavy-ion single-event-upset cross-section for the Registers (FPR+GPR+SPR) of the Motorola 7400 PowerPC for "1" to "0" and "0" to "1" upsets.

Cache Tests

Tests of the *d*-cache in the SOI version of the Motorola processor did not show the asymmetry in response for different stored logic levels that was seen in the register tests; the cross section was the same for upsets in both directions in the SOI processor as well as the G4 (with epi- substrate). The "saturation" cross section at high LET, where the curve becomes nearly flat, was about a factor of three lower for the cache than that observed for registers for both the SOI and bulk processor types. This is directly related to the more compact design used for 6-T memory cells within the cache compared to memory cells in the registers [11].

### B. IBM Processors

A similar asymmetry was observed between "0" to "1" and "1" to "0" upsets for the IBM SOI PowerPC registers (FPR+GPR+SPR), although the asymmetry was reversed (worst for "1" to "0" upsets) compared to results for the SOI processor from Motorola. Fig. 3 shows the results. The saturated cross section for "1" to "0" upsets is $7 \times 10^{-9}$ cm$^2$/bit.

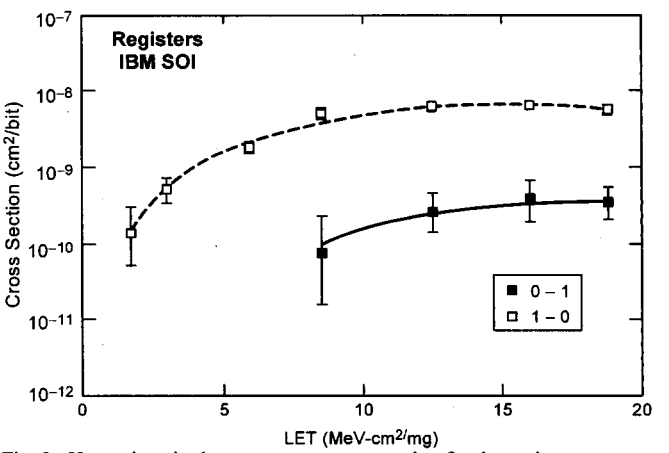


Fig. 3. Heavy-ion single-event-upset cross-section for the registers (FPR+GPR+SPR) of the IBM750FX SOI PowerPC for "1" to "0" and "0" to "1" upsets.

Fig. 4 shows cross section results for the bulk version of the IBM PowerPC registers for "0" to "1" and "1" to "0" upsets. There is a slight asymmetry in sensitivity for the two different logic state directions, but it is much smaller than the approximate order of magnitude difference observed for the SOI design.

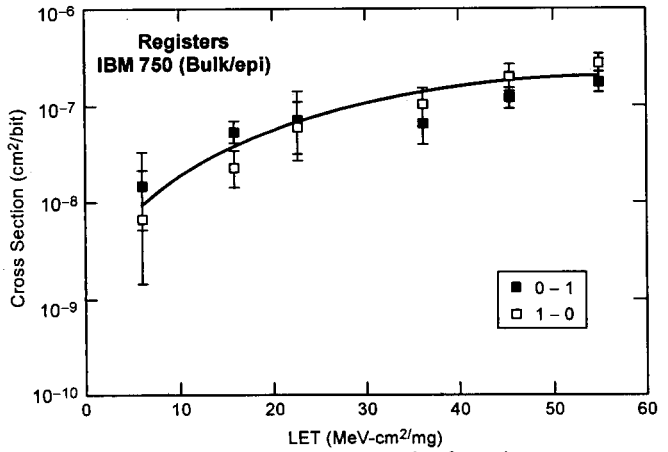


Fig. 4. Heavy-ion single-event-upset cross-section for registers (FPR+GPR+SPR) of the IBM750 PowerPC for "1" to "0" and "0" to "1" transitions (bulk substrate).

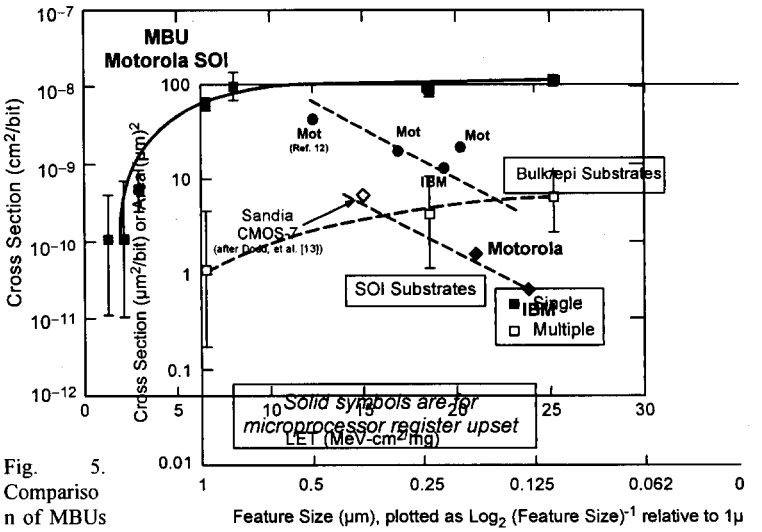


Fig. 5. Comparison of MBUs and SEU cross-sections for registers of the Motorola SOI PowerPC.

### C. Multiple-Bit Upsets

Measurements of multiple-bit upsets are not straightforward for these complex devices because of the latency period that is needed between successive measurements of registers or cache. Low flux rates are required, which conflicts with many of the requirements for detecting single-bit errors, functional errors, and doing tests in a time-efficient manner. Consequently, it was not possible to determine the true MBU rate in our initial test results of the *d*-cache because of interference from coincidental individual upsets on the cache. However, it was possible to measure multiple-bit errors on the registers, because of their smaller size, which reduced the time interval between successive interrogations of the register states during each test run.

Fig. 5 shows the multiple-bit upset rate – defined as two or more bit upsets in the same register - for the SOI version of the Motorola PowerPC. For comparison we also show results for single upsets. The MBU upset rate is about 25 times lower, and begins to occur at relatively low LETs. This result is somewhat surprising because of the very shallow charge collection depth from the silicon film (110 nm for this device). The full paper will include results from a new set of tests that are specifically designed to examine MBU in the *d*-cache for both SOI processors, improving the counting statistics.

## IV. Discussion

### A. Scaling Trends

As discussed in the Introduction, the threshold LET of commercial processes has changed very little with scaling, and is only slightly influenced by the concerns of mainstream manufacturers with atmospheric radiation. However, the saturation cross section has steadily decreased with smaller feature size. Fig. 6 shows how the cross section for registers has changed over several generations of the Power PC family [the abscissa is a logarithmic (*base 2*) scale reflecting the approximate doubling of feature size over various generations of CMOS devices]. The dashed lines show a slope of minus one-half, reflecting the assumed dependence of area on the square of the feature size. There is a decrease of nearly a factor of ten in cross section with the transition to SOI processes.

The earliest results, with 0.5 μm feature size, are from Bezerra, *et al.* in 1997 [12]. New results for test SRAMs from the Sandia CMOS-7 SOI process are also include from Dodd, *et al.* [13]. The Sandia results agree well with the results from the two SOI processors, which have even smaller feature size.

A similar plot for saturation cross sections of the *d*-cache is shown in Fig. 7. Again, the cross section trend for SOI processors is about a factor of ten lower than for bulk devices. Note also that the cross section for the *d*-cache is a factor of 2.5 to 4 lower than the cross section for registers in the previous figure. That difference is due to the smaller cell area used for cache design, which optimizes performance and reduces chip area. The gate and drain area of transistors in the IBM cache, provided by the manufacturer, are shown for comparison. The total cross section is slightly less than the sum of the areas of the drain and gate, which agrees with results obtained by

the Sandia group in microbeam studies of devices from their SOI process, with 0.35 μm feature size [13].

Fig. 6. Scaling trends for upset in registers (and basic SRAM designs) for Power PC processors. Results for test SRAMs from Dodd, *et al.* [13] are also included for comparison.

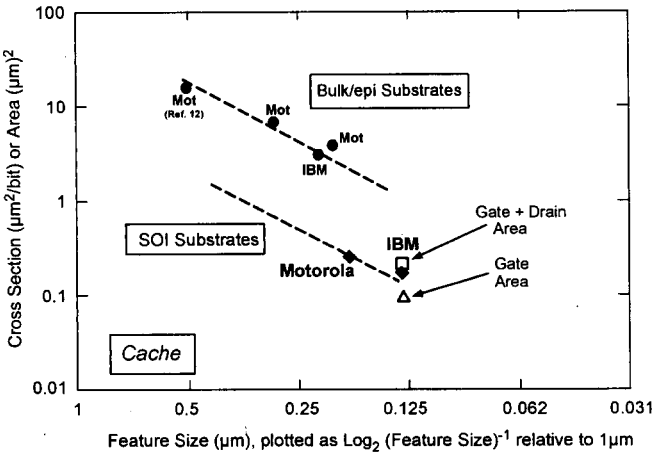


Fig. 7. Scaling trends for upset in d-cache for Power PC processors.

The combination of the transition to SOI technology and the decrease in feature size reduces the error rate in deep space by more than a factor of 30 compared to error rates calculated for the Motorola PC750 (bulk/epi substrate with 0.29 μm feature size) [8]. The error rate in deep space (solar minimum) decreases from $10^{-6}$ to 3 x $10^{-8}$ errors per bit day, and would be approximately halved by taking the asymmetric cross section into account. That is an impressive reduction. Error rates will be discussed more completely in the full paper, along with geometrical arguments for asymmetric responses in registers.

*B. Multiple-Bit Upset*

The sensitivity of the Motorola SOI device to multiple-bit upset was unexpected, because earlier work showed that SOI upset only occurs for gate strikes. However, more recent work has shown that strikes in the drain also contribute to the cross section [13]. This provides a possible mechanism for charge sharing between adjacent isolated films in PD SOI from a particle strike in regions that are closer to the isolation regions. Schwank, *et al.*, discussed the possibility of MBU from displacement currents in the underlying isolation oxide, which is a potential mechanism for MBU in these devices [14]. New MBU results in the full paper for the Motorola processor with 0.13 μm feature size may provide additional insight in how scaling affects multiple-bit upset.

*C. Design Issues*

Although future processors may use DRAMs, the cache and registers in these processors use 6-T SRAM cells. Design of compact SRAM cells is extremely complex. Although SOI provides some advantages, the history dependence, pattern dependence from bipolar currents and self-heating must all be taken into account [15]. New circuit design approaches using low threshold transistors improve speed and power dissipation, but reduce internal noise margin [16]. These factors, along with geometrical factors (such as extended regions for contacts, which causes asymmetric cross sections in earlier work on 4-T SRAMs [17]) may contribute to the asymmetric cross sections that were observed for registers in the SOI processors. This will be discussed further in the full paper.

## V. Conclusions

This paper has discussed scaling trends for SEU from heavy ions in the Power PC family of microprocessors, emphasizing upsets in registers and cache. The latest versions of these processors have error rates that are more than 30 times lower than PowerPC 750 processors because of the reduced feature size and the transition to SOI. Multiple-bit upset was observed in register tests of an SOI processor with 0.18 μm feature size. This is not only important from a fundamental standpoint, but makes implementation of error correction methods more difficult.

The final paper will include data for the Motorola PowerPC 7457 (0.13 μm), comparing it with the Motorola SOI processor with a feature size of 0.18 μm. This will help to determine whether the trend towards improved hardness is likely to continue as scaling progresses.

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