

Saturation Current Model for the N-channel G⁴-FET

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Abstract. A new saturation current model is presented for the n-channel G⁴-FET, a novel 4-gate transistor. The model is verified against measurement results from G⁴-FETs fabricated using a standard 0.35-micron partially-depleted SOI process. Since the G⁴-FET is an accumulation-mode device, the conventional first-order JFET model provides the basis for the G⁴-FET saturation current model. The JFET gate-to-source voltage is replaced by V_{JG} , the bias voltage applied to the G⁴-FET's junction (or lateral) gates. Then, to include the additional MOS gate bias effects exhibited by the G⁴-FET's saturation I-V characteristics, the new model develops hierarchical equations for the JFET zero-bias saturation current parameter, I_{D0} , and the pinch-off voltage, V_p . Parameter values for the new model were extracted using curve-fitting techniques.

INTRODUCTION

The G⁴-FET is formed using the normal layout of a SOI MOSFET with the addition of two explicit body contacts on opposite sides of the MOSFET. The MOSFET layout's source and drain are the two junction gates of the G⁴-FET (JG1 and JG2 – see Figure 1). The source and drain of the G⁴-FET are the two separate body contacts of the MOSFET structure. Table 1 indicates the conversion of parameters between the G⁴-FET and a common MOSFET. The channel of the G⁴-FET is coincident with the body of the MOSFET, therefore an inversion-mode p-channel MOSFET is an accumulation/depletion-mode n-channel G⁴-FET. The top poly gate (G1) can still be used to modulate the current, as well as the back gate (G2) formed by the SOI substrate beneath the buried oxide. Figure 1 shows a three dimensional view of a G⁴-FET. The attractiveness of the G⁴-FET comes from the unique opportunity to independently command four separate gates. Single transistor logic functions, novel analog/mixed-signal circuits, low-power modulation for RF applications, and emulation of quantum wires are just a small number of the exciting opportunities envisioned using the G⁴-FET and leveraging its multiple gates.

Table 1. Conversion from MOSFET to G⁴-FET

MOSFET	↔	G ⁴ -FET
p-channel	↔	n-channel
n-channel	↔	p-channel
Width	↔	Length
Length	↔	Width
Source/Drain	↔	Lateral junction gates
Body contacts	↔	Source/Drain

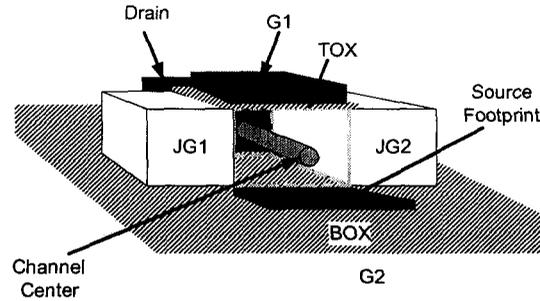


Figure 1. Three-dimensional view of the G^4 -FET structure.

The G^4 -FET operational characteristics have been presented in [1]. In this paper, the saturation current model for an n-channel G^4 -FET will be presented. The model development section will describe the extraction techniques used to achieve parameter values for various bias conditions. Then, the next model section will demonstrate and explain the developed model. The accuracy of the model will be compared to measured data in the results section.

MODEL DEVELOPMENT

The conventional saturation model for the JFET [3] is used as a starting point for the G^4 -FET model. The model is developed using measured data from n-channel devices fabricated in $0.35\mu\text{m}$ PDSOI. During the measurement, the lateral junction gates (JG1 and JG2) were tied together for simplicity. Three basic JFET model parameters were extracted from the G^4 -FET measured data [4]:

- pinch-off voltage (V_P) that corresponds to the junction bias necessary to suppress the current,
- zero-bias saturation current (I_{D0}), measured for V_{GS} (V_{JG}) = 0V, $V_{DS} = 4$,
- channel length modulation (λ) that accounts for non-zero conductance in saturation operation.

Values were extracted for varying top gate (G1) bias conditions such that unique values for V_P , I_{D0} , and λ were obtained for each top gate bias condition. Behavioral models for V_P , I_{D0} , and λ were then developed to describe their dependence on top gate bias voltage. The resultant equations form the basis of the n-channel G^4 -FET saturation model described in the next section.

G^4 -FET MODEL

Though the basis of the G^4 -FET saturation model is formed from first-order JFET theory,

$$I_{Dsat} = I_{D0} \left[1 - \frac{V_{JG}}{V_P} \right]^2 (1 + \lambda V_{DS}), \quad (1)$$

the conventional parameters V_P , I_{D0} , and λ are not constants in this new model due to the multiple control gate natural of the G^4 -FET. The new V_P , I_{D0} , and λ behavioral equations were derived using a standard curve fitting approach and measurement data obtained at different top gate bias conditions.

The derived pinch-off voltage expression for the G^4 -FET model is

$$V_P = W \left(E_{Pjg} + \phi_{vp} (V_{g1} - k_{vp})^2 + E_{Pg1} \right). \quad (2)$$

Parameter definitions are provided in Table 2. Similar to normal JFET operation, V_P is shown to be linearly proportional to the channel width of the device. Interestingly, the pinch-off voltage exhibits a square-law dependence on top gate bias (V_{g1}), indicative of MOS action. The top gate (G1) and bottom gate (G2) are biased at 0V and the pinch-off parameter for the junction gates ($W \times E_{Pjg}$) is extracted using conventional extraction techniques outlined in [4] (V_P is the x-intercept taken from the I_{DS} versus V_{JG} measured data). This technique is also used to extract the pinch-off parameter with a varying top gate bias from -1V to 3V. The extracted parameters from the top gate bias conditions are used to develop the equation for the top gate influence on V_P .

Equation (3) shows the zero-bias saturation current parameter equation, which is also somewhat similar to the effect seen in a standard JFET. Again, due to the current modulation induced by the top gate bias, this equation also has a square-law dependence on V_{g1} . The extraction techniques for the I_{D0} parameter are similar to the techniques used in the V_P parameter extraction. The top gate and bottom gates are again biased at 0V and the I_{D0jg} parameter is extracted using the y-intercept of the I_{DS} versus V_{JG} measured data. The I_{D0} y-intercept value is also extracted for varying top gate voltages of -1V to 3V. These results are then used to develop the equation for the top gate influence on I_{D0} as shown below.

$$I_{D0} = \left(\frac{W}{L} \right) \left(I_{D0jg} + \phi_{id0} (V_{g1} - k_{id0})^2 + I_{D0g1} \right) \quad (3)$$

For G^4 -FET channel length modulation, the normal JFET equations were extensively altered. The top gate bias and the junction gate bias each have an exponential impact on this parameter as shown in equation (4). More tests are being conducted to further understand this outcome. The extracted parameters for the channel length modulation parameter λ differ from the previous extraction techniques due to the strong bias dependence on both the junction gate and the top gate. With the bottom gate fixed at 0V, the λ parameter is extracted using the measured slope of the I_{DS} versus V_{DS} characteristic divided by the I_{DS} current value at a specific gate voltage. This method is based on the assumption that small-signal output conductance, g_{ds} , is approximately λI_{DS} . The λ values extracted from the measured data are then used to form exponential expressions to describe the influence of the top gate and lateral junction gates.

$$\lambda = \lambda_{eff} + \left[\lambda_{jg} \left(e^{\phi \lambda_{jg} V_{jg}} \right) + k_{\lambda_{jg}} \right] + \left[\lambda_{g1} \left(e^{\phi \lambda_{g1} V_{g1}} \right) + k_{\lambda_{g1}} \right] \quad (4)$$

Note that the poly gate plays a primary role ($\phi_{\lambda_{jg}} = 2$). Coefficients $\phi_{\lambda_{jg}}$ and $\phi_{\lambda_{gl}}$ have opposite signs because normally $V_{jg} < 0$ and $V_{gl} > 0$.

These equations can be used to estimate the saturation current of a device with a channel width of $0.4\mu\text{m}$ and a channel length of $0.9\mu\text{m}$. The saturation model is accurate for a back gate bias of 0V, junction gate bias ranging from -4V to 0V , top gate bias level of -1V to 3V , and drain-to-source voltage of 3.5V to 10V . Table 2 lists the notions and values of the new parameters used to model the n-channel G^4 -FET.

Table 2. Extracted parameters for G^4 -FET fabricated in standard $0.35\mu\text{m}$ PDSOI.

Parameter Name	Parameter Symbol	Parameter Value
Effective Zero Bias Drain Current for Junction Gate	I_{D0jg}	$78.2\mu\text{A}$
Effective Zero Bias Drain Current for Top Gate	I_{D0gl}	$-8.30\mu\text{A}$
Effective Pinch-off Field for Junction Gate	E_{pjg}	$-10.1\text{V}/\mu\text{m}$
Effective Pinch-off Field for Top Gate	E_{pgl}	$0.865\text{V}/\mu\text{m}$
Fitting Constant pinch off	k_p	-2.1V
Fitting Constant Drain current	k_{id0}	-1V
Fit Parameter for Pinch off	ϕ_{vp}	-0.3μ
Fit Parameter for I_{D0}	ϕ_{id0}	25k
Effective Lambda	λ_{eff}	1m
Effective Lambda for Junction Gate	λ_{jg}	280μ
Effective Lambda for Top Gate	λ_{gl}	55μ
Fit Parameter for effect of Junction Gate on Lambda	$\phi_{\lambda_{jg}}$	-1
Fit Parameter for effect of Top Gate on Lambda	$\phi_{\lambda_{gl}}$	2
Fit Constant for effect of Junction Gate on Lambda	$k_{\lambda_{jg}}$	-100μ
Fit Constant for effect of Top Gate on Lambda	$k_{\lambda_{gl}}$	448μ

RESULTS

The n-channel G^4 -FET saturation current model is used to calculate current levels for varying voltages on junction gate, top gate, and drain. Figure 2(a) shows the characteristics with sweeping junction gate bias and top gate bias as a parameter while Figure 2(b) is the reciprocal characteristic for swept top gate bias. In Figure 2(a), the current is decreasing as the channel gradually narrows until pinch-off occurs when both the junction gates and top gate become strongly depleted. Zero saturation current infers that the transistor body is fully depleted either by lateral junction gate (JFET) action or combined JFET plus MOS actions. In Figure 2(b), the saturation current increases with top gate bias, particularly as the top gate becomes strongly accumulated for positive values of V_{Gl} . Figure 2 indicates that the saturation current model accurately predicts drain current for junction gate bias in the range of 0V to -4V and top gate bias of -1V to 2V . As the top gate heavily accumulates the channel, say in the top gate bias range of 2V to 3V , the accuracy of the saturation model weakens. This effect is still under investigation.

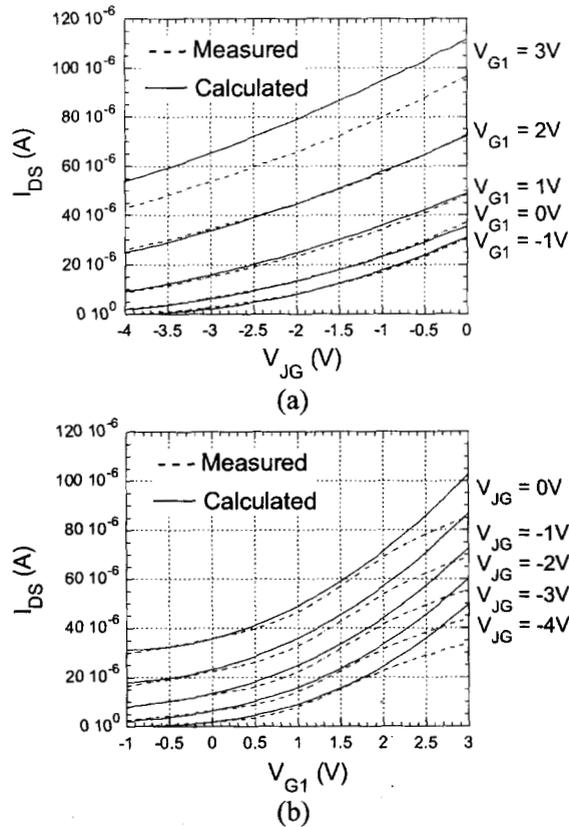


Figure 2. Saturation drain current vs. junction gate (a) and top gate (b) for n-channel G^4 -FET with varying gate voltages. $V_{DS} = 4V$, $V_{G2} = 0V$, $W = 0.4\mu m$, and $L = 0.9\mu m$.

Figure 3(a) shows the characteristics with sweeping drain voltage bias and junction gate voltage bias as a parameter while Figure 3(b) is sweeping drain bias with top gate bias as a parameter. In Figure 3(a), the current modulation across drain voltage is minimal due to high output resistance. However, in Figure 3(b), the channel length modulation of the device increases at higher current levels, as one might expect, thus weakening the output resistance. Here again, the accuracy of the model is compromised at high levels of top gate accumulation.

CONCLUSION

The model presented displays the complexity of this novel device. The model presented can be used to develop circuit topologies for applications exploiting the multiple gate characteristics of the G^4 -FET. Additional work will extend this model to account for all points of operation (linear and saturation) and for more extensive gate biasing conditions (e.g., varied back gate bias).

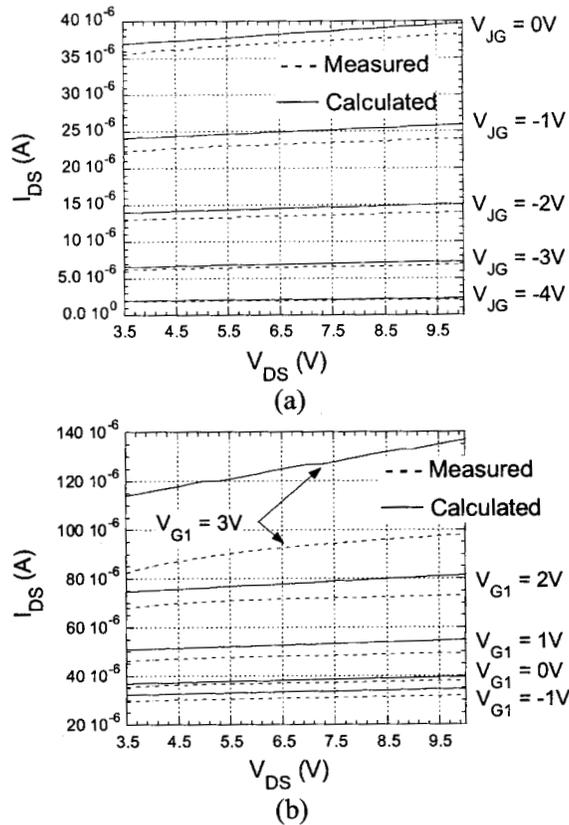


Figure 3. Saturation drain current vs. drain voltage for n-channel G^4 -FET with varying junction gate bias levels (a) and varying top gate bias levels (b). $V_{G2} = 0V$, $W = 0.4\mu m$, and $L = 0.9\mu m$.

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