Integration of Analyses in an EMC Control Plan for Avionics Hardware in Space Applications

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Abstract: **An EMC Control Plan is a very valuable tool for outlining the processes needed to suppress EMI and provide EMC for the avionics hardware used in space applications. The EMC Control Plan provides guidance to EMC engineers and avionics hardware designers on methods, procedures, and practices to achieve optimum EMC. The design of an EMC Control Plan for space avionics requires unique challenges due to the nature of the space missions and the space environment. An EMC Control Plan for avionics hardware in space applications can be optimized by the integration of reliability and margin analyses that are uniquely suitable to space applications and avionics hardware. The paper provides a description of the analyses and the rationale for the inclusion of such analyses in the EMC Control Plan, including some examples. The paper concludes by providing a detailed outlined of an EMC Control Plan for avionics hardware in space applications and how this approach fits well with the overall avionics hardware design and development cycle.**

Keywords---EMC control plan, reliability analysis, margin analysis, space, avionics, worst case analysis, interface fmeca.

I. Introduction

Most space applications require testing of avionics hardware to address potential electromagnetic interference (EMI) per applicable Electromagnetic Compatibility (EMC) requirements for the particular hardware. The EMC requirements are also, most often tailored to the mission profile and its requirements. An EMC Control Plan provides guidelines and best practices to achieve success in EMC.

It is common in the development of avionics hardware to create an EMC Control Plan. An EMC Control Plan also addresses general design principles that hardware designers should adhere to minimize EMC problems in hardware development. The results of this EMI minimization process during design translate into reduced EMI problems during performance testing and formal EMC certification testing of the hardware. Though design engineers usually follow their own EMC design practices, an EMC Control Plan can provide them with additional proven design practices, which they can use to avoid serious EMI problems at the board, box, and even system level. For hardware already developed, or in the advances stages of developmental cycles, the EMC Control Plan can outline preliminary or "risk reduction" EMC tests. These EMC tests provide early indication of EMC interference problems, which when addressed early in the development process, can avoid even larger EMC problems at the conclusion of full hardware development. Therefore, the EMC Control Plan should also address legacy or heritage equipment.

Several examples of existing EMC Control Plans are shown in [1-5]. The EMC Control Plans outlined in [1-2] have been tailored to avionics hardware in space systems. An EMC Control Plan for a given space avionics hardware must always adhere to specific mission requirements in addition to specific hardware requirements. In essence, the EMC Control Plan must reflect a subsystem and even a system view of the requirements in order to be properly effective, since avionics hardware are usually utilized in an integrated manner.

The paper proposes an innovation to the writing of an EMC Control Plan for space avionics by the inclusion of reliability and margin analyses that designers and EMC engineers can implement in the hardware development process to address EMI issues. It has been the experience of this author that incorporating reliability and margin analyses has resulted in minimizing, and in many cases eliminating, EMI issues that could have manifested themselves during EMC testing. Resolving EMI problems before EMC testing is always the preferred approach.

II. Implementing Analyses in the EMC Control Plan

A process in the space industry during the design and development of avionics hardware is the implementation of certain types of electronic analyses, depending on the type of hardware design, during the development cycle. The application of both engineering design processes and electronic analyses provide optimization in hardware performance. Corroboration that the performance requirements were met is confirmed during hardware performance testing at the end of the hardware development cycle. From an EMC point of view in addition to meeting hardware performance requirements space avionics hardware must also meet "self" and "shared" EMC compatibility with the other avionics hardware and sensors in the space system. Often, managing EMC within a space system is a challenge. Therefore, a series of targeted reliability and margin analyses in certain types of avionics hardware circuitry are recommended to be included in an EMC Control Plan to address potential EMC problems in the design and developmental phases.

A unique issue with space applications of avionics hardware is the space environment and the nature of space missions. Concerning the nature of the space missions, EMC problems are very unlikely to be resolved once the avionics hardware is in space, hence the need to maximize the effort to solve EMC problems during the design and development cycles of the hardware. Furthermore, space missions can be very long in duration; hence, the avionics hardware needs to be designed and built for maximum reliability. It is also well understood that the space environment is highly detrimental to the electronics in the avionics, and this exacerbates the problem of EMI generation. Therefore, avionics hardware must be designed and built for the worst-case space environmental conditions of temperature, space radiation, length of time, and the changing parameters of electronic parts due to damage from the space environment. There are several types of reliability and margin analyses useful to perform for early identification of potential EMC problems. We can outline a few of these but the list is not all-inclusive.

A. Electronics Worst Case Analysis

The Electronics Worst Case Analysis (EWCA) allows for the evaluation of electronic circuits, for both, performance and EMI control under the worst-case space environment conditions as previously stated. The EWCA can be useful in addressing EMC problems early in the avionics hardware design cycle because it contributes to the design of circuits whose performance can be maximize for generating the least amount of conducted EMI or allow the for the least amount of conducted EMI propagation. For example, consider the power line EMI filter in Fig. 1. The main function of the low frequency (LF) EMI filter in Fig. 1 is to suppress the conducted EMI generated by the switching mode power supply (SMPS) to propagate into the main power bus (Vin).

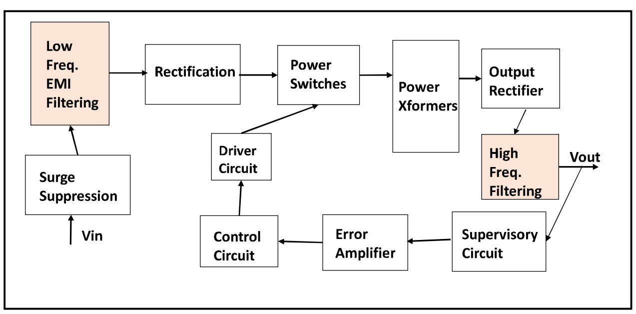

Fig. 1. Low and High Frequency Filters in a SMPS

The EWCA allows for the performance of the EMI filter to be modeled in two steps: (a) the noise suppressing capabilities of the EMI filter can be modeled a priori and then assess the filter's capabilities against the required filter specifications. The modeling analysis will help in providing a preliminary design of the filter, and (b) the EWCA will then be use to allow for the evaluation of the preliminary EMI filter design under worst-case space environmental conditions to aid in the final EMI filter design. Fig. 2 shows the need for such a process. As an example of previous work reviewed by this author on a low pass filter design for an application, Fig. 2 shows a computer modeling and simulation of the conducted emissions on a 28V power bus with an EMI filter that was modeled without using EWCA. Fig. 2 also shows a computer modeling and simulation of the conducted emissions on the same power bus and the same EMI filter using EWCA. Fig. 2 shows that the conducted emissions spectrum above 500 KHz increased in magnitude for several frequencies (frequencies shown in red color for ease of identification) when using EWCA. Therefore, under worst case conditions it is observed that the performance of the EMI filter deteriorated. The design of the EMI filter needed to be improved, but such improvement was never pursued and no further analysis was needed because the increased emissions were still well below the emission limits requirements. The EWCA can be used as an aid in the design of low and high frequency power line EMI filters as shown in Fig.1. These types of results show that EWCA can be used to improve the design of hardware that will perform per its requirements under worst-case space environmental conditions.

The results of the EWCA in Fig. 2 are only applicable to the given topology being analyzed. Power line EMI filters vary substantially in their design and most important, in the type of components being used. For example, some EMI power line filters designs combine a linear passive low pass filter with active non-linear circuitry to provide a slow-start for the bus voltage application. Also, the effect of components' parameters variations due to space environmental conditions depends greatly on the type of components used for the filter, the number of each type of components used, and the quality of the components (i.e. manufacturing and qualification processes). Therefore, it is expected that the results obtained in Fig. 2 can vary greatly depending on the topology of the power line EMI filter used. In the results of Fig. 2 less attenuation is shown at higher frequencies after the application of EWCA. These results are only applicable to the topology analyze. No additional analyses were performed as previously stated. At present the author can only infer that it was the topology of this filter, including the fact that it was a low pass filter, that allowed for performance deterioration to increase at higher frequencies.

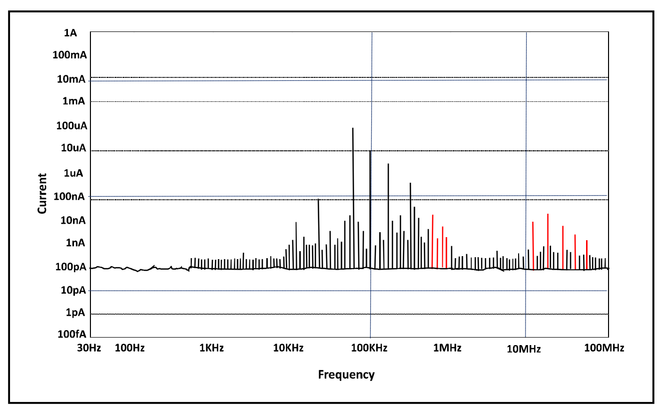

Fig.2. Simulation of conducted emissions using EWCA for the EMI filter

B. Interface Functional Failure Modes Effects and Criticality Analysis

The Interface Functional Failure Modes Effects and Criticality Analysis (IFFMECA) allows for assessing the consequences of functional failures in a circuit (e.g. part(s) failure or failures in performance) and how such functional failures affect the performance of upstream functions in other upstream circuits. For EMI applications the IFFMECA can also show how conducted noise can propagate and affect upstream electronics and their interfaces and how such propagation affects the performance of the electronics. EMI propagation can affect other avionics hardware in manners that can cause the hardware to degrade in its performance or even fail. This is an important issue because when formal EMC tests are performed on a given avionics hardware, only the EMI signature of such hardware is known but there is often not thought as to how such conducted EMI signature will affect other hardware connected to it because such an analysis is often not required for formal EMC compliance. The fact that a piece of hardware "passes" EMI conducted emissions tests does not necessarily means that its conducted emissions will not affect other hardware. In essence, we may lack knowledge about the shared compatibility between two or more avionics connected to each other. The IFFMECA can provide an answer concerning shared compatibility in the presence of shared conducted EMI. For example, let us consider again the simple example of the EMI filters in the switching mode power supply of Fig. 1. Let us consider the scenario in Fig.3 where the high frequency (HF) EMI filter in the SMPS fails to suppress certain high frequency noise in a given frequency band. Let us further consider that an avionics sensor whose biased voltages are supplied by the SMPS must process analog data in the same frequency band where the un-suppressed noise is present. It is very likely during the analog-to-digital (A/D) conversion process at the sensor that high levels of conducted noise during data processing will produce corrupted downlinked digital data as shown in Fig.3. The figure also shows that when the IFFMECA is performed at each of the interfaces the IFFMECA can track how the conducted noise propagates and affects each of those interfaces.

As the IFFMECA tracks and assess the conducted noise propagation across the interfaces, the IFFMECA becomes a guiding document for ways to suppress the effects of EMI and even how to avoid it where applicable.

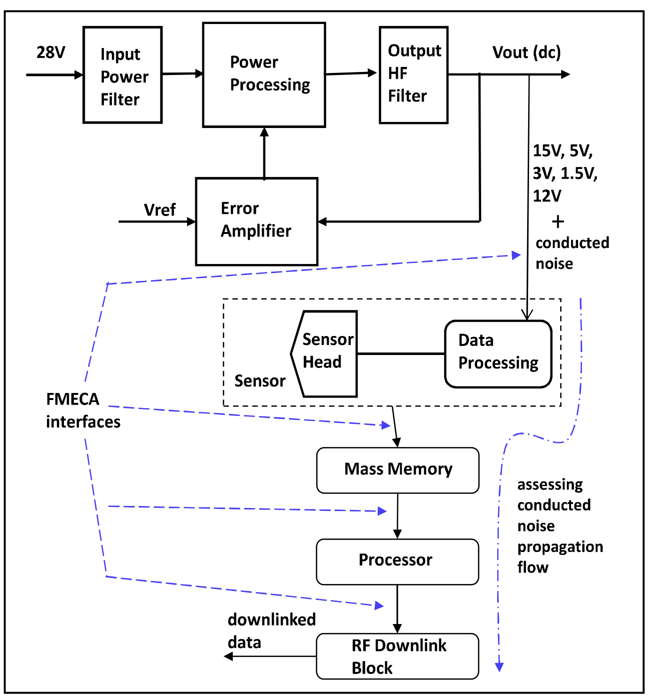

Fig.3. The IFFMECA can track the conducted noise propagation from a source.

C. Interface Worst Case Timing Analysis

The Interface Worst Case Timing Analysis (IWCTA) is a very useful tool. The analysis is used mainly for high-speed interfaces (e.g. up to 10Mb/sec in RS422 in Fig.4) and it is basically a signal integrity (SI) analysis of the interface. The analysis allows for the evaluation of high-speed timing signals across wired interfaces among avionics hardware. For example, the interface between an imaging sensor and a fast memory storage device, or the interface between the fast memory storage device and a downlink RF signal. These types of avionics hardware interfaces are very common in space applications. The evaluation of the SI in high-speed timing signals among these interfaces must account for worst-case timing delays, worst-case setup times, and several other worst case aspects of the overall signal integrity of the signals involved. Because it is a type of worst-case analysis, the IWCTA must account for the worst-case space environmental

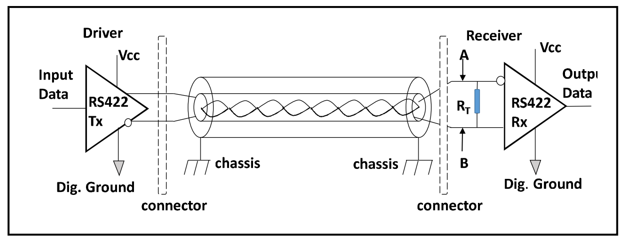

Fig. 4. The RS422 Interface and its transmission line.

conditions and other worst-case requirements of the mission. Consider again Fig. 4 which shows a RS422 interface which is very common in aerospace applications. RS485, MIL-STD-1553, and LVDS interfaces are also very common in aerospace applications. The RS422, RS485, and LVDS interfaces are differential signaling interfaces and they consist of drivers with differential outputs and receivers with differential inputs.

These interfaces have better noise performance because the noise coupling into the system is equal on both signals. One signal emits the opposite of the other signal and electromagnetic fields cancel each other. Furthermore, in aerospace applications the transmission lines are double-shielded for additional immunity. Differential signaling is mostly immune to common mode noise. Therefore, the main issue with these interfaces is not EMI but SI.

The RS422 in Fig. 4 is commonly used to connect data, clock, and command signals in space avionics hardware. The IWCTA for this interface must include the worst-case parameters of all the matching impedance terminations (e.g. resistor R_T in Fig. 4), the driver and receivers ICs, the wiring, the cable shields, and any parasitic elements from a transmission line model perspective. For example, R_T in Fig.4 is formally chosen such that its value would match the characteristic impedance of the transmission line, but the IWCTA could show a different value for R_T which will cause an impedance mismatch. Therefore, under worst-case conditions and with high speed signaling (e.g. 3.6Mbps) and about 6.5 feet of cabling (long cabling is quite common in aerospace avionics) the transmission line will show signal reflections as shown in Fig. 5.

Fig. 5 shows signal reflections in the RS422 interface of Fig.4. Signal reflections can cause several types of SI issues such as intersymbol interference (ISI) and jitter. Jitter can be defined as a type of line distortion caused by a random variation in a signal's reference timing position. The deviation can either be leading or lagging the ideal position and the end result is dropped bits in the transmission. Fig. 5 shows the application of IWCTA and the analysis is divided into four channels. Channel 1 (CH-1) shows the input data signal to the RS422 interface driver. Channels 2 and 3 show the input data signal at locations A and B marked in Fig.4. Channel 4 (CH-4) shows the output signal. As observed in CH-4 the application of IWCTA starts showing a distinct distortion of the output signal due to reflections in the transmission line. As the reflections get more pronounced and depending on the type of interface used SI issues start showing up.

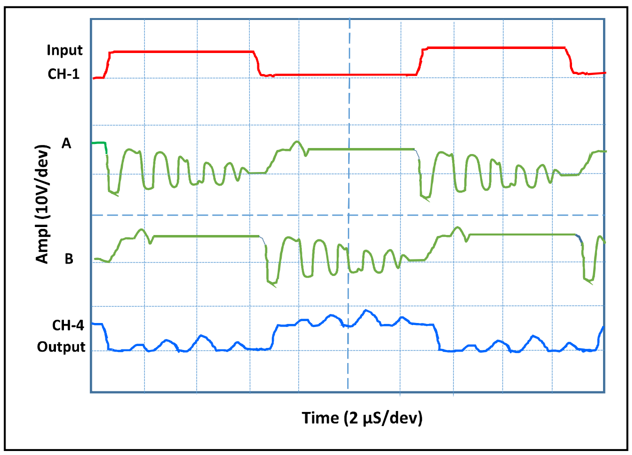

Fig. 5. RS422 signal reflections upon application of IWCTA

D. Radiator-Receiver Margin Analysis

The Radiator-Receiver Margin Analysis (R2MA) can address radiator-receiver margins in a graphical and quantitative fashion. The analysis addresses the susceptibility of both, intentional and unintentional receivers to intentional transmitters within the confined area of a spacecraft (unintentional transmitters are not considered in this paper). In a typical spacecraft, RF transmitters and receivers must coexist, which is often a difficult task since both must share a very confined area in the spacecraft bus. Most often, to avoid RF interference, intentional transmitters and intentional receivers are designed so that their transmitters and receivers bands are well separated, including sidebands, and their operations do not occur simultaneously. However, very problematic interference problems occur with the susceptibility of unintentional receivers to intentional transmitters. This scenario is important because it is typical of the interference effects that intentional transmitters have on science instruments in a spacecraft, which most often operate as receiving passive sensors. In this category, analog sensors in science instruments often play the role of unintentional receivers as shown in Fig. 6. Because of their low threshold of susceptibility (as low as a few millivolts), analog sensors are highly susceptible to EMI. As shown in Fig. 6, the true sensor signals in combination with their added EMI noise are amplified. The analog signals are conditioned for analog-to-digital conversion. The resulting digital signals are highly corrupted. The corrupted digital signals are processed for storage, manipulated, and prepared for transmission. Spacecraft technology is progressing rapidly into advance sensor technology and the need to protect the analog signals from EMI is increasing in importance.

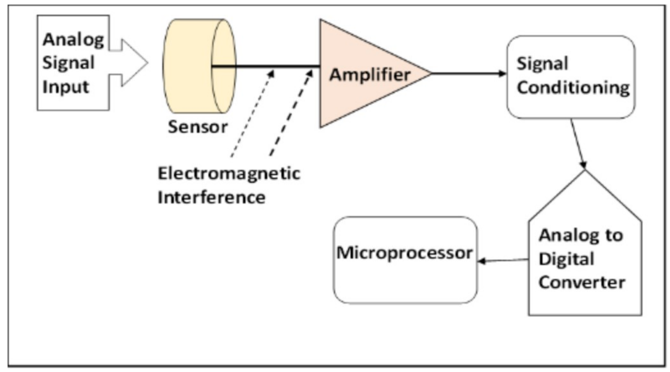

Fig. 6. Ease of Radiated EMI Coupling to Sensor Circuitry

The R2MA is often done in a quantitative fashion (not considered in this paper) using graphical aids as shown in Fig. 7. The figure shows that at certain frequency bands an unintentional receiver is susceptible to an intentional transmitter. Therefore, the transmitter is known as the "offender" and the unintentional receiver is known as the "victim". The figure shows a region of vulnerability where the field strength (electric or magnetic) of the known transmitter is higher than the RF susceptibility threshold of the unintentional receiver at a given frequency band, hence causing interference. Quantitatively, it is possible to estimate the "delta" of susceptibility, i.e. the amount of field strength above the threshold of susceptibility of the receiver. It is sufficient to know for this paper, in a qualitative manner, that such interference exists for which design and EMC engineers must decide on the course of action. There are three main courses of actions: (1) not to allow the transmitter(s) and affected receiver(s) to be operating simultaneously, (2) after a quantitative R2MA, there may be a need for design changes, and (3) impose requirements on the transmitter(s) so as not to violate the "window" of susceptibility of the receiver(s) as shown.

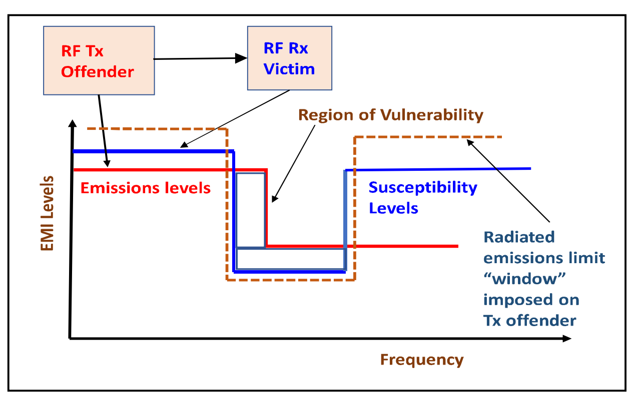

Fig. 7. RF radiated susceptibility of a receiver by a transmitter.

In order to address the potential multiplicity of susceptibility scenarios, a "vulnerability" graph is used. In Fig. 8. RF offenders and victims are paired-up. Fig.8 shows the frequency bands of the offenders. The figure shows that offender 1 in the frequency band ΔF1 interferes only with victim 7 while offender 2 interferes with victims 4 and 6 in the frequency band ΔF2. The vulnerability graph is mostly applicable to intentional transmitters and intentional receivers. However, the vulnerability graph is also applicable to intentional transmitters and unintentional receivers when such can be found. Unintentional receivers can be almost any type of hardware, such as cables and wires for example, but such are not often the case since cables/wires are well protected from field-to-wire/cable interference by good shielding and grounding practices well known in the space industry. It is the "unsuspected" unintentional receiver the one that most often causes unpredictable concerns, as shown in the example of Fig. 9.

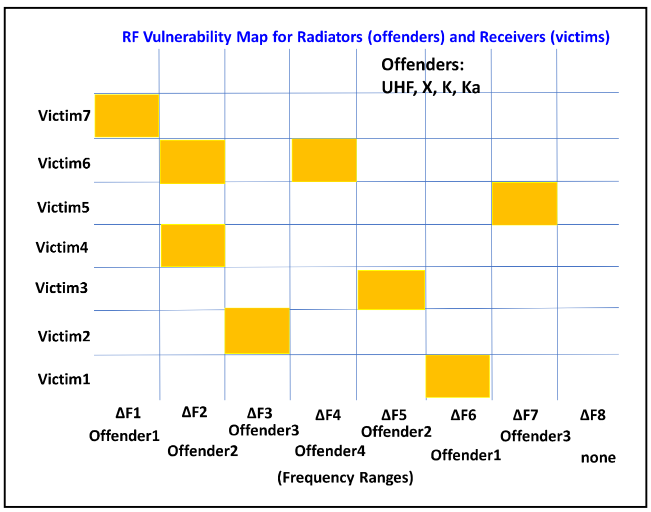

Fig.8. RF Vulnerability Map

Consider the case of Fig. 9 for an intentional transmitter to unintentional receiver interference scenario. A UHF transceiver is commanded to turn-on and to start transmitting and start sending data, in a downlink mode, through a relay station (e.g. another spacecraft).

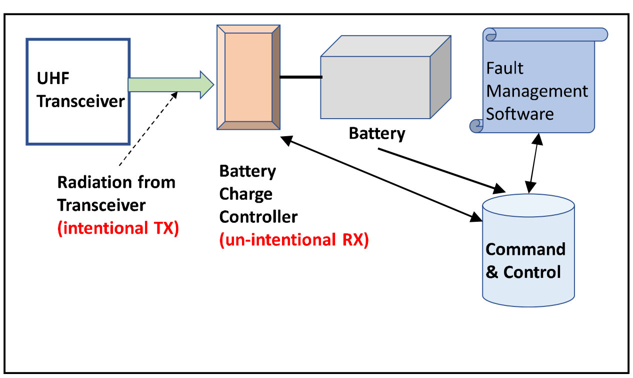

Fig. 9. Illustration of un-intentional radiated EMI coupling

It is observed, via downlinked spacecraft telemetry, that unintentional RF coupling is occurring at the spacecraft battery charger controller analog telemetry electronics. The analog telemetry circuitry, within the battery charger, functions erratically due to the RF interference. The spacecraft downlink telemetry shows the battery is actually discharging! Though the battery is fully charged, and not discharging, the false telemetry causes the command and control unit to start the battery charging of the spacecraft. Overcharging of the battery will cause a thermal run-away in the battery and will disable the battery, a most likely loss of mission. A fault-management software algorithm diagnoses the problem correctly and turns-off the UHF transmitter before the battery is overcharged.

III. A Suggested EMC Control Plan For Space Avionics

This section now proceeds to outline a proposed EMC Control Plan for space avionics. It is proposed that the EMC Control Plan incorporates reliability and margin analyses for specific types of critical electronics that have been known, or suspected in the past, of providing the bulk of potential EMC problems in space avionics. The list of critical electronics is by no means all-inclusive but it is a start and the list should be tailored to the hardware and the space mission type. A suggested list of circuits types are: (a) SMPS EMI filtering (low and high pass), (b) RF transmitter and receivers (intentional transmitters and intentional and unintentional receivers) including antenna terminals, (c) high speed electronic interfaces and wiring, (d) analog sensory electronics for sensors and their signal processing hardware, and (e) pyrotechnics hardware. The new outline of the suggested EMC control plan follows:

Title (specific to the project, mission, and hardware).
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Signatures Page.
Introduction.
Mission Description.
Applicable Hardware Descriptions.
Description of System Level EMC Requirements.
Description of Subsystem Level EMC Requirements.
Applicable and Reference Documents:
(a) EMC Standards and Specifications.
(b) Company Documents and Handbooks.
(c) Customer Documents, Drawings.
EMC Program Organization, Responsibilities, and Management.
Bonding Design Guidelines.
Grounding Design Processes and Guidelines.
Cable Harness Design Guidelines.
Shielding Design Guidelines.
PCB Design and Layout for Signal Integrity.
Power Design, Grounding, and Filtering.
EMC Analyses upon Identification of Critical Circuits (where applicable):
(a) Electronics Worst Case Analysis (EWCA).
(b) Interface Functional Failure Modes Effects and Criticality Analysis (IFFMECA).
(c) Interface Worst Case Timing Analysis (IWCTA).
(d) Radiator-Receiver Margin Analysis (R2MA).
Description of EMC Testing Requirements and Guidelines.
Requirements and Plans for Testing Heritage Hardware

Description of EMC Testing Processes.
Appendices.

IV. AVIONICS HARDWARE DEVELOPMENT PROCESS

It is important to now consider the usefulness of the EMC Control Plan for avionics hardware development in space system applications. The usefulness of the EMC Control Plan has been demonstrated, even further in this paper, through the inclusion of reliability and margin analyses as part the EMC Control Plan. This overall product development approach is illustrated in Fig.10. Fig.10 shows a space avionics hardware development cycle that is improved through the use of a new EMC Control Plan.

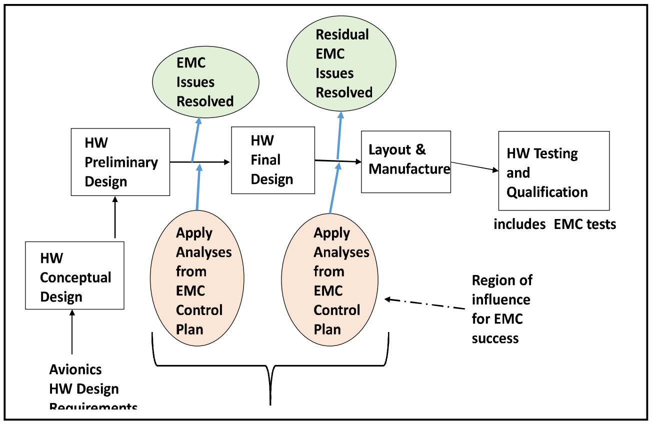

Fig. 10. Avionics hardware development cycle aided by an EMC Control Plan.

Fig. 10 shows the avionics hardware development processes practiced by most aerospace companies. Actually, these processes are also applicable in general to the development cycle of other electronics engineering hardware. Fig. 10 shows the implementation of the reliability and margin analyses within the product development cycle as part of the EMC Control Plan. Fig. 10 also shows that the application of this improved EMC Control Plan can contribute significantly to the successful preliminary and final designs of the hardware, which will include substantially reduced levels of EMI, a fact that will be demonstrated during acceptance EMC testing. Fig. 10 shows that there are two stages in the development cycle where the reliability and margin analyses in the EMC Control Plan should be applied. The analyses should be applied after the preliminary design and after the final design, before the manufacturing cycle begins. Therefore, it is in these two phases where EMI problems are more likely to be identified and removed before final EMC testing.

V. CONCLUSION

An EMC Control Plan for avionics hardware in space system is proposed that includes the performance of tailored reliability and margin analyses in critical circuits of the avionics hardware. The goal is to develop maximum flexibility in addressing potential EMI problems in avionics systems via a combination of testing methods and procedures with targeted reliability and margin analyses tailored to the critical circuits in the space avionics. This approach allows for the optimization of hardware design and development in space applications. The EMC Control Plan also becomes an integral part of the avionics hardware development cycle and allows for a great synergy between design engineers and EMC engineers.

REFERENCES

[1] NASA, General Environmental Verification Standard for GSFC Flight Programs and Projects, GSFC-STD-7000A, Section 2.5.1.6.1, 2013.

[2] Perez, R. "*Steps in the Proper Development of an EMC Control Plan*," International Symposium of Electromagnetic Compatibility, Minneapolis, MN August 19-23, 2002.

[3] "*EMC Test and Control Plan*," Appendix B. *EMC for Product Designs, Meeting the European EMC Directive*, Elsevier, pages 213-218, 1992.

[4] Payne, William F, McGowan, John J. "*The First Step to a Successful EMC System: Develop an Initial Energy Management Plan*" Energy Management System and Control Handbook, pages 21-44, Springer, 1988.

[5] *EMC Control Plan CP121 Tracker Horizontal Stabilizer Fatigue Stress Spectrum Survey Installation*, Grumman Aircraft Eng. Corp. 1986.

The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.