Technology Trends in Failure Analysis

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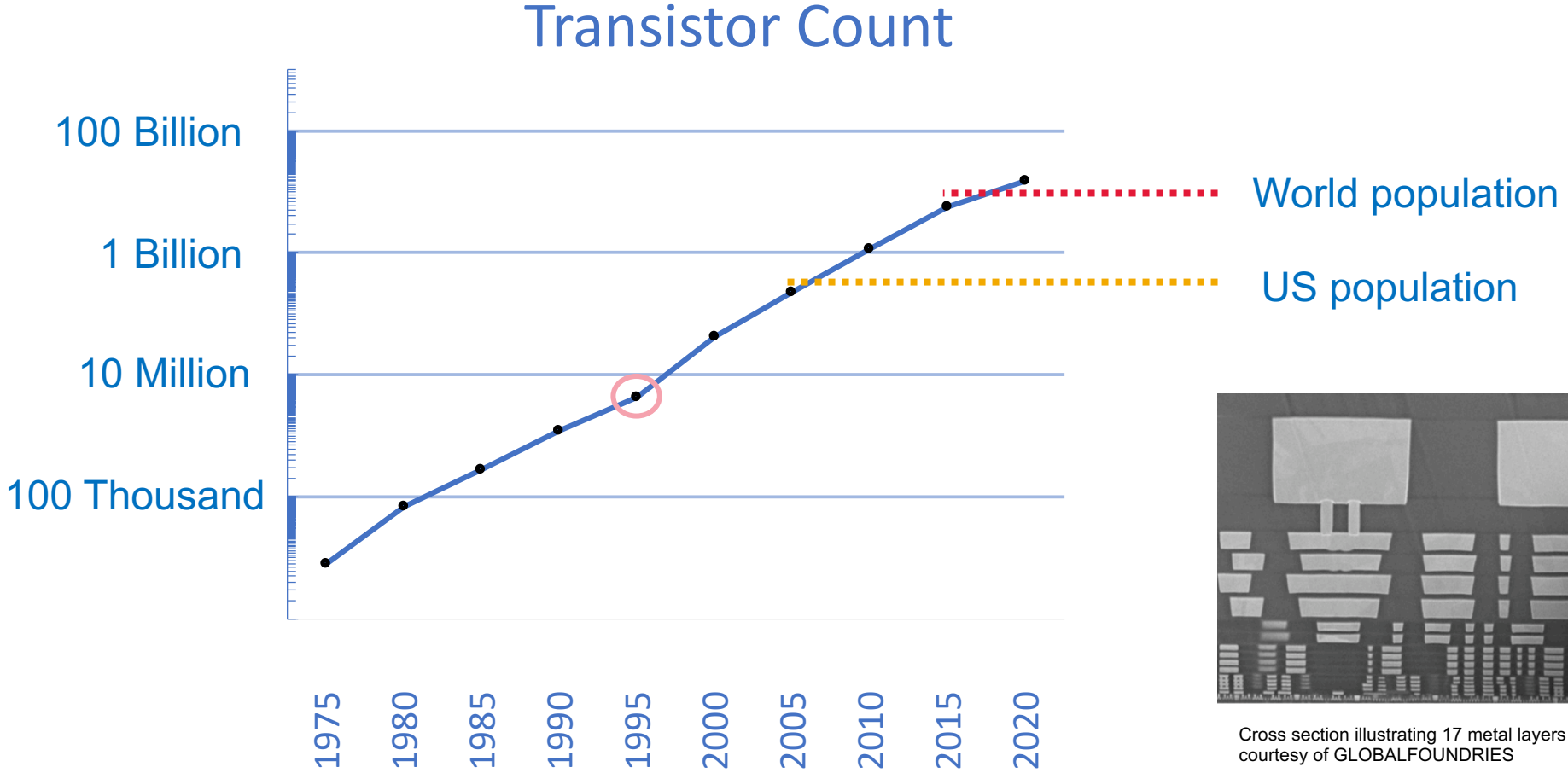
Failure Analysis Flashback: *1995 Alarm*

- Increasing IC complexity
  - ~4 million transistors, 5 metal layers
  - Smaller feature & defect sizes
  - Larger die size - ~200mm^2
  - Increasing pin / IO / power supply count
  - Reduced operating voltage, increased frequency
- New packaging technologies
  - Flip chip
  - Multichip modules (MCM)
  - Smaller package profiles
- Industry changes needing attention
  - FA transitioning to value added process
    - R&D, investment
  - CAD navigation linked with FA equipment
  - Tester based fault isolation

- 2019
  - ~10+ billion, 17 metal layers
  - ✓
  - Larger die size - ~800mm^2
  - ✓
  - ✓
- 3D packaging
  - ✓
  - ✓
- Reduction in R&D
  - US Loss of capability / access
  - ✓
  - ✓

Reference: Failure Analysis: Status and Future Trends, Sandia National Laboratories 1995



Cross section illustrating 17 metal layers
courtesy of GLOBALFOUNDRIES

Increasing complexity & scale increases FA challenges

>100's of billion single point failure locations <40nm in size

Microcircuit Failure Analysis Example: 14nm

Failure Characterization

Test Engineering
- Special Engineering Program
- Enable unique FA related support
- Shmoo timing, voltage, frequency
- Identify boundary / recovery conditions for soft defect isolation

Fixturing
- Custom wafer prober interface
- Package device with cooling
- 3-6 months lead time

Diagnostics

Logic
- Physical routing aware simulations identify failure scenarios matching test results
- Identify & score high probability candidate nets for analysis
- Net layout ported to CAD NAV

Memory
- Bitmap Processing
- Statistical correlations & overlay to FAB defect maps
- Ported to CAD NAV files to enable localization on FA tools

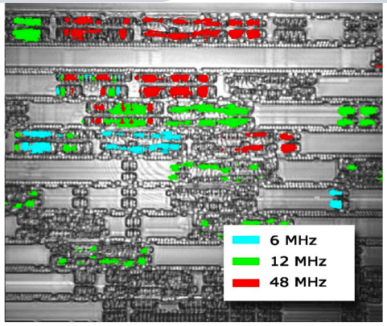
Global Fault Isolation

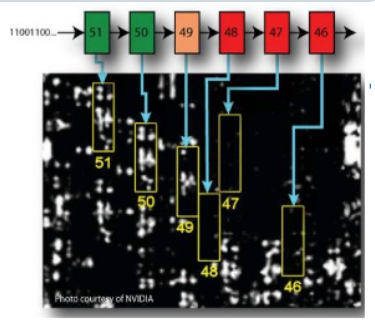
Static
- Lock-in IR (shorts)
- 1340nm Laser (obirch, XIVA, etc)
- MCT Photoemission (<500mv)

Dynamic (tester driven)
- Laser Voltage Imaging
- Laser Voltage Probing
- Soft Defect Localization
- Time resolved Photo Emission

Waferscan Dynamic Failure Isolation system image courtesy of Thermo Fisher Scientific

Failed Logic Diagnostic CAD image courtesy of Synopsys





Backside Laser Voltage Imaging (frequency mapping) images highlighting active flip flops courtesy of Thermo Fisher Scientific / Nvidia

Microcircuit Failure Analysis Example: 14nm

Intermediary Isolation

Sample Preparation
- Chemical Mechanical Planarization delayering system, removes M15-M5,
- Layer by layer artifact free deprocessing

Logic
- SEM nanoprobing / Electron Beam Absorbed Current Imaging (EBAC)
- Conductive Atomic Force Probe
- Layer by layer SEM inspection w/ passive voltage contrast analysis

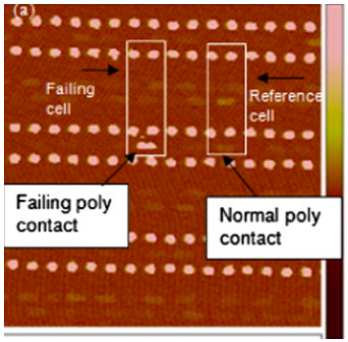
Memory
- SEM Nanoprobing within bit cell
- Conductive Atomic Force Probe
- Passive voltage contrast

Defect Capture

Sample Preparation
- Focused Ion Beam (FIB) surface defect alignment markings using CAD navigation
- Low kV FIB slice and view, 1-4nm slices capturing 100's of e-beam photos
- Layout analysis to determine appropriate Transmission Electron Microscopy (TEM) sample axis
- Conversion to TEM lamella (15-50nm thick)

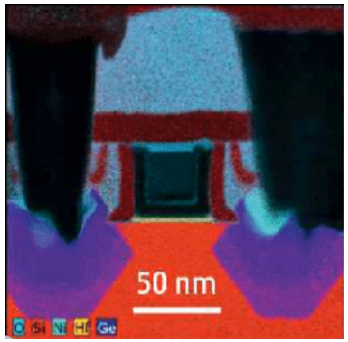
Material Characterization

TEM
- Replaces bulk of SEM work
- Special processes to create damage free15nm thick lamella
- Super EDX TEM imaging
- Visualized maps enable visualization of defect by material



Conductive Atomic Force Microscopy Image highlighting defective contact location courtesy of Advanced Micro Devices, Singapore, Microelectronics Reliability Volume 51

Focused Ion Beam image illustrating TEM Lamella sample ready for liftout courtesy of Fibics Incorporated



TEM EDX mapping of gate last transistor courtesy of D. Klenov, Thermo Fisher Scientific

2.5D & 3D Packaging example

Failure Characterization

Challenges

- Multiple die with shared power planes – Unknown which die contains failure
- Diagnostics solutions needed with test patterns linking die, package and predicting failed nets.
- Design for FA considerations needed to provide greater detail to FA community

Fault Isolation

Shorts

- Lock-In Thermography capable of identifying low power shorts
- Magnetic current imaging techniques highly capable

Opens

- TDR resolution insufficient
- Electro-Optical Terahertz Pulsed Reflectometry (EOTPR) effective
- EBAC can be effective

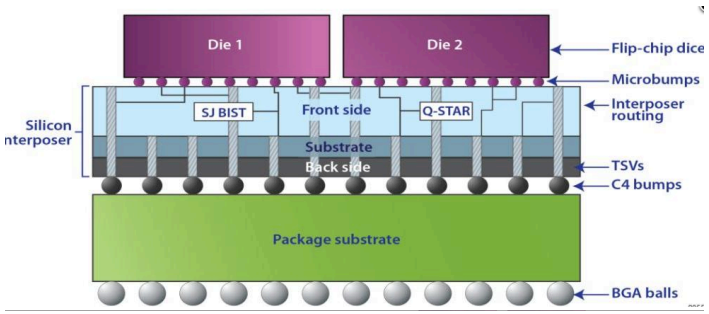
Physical Characterization

CT X-ray

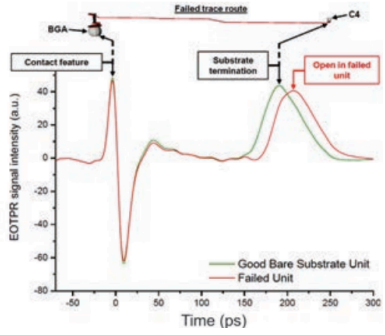
- Highly capable of visualizing many failures without need for cross sections.
- Can significantly reduce need for physical cross sections

Sample Prep

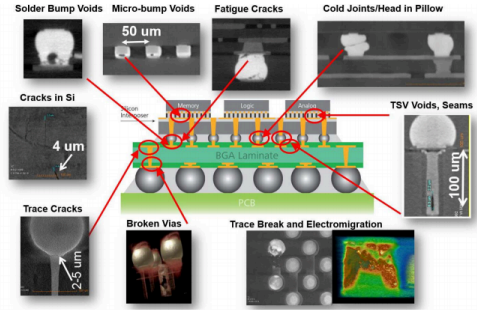
- Plasma FIB enables "Slice and view" cross sectioning through package due to high power
- Solutions to remove 1 of N die while maintaining function needed



Conceptual image of Built In Self Test (BIST) structures inserted in advanced packaging courtesy of Ridgetop Group Inc.



EOTPR image highlighting failed C4 bump location courtesy of C. Schmidt, GLOBALFOUNDRIES, TeraView Ltd.



CT X-ray collage illustrating typical failure modes in advanced packaging courtesy of C. Schmidt

A few comments:

- Bleeding edge Photoemission requires MCT
- New Failure Analysis techniques needed to identify defects in GAAFET
- With Foundry model, many companies have reduced FA investment and rely on FA at Foundry
- Expertise and capability at Foundry assigned to largest customer in current ramp. Support will not be available to end user
- FA knowledge and capability decreasing in US

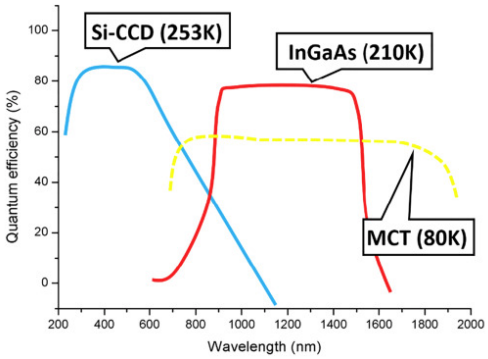
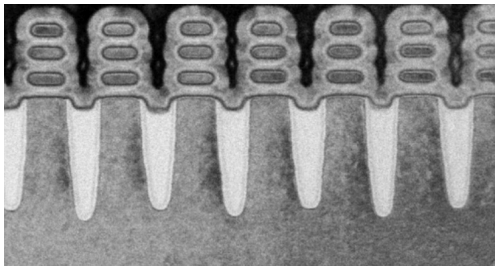
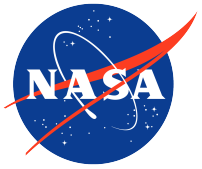


Image illustrating typical photoemission camera performance courtesy of J.C.H. Phang, IPFA 2005



TEM cross section of 5nm GAAFETs courtesy of IBM, Samsung and GLOBALFOUNDRIES

Image illustrating reduced industry footprint courtesy of Wikichip



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