A Common Platform for DSN Receiver Development

Andre Jongeling
Jet Propulsion Laboratory,
California Institute of Technology
4800 Oak Grove Dr.
Pasadena, CA 91109
818-393-2404
Andre.Jongeling@jpl.nasa.gov

Robert Navarro
Jet Propulsion Laboratory,
California Institute of Technology
4800 Oak Grove Dr.
Pasadena, CA 91109
818-354-9807
Robert.Navarro@jpl.nasa.gov

Abstract— **NASA's Deep Space Network is currently updating a number of sub systems within the Signal Processing Centers at its Deep Space Communication Complexes in order to modernize aging equipment in the downlink receivers for telemetry, tracking, radio science, and radio astronomy. To reduce development costs and increase commonality among these traditionally custom-built receivers, the implementation team has developed a flexible architecture built primarily around commercial off-the-shelf hardware compliant with the Micro Telecommunications Computing Architecture (uTCA) specification and commercial high speed 10Gbit Ethernet switches. Custom firmware and software are being developed to perform the required signal processing functions needed to replace the legacy systems in a phased implementation approach which establishes a new digital Intermediate Frequency (IF) signal distribution system first, followed by implementations of various receiver functions as dictated by need. The first of these new receivers, the Open Loop Receiver, will come online in the Fall of 2018. A description of the new architecture, referred to as the "Common Platform", will be provided followed by an overview of the phased implementation approach and initial OLR performance results.**

TABLE OF CONTENTS

1. INTRODUCTION 1
2. THE COMMON PLATFORM SYSTEM 2
3. DIGITAL IF DISTRIBUTION 5
4. PHASED IMPLEMENTATION 6
5. CURRENT STATUS AND EARLY RESULTS 7
6. SUMMARY 7
ACKNOWLEDGEMENTS 7
REFERENCES 8

1. INTRODUCTION

The Deep Space Network (DSN) provides telecommunications and navigation services to NASA's deep space scientific missions by way of three communications complexes located near Madrid Spain, Canberra Australia and Goldstone California in the United States. Each of the complexes is composed of a number of large aperture antennas that transmit and receive signals to and from the spacecraft and a central Signal Processing Center (SPC) that supports the operation of the antennas. Figure 1 depicts a simplified block diagram of the systems that handle the received signals. RF signals are collected by the large aperture antennas where they are amplified and down converted to an analog Intermediate Frequency (IF) signal that is then sent to the SPC for further processing. The IF signals at the SPC enter a network of distribution amplifiers and IF switches that are used to feed IF signals to an array of signal processing systems that perform various functions. At present these functions include a high rate telemetry receiver, a low rate telemetry and tracking receiver, an IF signal arraying system, and three generations of open loop recorders that are used for Radio Science, Delta-Differential One Way Ranging (DOR) and various forms of Very Long Baseline Interferometry (VLBI) measurements.

The current configuration of signal processing equipment at the SPCs is the result of an evolution of the various systems over a number of years. While very capable, the current configuration is becoming more difficult to maintain due to obsolescence issues with various components and assemblies and is also reaching its capacity limits as the DSN has added new downlink bands and antennas to each of the complexes. To resolve these issues the DSN has undertaken a task to replace these systems with a uniform set of hardware that can be tailored with custom firmware and software to implement the various receiver functions needed in the SPCs. While in the past, the requirements of these systems have dictated the need for custom hardware, the current implementation is taking advantage of an architecture built primarily around commercial off-the-shelf (COTS) hardware compliant with the Micro Telecommunications Computing Architecture (uTCA) specification and commercial high speed 10Gbit Ethernet switches. Because the various receiver types share common commercial hardware, this new system became known as the 'Common Platform'.

The 'Common Platform' is being implemented and delivered into DSN operations in multiple phases. This reduces the complexity of each delivery and allows tailoring of the system from delivery to delivery as more experience is gained on its performance in operation. The first phase of this system is currently undergoing acceptance testing prior to becoming operational in the DSN complexes. This first

978-1-5386-6854-2/19/$31.00 ©2019 IEEE

phase provides the infrastructure for the Common Platform, a new digitization and digital IF signal distribution system and a set of chassis to perform signal processing functions required by the various receiver types. To make use of this new infrastructure, this first phase also implements a new Open Loop Receiver (OLR) capability that will replace the DSN's current Radio Science Receivers (RSRs), VLBI Science Receivers (VSRs) and Wideband VLBI Science Receivers (WVSRs).

DIS to support a maximum of thirty-six IF inputs per rack. Each rack also contains an IF Equipment Controller (IEC) that provides for monitor and control of the equipment in that rack, as well as a number of Frequency and Timing Distribution (FTD) amplifiers that provide a 10 MHz reference clock and a one pulse per second timing pulse to the IFD chassis in the rack. Finally, each rack contains a Monitor and Control Switch (MCS) which provides an isolated monitor and control network for the assemblies

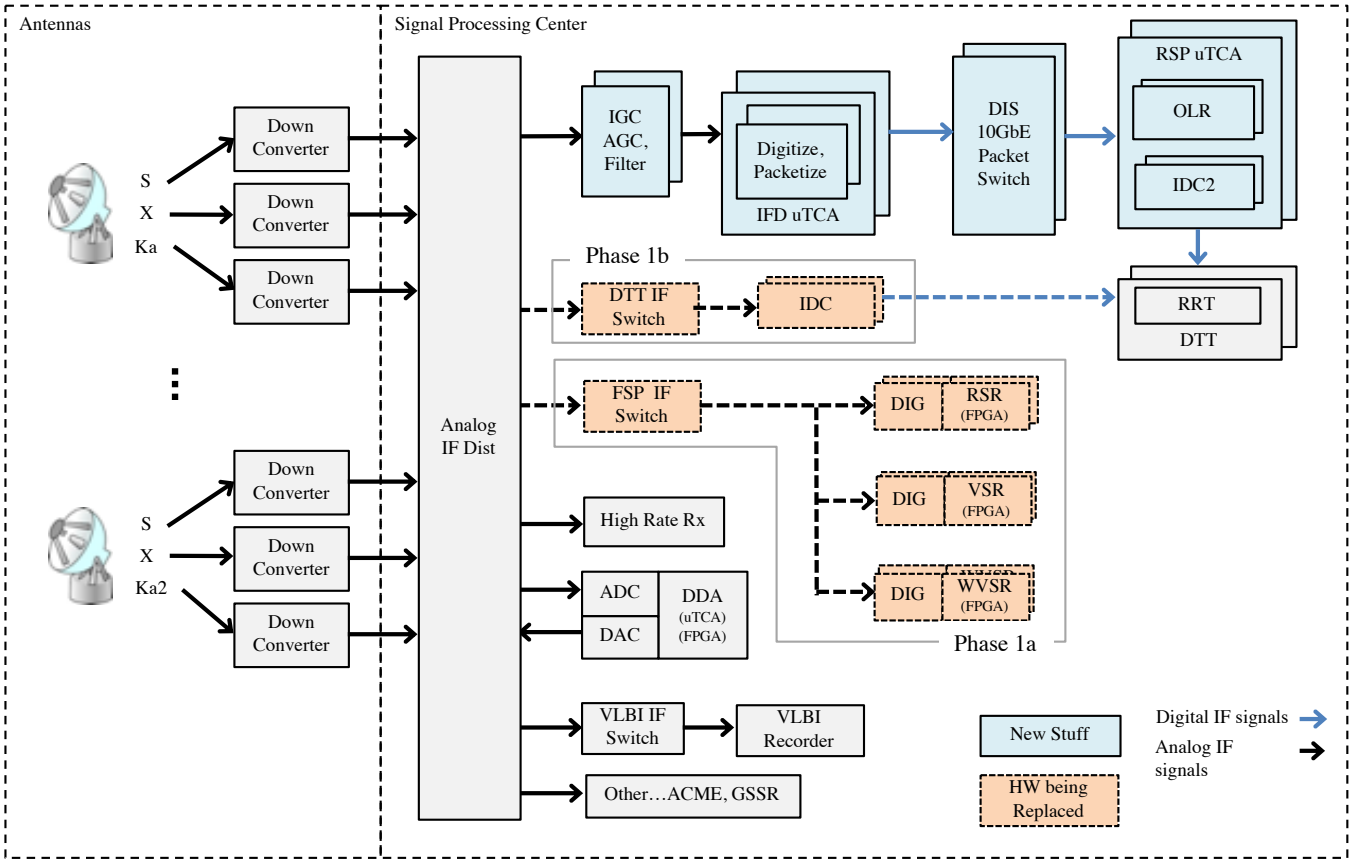

Figure 1. Simplified Block Diagram of Receiver Signal Processing within a DSN Complex

2. THE COMMON PLATFORM SYSTEM

A basic block diagram of the Common Platform system is depicted in the upper right corner of Figure 1. A number of IF Gain Control (IGC) chassis receive and process the analog IF signals preparing them for use by a number of IF Digitizer (IFD) chassis. The IFDs convert the analog IF signals into 10Gb Ethernet digital IF signal packet streams which are fed to the Digital IF Switch (DIS). The DIS is a COTS Ethernet switch that is used to distribute the digital IF packet streams to a number of Receiver Signal Processor (RSP) chassis. The RSP chassis perform real-time signal processing functions for various receivers.

The IGC and IFD chassis are arranged in pairs and can support up to twelve analog IF inputs. Up to three of these IGC / IFD pairs can be assembled into a rack along with a within the rack. Two racks are installed per complex with each rack supporting the same analog IF signals in order to provide redundancy.

The digital IF signals from the DIS in both racks are sent to a set of four RSP chassis that are hosted in racks of the current telemetry receiver systems. Since each RSP chassis has access to the digital IF signals from either DIS they can use either one to acquire the desired signal guarding against single point failures in the Common Platform system front end that could make an IF signal or the entire system unavailable. Similarly, the processing performed in the RSPs is intentionally distributed across four chassis to avoid a single point failure that would take all receivers offline.

IF Gain Control Chassis

Analog IF signals enter the Common Platform system at the IGC chassis. The IGC prepares the analog signals for sampling in the IFD chassis by both low pass filtering the signals (0-1.5GHz passband) and adjusting the analog signal levels (0-31.75 dB range) to an appropriate value for the analog-to-digital converters in the IFD. Each IGC chassis can support up to 12 analog signal channels and provides a monitor and control interface via a network connection to an internal single board computer. Each IGC also accepts a single analog IF test signal which each channel can select in lieu of its normal input for test purposes. The IGC was one of the few custom designed components of the overall Common Platform system. A block diagram of the IGC is depicted in Figure 2.

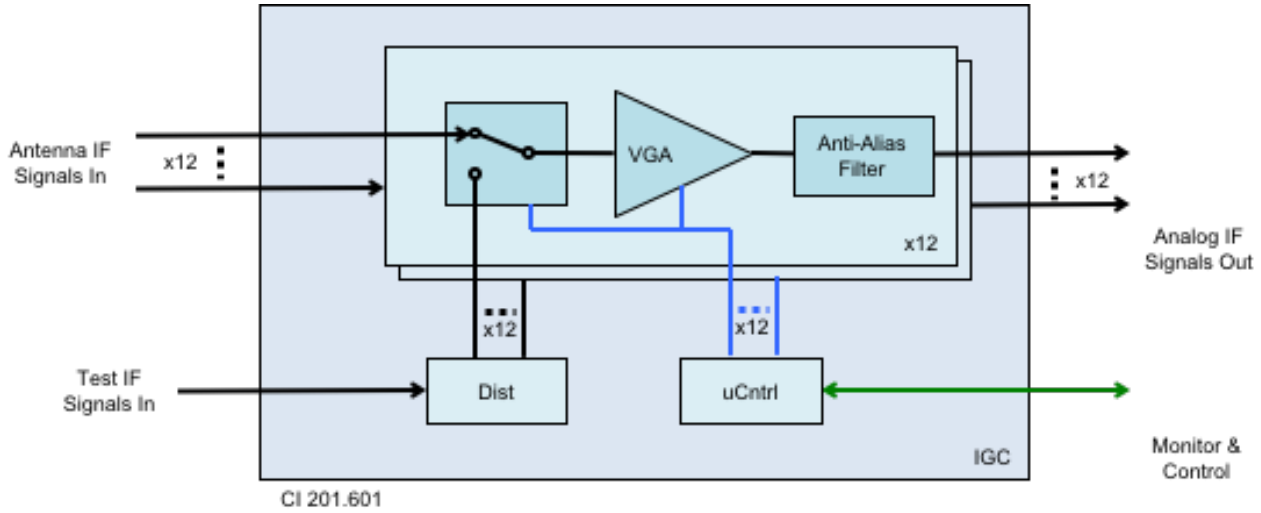

Figure 2. Block Diagram of IF Gain Control Chassis

uTCA Chassis

Two primary assemblies of the Common Platform system are built around a COTS uTCA chassis populated with a variety of COTS uTCA cards. These are the IF Digitizer (IFD) and the Receiver Signal Processor (RSP). A wide array of uTCA chassis and cards are available as COTS equipment. And while the uTCA specification is mature, many of the implementations of this specification are relatively new. As a result, a goal of the Common Platform team was to design a system that could be implemented with hardware from a single vendor to avoid potential compatibility issues. A number of providers were evaluated and, in the end, a uTCA chassis and a variety of cards from Vadatech were selected.

The uTCA architecture provides a very capable and flexible system allowing it to be adapted to a wide variety applications. The architecture is basically designed around Field Programmable Gate Arrays used together with a wide range of interface cards and a high-speed serial communications infrastructure. The Common Platform system makes use of the Vadatech VT866 uTCA chassis as the base for implementing the IFD and RSP assemblies. The chassis supports up to 12 Advanced Mezzanine Cards (AMCs) and 2 MicroTCA Carrier Hub (MCH) cards. When fitted with the 2 MCH cards the chassis provide dual 10Gb Ethernet connections and dual 1Gb Ethernet connections to each AMC, allowing for the flow of both high-speed digital data and monitor and control traffic between the AMCs and the MCH cards. Each MCH cards also supports dual 10Gb and 1Gb Ethernet ports on their front panels allowing for some external interconnections.

IF Digitizer

Using a uTCA chassis configured with an array of high-speed analog-to-digital converters and high-speed Field Programmable Gate Arrays an IF signal Digitization (IFD) system has been assembled that receives and converts all of the IF signals at an SPC into a new digital IF signal format that is carried on commercial 10Gb Ethernet equipment. The IF Digitizer (IFD) chassis performs a number of functions. It first samples the analog IF signals (3.2GHz sample clock) then processes the digital data with a discrete Fourier transform filter bank to divide the signal into a number of adjacent frequency channels (6.25MHz per channel). The channel data is then encapsulated in an Ethernet packet structure and transmitted to the Digital IF Switch via a 10Gb Ethernet interface. The IFD chassis are configured to handle 12 IF signals so that they paired easily with the IGC chassis. A block diagram of the IFD is depicted in Figure 3. The IFDs are implemented with a Vadatech VT866 uTCA chassis configured with 2 UTC002 MCH cards, 6 AMC516 FPGA cards fitted with AMC226 dual ADC daughter cards, and 4 AMC215 dual Small Form Pluggable Plus (SFP+) interface cards. Each AMC516 card in the IFD chassis converts 2 analog IF signals into 2 digital IF signals and is paired with an AMC215 card or UTC002 MCH card to provide the pair of 10Gb Ethernet interfaces needed for its digital IF output.

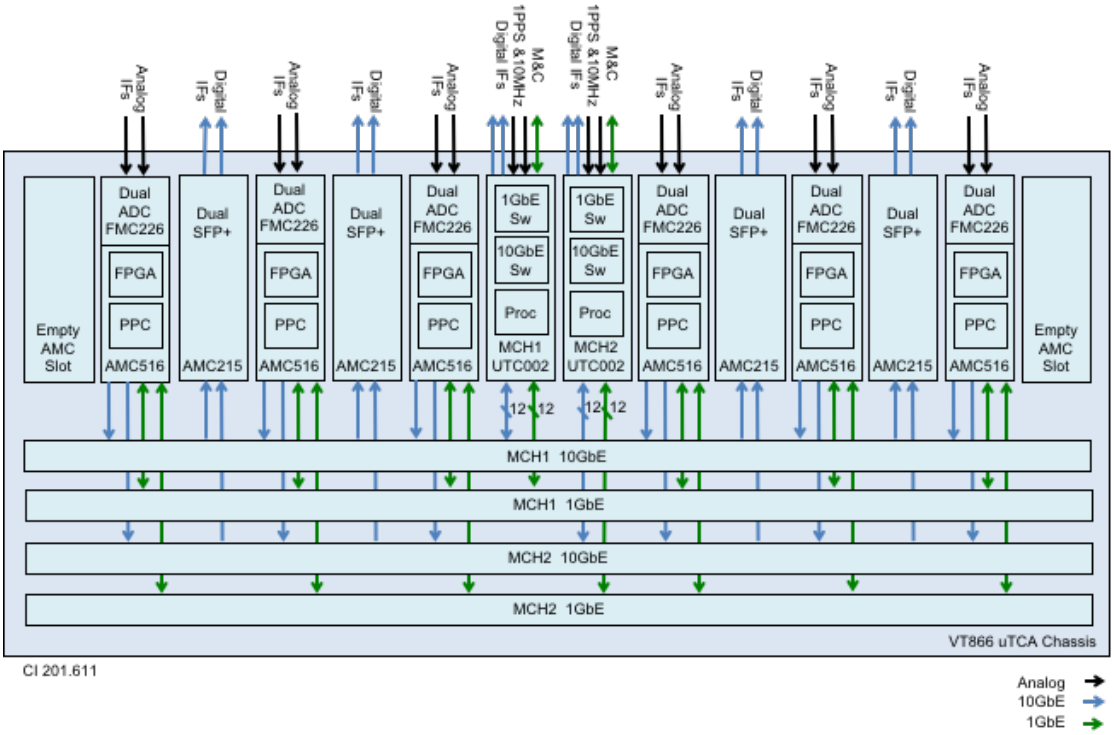

Figure 3. Block Diagram of IF Digitizer Chassis

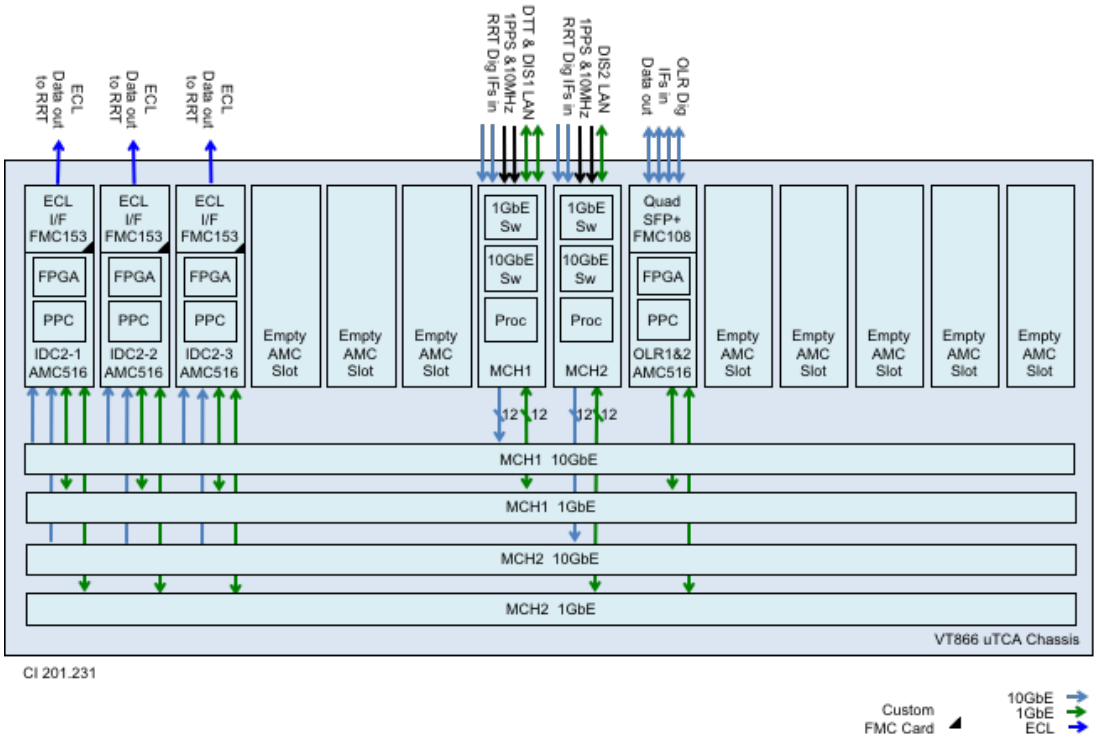

Figure 4. Block Diagram of Receiver Signal Processor Chassis

Digital IF Switch

The signals from the IFD are fed to a commercial 10Gb Ethernet switch that acts as a Digital IF Switch (DIS). The DIS performs the same function as its analog equivalent in the legacy systems. It allows each downstream receiver connected to it, to select which IF signal it works with. However, while previous systems required expensive custom assemblies to meet stringent DSN isolation requirements the DIS is implemented with a standard 10Gb Ethernet switch. A Cisco Nexus 56128 was selected for the Common Platform system as it met the wire rate transfer requirements needed to properly handle the 10Gb Ethernet digital IF signals, provided enough ports to allow for reasonable system growth in the future (up to 36 IF inputs and 20 receivers) and was also being used elsewhere in the DSN, allowing for spare components to be shared between systems.

Receiver Signal Processor

The digital IF signals selected by the DIS are fed into the Receiver Signal Processing (RSP) chassis. The RSP chassis provides the real-time signal processing resources needed by the various receivers implemented in the Common Platform system. Each RSP consists of a Vadatech VT866 uTCA chassis configured with a single AMC516 FPGA card fitted with an FMC108 quad SFP+ daughter card for Open Loop Receiver (OLR) processing and up to six AMC516 FPGA cards fitted with FMC153 Emitter Coupled Logic (ECL) interface daughter cards to provide interfaces to existing low rate telemetry receiver signal processing systems. A block diagram of the RSP is depicted in Figure 4.

The RSP AMC516 FPGA cards performing OLR functions each provide real-time signal processing functions for 2 receivers. These cards are referred to as ORX cards. For each receiver, digital IF data is received via one of the 10Gb Ethernet interfaces on the ORX card's FMC108 quad SFP+ daughter card and is processed by up to 16 OLR channels implemented in the FPGA. Each of the 16 OLR channels can select its own digital IF input and selects and down converts a portion of its selected digital IF signal spectrum to baseband. The baseband data is then sent back out the 10Gb Ethernet interface for recording on an associated OLR server.

As stated above, the RSP AMC516 cards implementing interfaces to the existing low rate telemetry and tracking receivers are fitted with FMC153 ECL interface cards. These cards are referred to as IDC2 cards as they provide a replacement for the legacy IF to Digital Convertor (IDC) chassis used in the low rate receivers. The FMC153 daughter cards were custom designed by Vadatech to JPL's specifications and provide a convenient interface point to the legacy low rate receivers. Each IDC2 card receives digital IF data across the VT866 10Gb Ethernet backplane from one of the 10Gb Ethernet interfaces built into the MCH cards. Multiple IDC2 cards share the MCH 10Gb Ethernet interfaces so that all IDC2 cards can receive digital IF data in parallel. The use of the IDC2 cards was a compromise that allowed the legacy low rate receivers to make use of the new digital IF distribution system without having to port the full functionality of the low rate receiver signal processing into the new RSP chassis. This port however is planned for a future implementation.

3. DIGITAL IF SIGNAL DISTRIBUTION

Previous DSN receiver systems used analog distribution amplifiers and switches to make copies of the IF signals and route them to the various types and instances of downlink receivers. When the previous systems were implemented, commercial equipment did not readily meet the requirements for high isolation and as a result custom equipment was designed. The Digital IF signal switching provided by the Common Platform system avoids this problem and has other advantages as well, including lower hardware costs, and higher flexibility. Commercial 10Gb Ethernet switches are relatively inexpensive compared to custom designed analog IF switches and more easily expanded to meet future needs.

In designing a digital IF distribution system, some guiding principals were followed. First, the digitized data needed to be processed and formatted so it could be transmitted over one data link or, if not over one data link, formatted so that it could be easily split between multiple links. Second, the processing in the front-end digitization assembly needed to be simple, but flexible enough to support the needs of the various receivers it would support. If done properly this would avoid having to support numerous different modes to satisfy downstream users of the digital IF signals. Third, we wanted to take advantage of the signal processing capabilities in the front end to lessen the load on the downstream units. And fourth, we knew some of the downstream receivers only required access to portions of the IF signal, so it was desirable to send those units only a subset of the full IF bandwidth.

For the digital IF distribution system, leveraging off of popular commercial standards provided many advantages. These advantages include high availability, costs falling over time, and support from multiple vendors. For the required IF bandwidth of 500 MHz, 10Gb Ethernet links and switches provide enough network bandwidth to fit each IF signal over a single link and the technology is relatively mature and readily available.

Three options were considered for transmitting the digital IF signal data from the front-end digitizers in the IFD to the receivers in the RSP backend. In the first, the sample data for the entire IF signal bandwidth is transported over the link. The main advantage of this choice is simplicity in the front end, requiring minimal processing and only one mode of operation. However, assuming at least 8-bit samples and a desired 100 to 600 MHz IF band, this option would require more than one 10 Gb Ethernet link per IF signal. This in turn, would increase the complexity of the digital IF signal links as a method to manage the flow across the two links would be required. Alternatively, the data could quantized to less than 8 bits before sending over the link. But, then, dynamic range

is sacrificed. Finally, some flexibility is lost with this option since every downstream receiver must accept the full IF sampling band. Also, this choice uses the most network bandwidth for an Ethernet switch.

In the second option, multiple smaller sub-bands of variable bandwidth would be sent on demand over the link. This choice would require some processing to break the data up into smaller sub-bands, but that processing is straightforward. In this option, receivers that did not require the full bandwidth could request just the needed portion, but once the total 10Gb Ethernet capacity was filled by signals requested by different receivers, no other requests could be made unless they were for a sub-band already being provided. This would limit flexibility and potentially make the system difficult to manage.

In the third option, a fixed set of smaller sub-bands of a constant bandwidth are sent over the data links. Downstream receivers would request the sub-bands they need for their desired signal and then reconstruct the signal to the full desired bandwidth upon reception at the receiver. While this option does require some additional processing in the downstream receivers it solves the problems inherent in the first two options and is also highly flexible and easy to manage both at the digitization front-end and the back-end receiver.

For the Common Platform system, the third option was selected and a system to break the IF signals up into multiple fixed sub-bands was implemented in the IFD. The IFD analog to digital converters (ADCs) sample at 3.2 GS/s capturing the IF signals from roughly 0 to 1.5GHz. A first stage digital filter and down converter in the ADC chips on the IFD selects a bandwidth from 0 to 800MHz for further processing. This 800MHz signal is fed into an FPGA which implements a Modified Discrete Fourier Transform Filter bank (MDFT) which breaks the IF input signal into 128 sub-bands. The MDFT is a critically sampled filter bank that allows for near perfect reconstruction. [1] The critically sampled property provides for optimal use of limited data bandwidth resources. For the first delivery of the Common Platform all IF signals have a bandwidth from about 100 to 600MHz so only the 84 the sub-bands overlapping this region are actually sent over the 10Gb Ethernet link. This requires a serial link bandwidth of 8.4 Gbits/sec for each digital IF signal with 8-bit complex samples.

In the back end, RSP receivers will access only the sub-channels they need to perform their required processing. For both the OLR and IDC2 receiver types, up to 16 sub-bands are accessed and fed into an MDFT synthesis filter bank to reconstruct 100MHz signals which are then further processed by the OLR or IDC2. The sub-band selection feature also provides another stage of digital down conversion for downstream open and closed loop receivers.

Internet Group Management Protocol

The Digital IF signals generated by the IFD, carried by the DIS, and received by the RSP are transferred via the use of the one-to-many Internet Group Management Protocol (IGMP). The Ethernet packets of each IFD digital IF signal sub-band are assigned a unique address. When an AMC card in one of the RSP chassis wants to receive the data for a given digital IF signal sub-band it issues an IGMP join request on its 10Gb Ethernet interface specifying the unique address of the digital IF signal it desires. The DIS is running an IGMP snoop process that detects the join request from the RSP and starts the flow of the specified digital IF signal. Similarly, an AMC card in the RSPs can stop the flow of a digital IF signal by issuing an IGMP leave request. In this way the IFDs send out only one copy of the 84 sub-bands for each IF input signal and the DIS handles making extra copies for each RSP receiver using its own internal buffering.

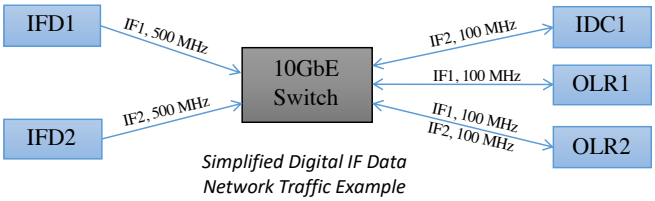

Figure 5. Digital IF Distribution Example

Figure 5 shows a simple example of the digital IF distribution system with two IF data sources and three back end receivers. Each IF data source produces 500 MHz of bandwidth, two of receivers subscribe to 100 MHz of bandwidth and the third subscribes to 100 MHz of bandwidth from IF1 and 100 MHz of bandwidth from IF2.

4. PHASED IMPLEMENTATION

As stated earlier the Common Platform system is being delivered as a phased implementation. The first phase, which is currently under acceptance testing, delivers the digitization and digital IF distribution functions which form the core of the Common Platform infrastructure. In addition, the first phase is also delivering a set of 4 RSP chassis that are hosting ORX cards to implement a new Open Loop Receiver capability that will be used to verify the performance of the Common Platform's front end and will also replace aging RSR, VSR, and WVSR receivers at the DSN SPCs.

Two additional deliveries are already under development for the Common Platform system. An IDC2 function for the RSP is currently under development. With this delivery the IDC chassis in the current low rate telemetry receivers will be replaced with an AMC card in the RSP chassis. These AMC cards will be fitted with a parallel ECL output daughter card to provide an interface to the low rate receivers existing signal processing chassis. In this way the Common Platform will act as a new 'digitizer' for the current low rate receivers

and give them access to all of the IF signals supported by the common platform system. This implementation removes the aging IDC assemblies from the low rate receivers and also replaces the aging analog IF selector switches used by the low rate receivers solving two primary maintenance issues of the DSN SPCs.

The second additional delivery of the Common Platform system currently under development, adds a high rate receiver capability that will replace the RT Logic high rate receivers currently fielded at the DSN SPCs. These receivers are no longer readily supported by RT Logic and have begun to suffer failures, prompting a desire to replace them. For this delivery, additional AMC cards will be installed into the existing RSP chassis. Each card will implement the real-time signal processing for one high rate receiver. This implementation requires only additional COTS hardware. The firmware and software for the high rate receiver is being developed at JPL which will allow the performance and capabilities of the high rate receiver to be tailored as needed in the future. The design for the new high rate receiver is based heavily on work done for a previous project for a Reconfigurable Wideband Ground Receiver. [2]

While no other additional functionality for the Common Platform system is currently under development, the system has been designed to accommodate growth in the future. Looking again at the block diagram in Figure 1 we can see a few obvious candidates. These include the IF signal arraying system, the wideband VLBI recorders and the Antenna Calibration and Metrology (ACME) systems.

5. Current Status and Early Results

As of this writing, all of the hardware for the first delivery of the Common Platform system has been assembled, tested, and installed in the DSN SPCs as well as the DSN test facility. The hardware installations at the DSN SPCs and test facility have been validated and the final acceptance tests of the operational firmware and software is underway. Numerous 'shadow tracks' have been completed for Radio Science, Delta DOR and Time and Earth Motion Precision Observations (TEMPO) VLBI activities. Various issues have been identified and corrected as a result of these shadow tracks helping to significantly mature the system prior to its going operational. The OLRs have been used to record standard System Performance Test (SPT) data in parallel with the legacy RSR, VSR and WVSRs at each of the DSN SPCs and are showing comparable results for Allan Variance and phase noise, two of the key performance metrics required for Radio Science. The data obtained for the Delta DOR and TEMPO VLBI shadow tracks have also been processed and again compare favorably with the data taken with the legacy system. Figures 6 and 7 depict comparisons of the OLR and legacy RSR from one of the shadow tracks observing a carrier signal from the Mars Express for both residual frequency and measured signal to noise ratio. As can be seen, when properly configured the OLR and the Common Platform system produce results that are virtually identical to the legacy RSR.

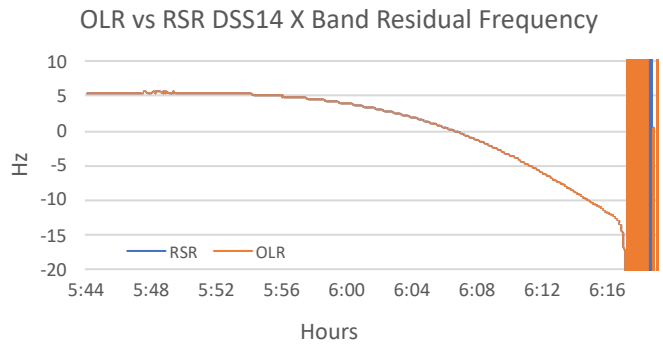

Figure 6. OLR vs RSR Residual Frequency

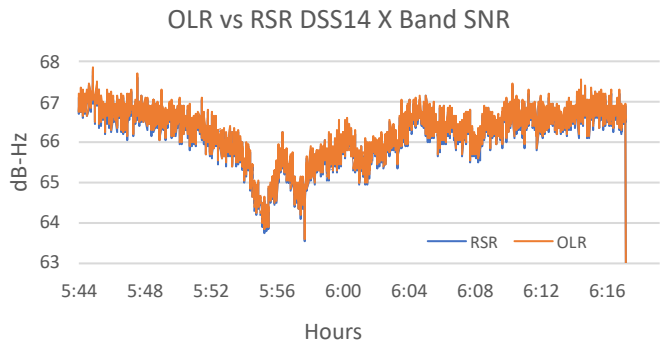

Figure 7. OLR vs RSR Signal to Noise Ratio

6. Summary

An overview of the Common Platform system has been presented along with details of some of the assemblies required to implement it. The phased implementation approach and some of its advantages have been presented. And finally, a brief status of the current installation and test results has been provided. If early results are any indication, the Common Platform system should provide years of reliable service for the DSN. In addition, due to its inherent flexibility, it will provide a cost-effective approach to adapt signal processing in the DSN SPCs to meet changing requirements.

Acknowledgements

The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. The authors thank the DSN Project Office and NASA for supporting this development effort. Also, they would like to express their gratitude to all of the members of the Common Platform development and test teams both at the Jet Propulsion Laboratory and Peraton. And finally, to the engineers and management of Vadatech who have been generous in their time in helping to adapt and configure their hardware to meet the demands of the Common Platform system.

REFERENCES

[1]Tanja Karp and N. J. Fliege, "Modified DFT Filterbanks with Perfect Reconstruction", IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 46, No. 11, November 1999

[2] Kenneth S. Andrews, Arby Argueta, Norman E. Lay, Mark Lyubarev, Elliott H. Sigman, Meera Srinivasan, and Andre Tkacenko, "Reconfigurable Wideband Ground Receiver Hardware Description and Laboratory Performance," IPN PR 42-180, pp. 1-22, February 15, 2010.

BIOGRAPHY

Andre Jongeling *joined JPL in 1991 where he is currently the Deputy Manager of the Communications Ground Systems Section and the System Engineer for the Common Platform development project. Previously he has been both an engineer and supervisor for JPL's Processor Systems Development Group. Andre has been involved in the development of a number of advanced systems for use in the DSN in the fields of Radio Science, Radio Astronomy, VLBI, and Antenna Arraying.*

Robert Navarro *received a B.S in Engineering from Harvey Mudd College in 1986 and a M.S. in Electrical Engineering in 1987. He is currently the Manager of the DSN's Telemetry Tracking and Command End-To-End Data Services Office. He has worked on DSN ground systems for radio science and VLBI recording as well as correlators and antenna arrays as an engineer and a manager. His career started with Hewlett Packard working on circuit design and image processing for ink jet printers.*