

3D Technology Overview

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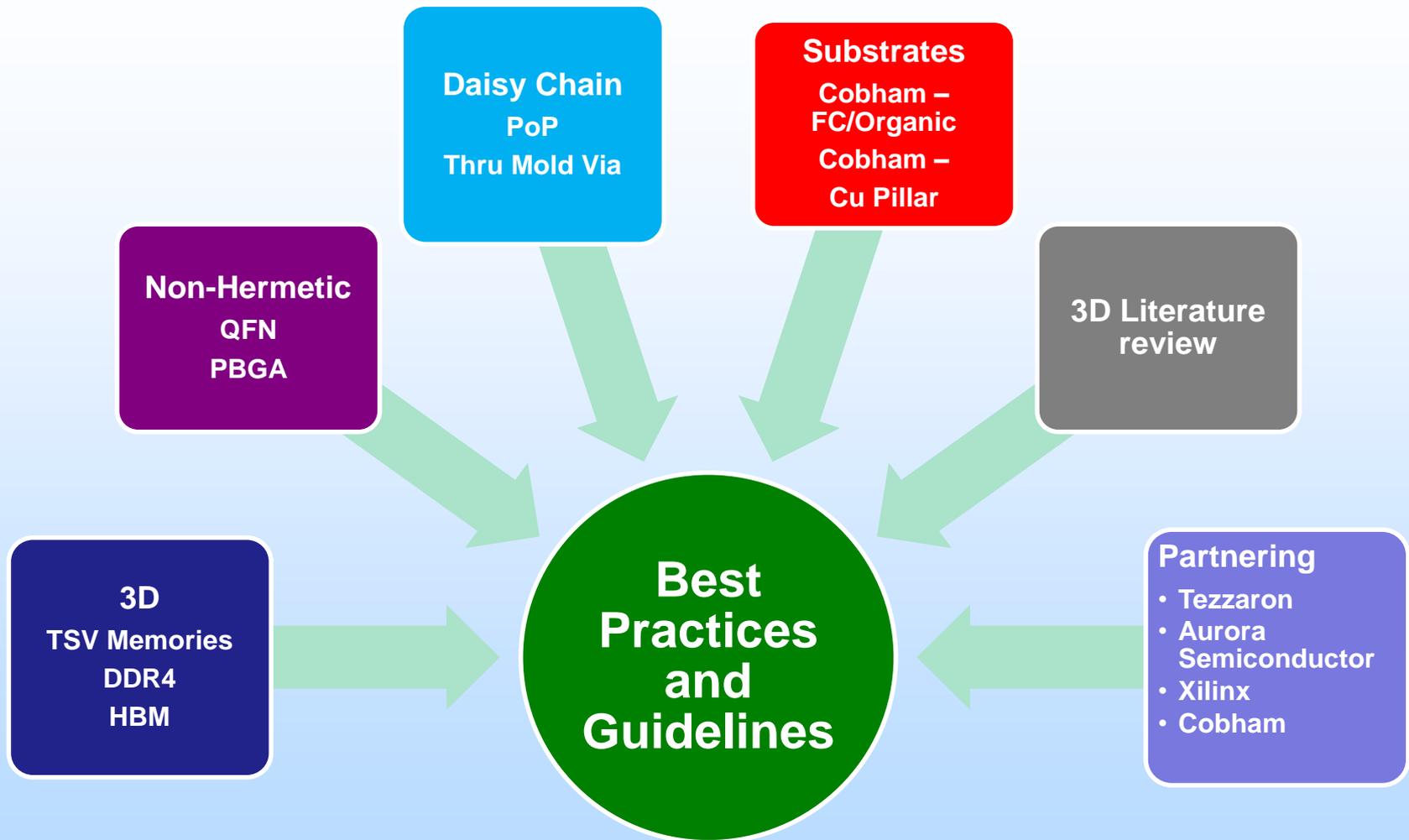
Acronyms

Acronym	Definition
3D	Three Dimensional
3DICs	3D Integrated Circuits
ADCs	Analog to Digital Converters
AF	Air Force
AFRL	Air Force Research Laboratory
AFSMC	Air Force Space and Missile Systems Center
BOK	Body of Knowledge
BYU	Brigham Young University
CIO	Chief Information Officer
CLTs	NASA CIO Leadership Teams
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf (COTS)
COTS	Commercial Off The Shelf
DACs	Digital-to-Analog Donverters
DC	Direct Current
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DIMM	Dual in-Line Memory Module
DiRAM	Dis-integrated Random Access Memory
DLA	Defense Logistics Agency
DMEA	Defense MicroElectronics Activity
DoD	Department of Defense
DOE	Department of Energy
EEE	Electrical, Electronic, and Electromechanical
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GCR	Galactic Cosmic Ray
GIDEP	Government-Industry Data Exchange Program
GPU	Graphics Processing Unit
HiREV	High Reliability Virtual Electronics Center
IC	Integrated Circuit
IUCF	Indiana University Cyclotron Facility
JEDEC	Joint Electron Device Engineering Council (JEDEC)
JFAC	Joint Federated Assurance Center

Acronym	Definition
LANL	Los Alamos National Laboratories
MBMA	Model-Based Missions Assurance
MDA	Missile Defense Agency
MPSOC	Multiprocessor System-on-Chip
NASA	National Aeronautics and Space Administration
Navy Crane	Naval Surface Warfare Center, Crane, Indiana
NEPAG	NASA EEE Parts Assurance Group
NEPP	NASA Electronic Parts and Packaging
NESC	NASA National Electric Safety Code
NRL	Naval Research Laboratory
NRO	United States Navy National Reconnaissance Office
NSWC Crane	Naval Surface Warfare Center, Crane Division
OCE	Office of the Chief Engineer
PCB	Printed Circuit Board
POL	point of load
PoP	Package on Package
R&M	Reliability and Maintainability
RH	Radiation Hardened
SAE	Society of Automotive Engineers (SAE)
SAPP	Space Asset Protection Program
SBIR	Small Business Innovation Research
SCRIPPS	SCRIPPS Proton Therapy Center
SEE	Single Event Effect
SiC	Silicon Carbide
SiC	Silicon Carbide
SiGe	Silicon-Germanium
SMDs	Selected Item Descriptions
SME	Small and Medium-sized Enterprises
SNL	Sandia National Laboratories
SOC	Systems on a Chip
STMD	NASA's Space Technology Mission Directorate
STMD	Space Technology Mission Directorate
TOR	Technical Operating Report
WLP	Wafer Level Packaging



NEPP – Packaging

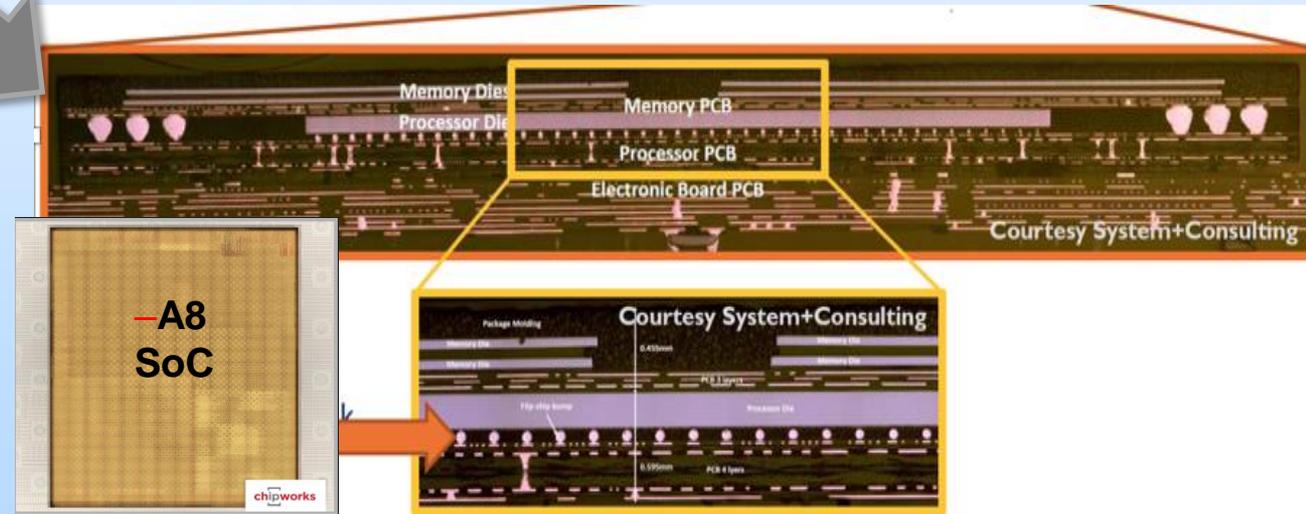




Evolution of IC Packaging

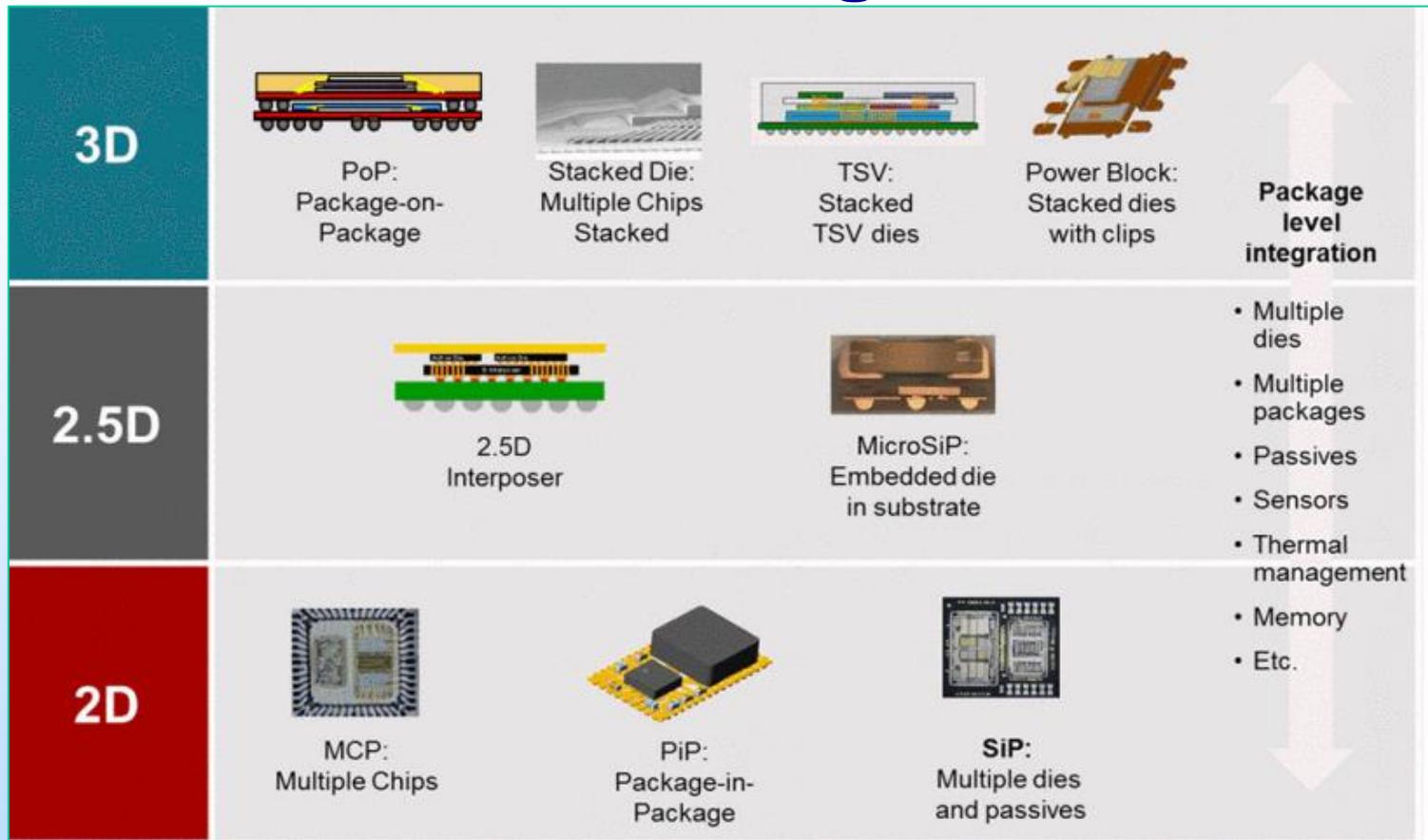


- IC packaging in the 1970's and 1980's was based on wire bonding silicon to a lead frame.
- External connections were along the periphery of the package
- Modern packaging uses multiple die stacked with various interconnection layers and bump using all available silicon area.





Dimensional Evolution of Packaging Technologies



- Packaging technologies have evolved in many different ways to meet demands of different market segments
- The trend throughout all of these is the need to add capabilities in the vertical dimension



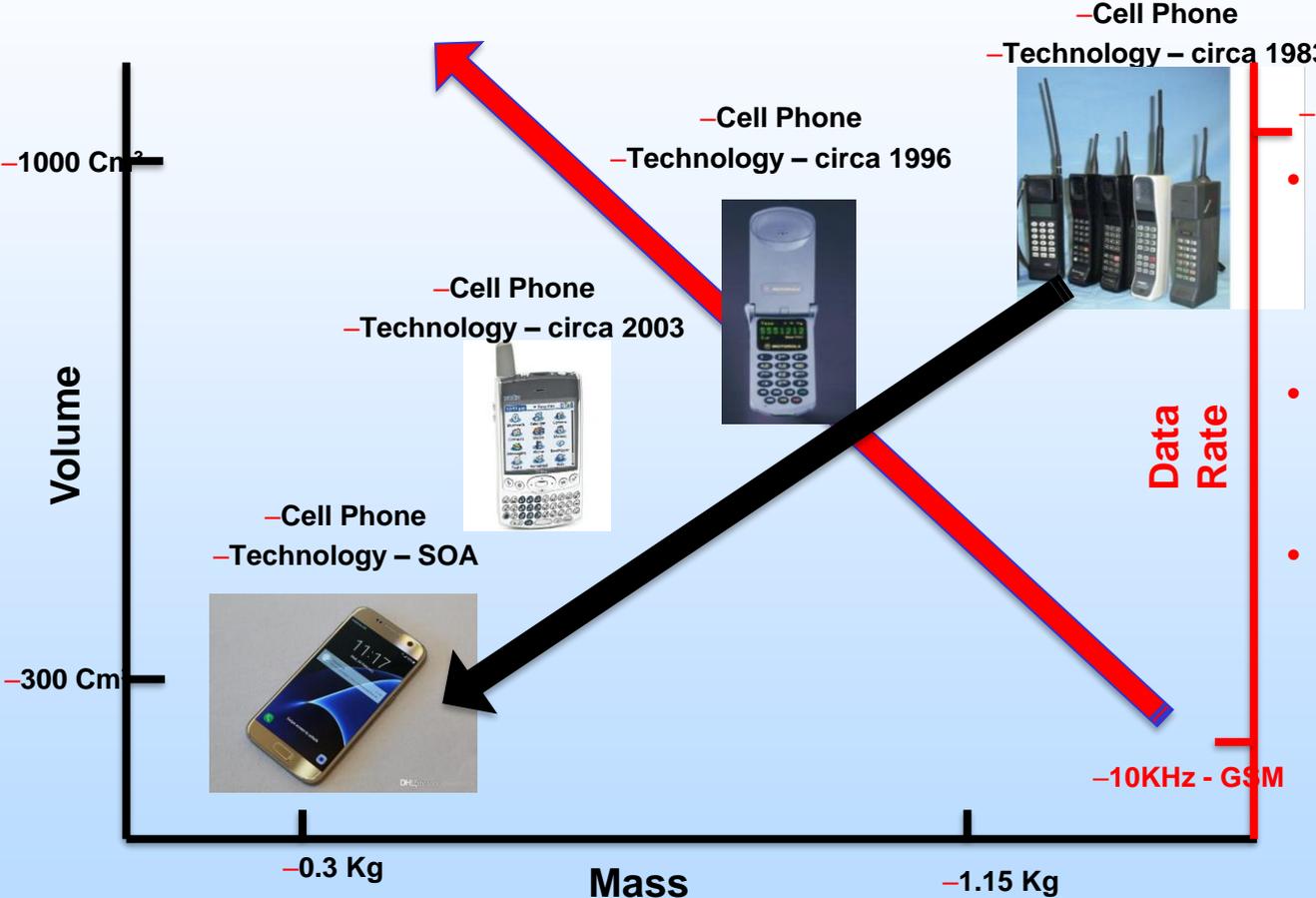
Packaging Technology is now very Market Specific

Category	Application	2013	2014	2015
Memory	Main Memory			
	Graphic Memory			
	Mobile Memory			
	SDRAM			
	Flash Memory	BOC/Mobile MCP(5Stack)/Nand MCP(6Stack)		PoP/FC Hybrid (TSV)/WL-CSP
System LSI	Logic IC	ASIC		
		ASSP		
	Appl.	PC		
		Mobile		
		Handheld	SIP(RF)/QFN (Multi-ROW)/MCM LGA/FC-CSP	
		Digital TV	SIP(6Stack)/E-QFP(MCP)/QFN/QFP All Body	SIP Hybrid/WL-CSP (Bumping)/Fan Out WLP
MEMS	MEMS			
	Bio	Microphone MEMS	MEMS (Pressure/Bio)	

- Memory requirements are for significant increases in density and throughput
- Logic requirements are for flexibility and multi-die access
- Different markets will have different reliability requirements
- ***This has to be foremost in mind when considering COTS 3D packages***



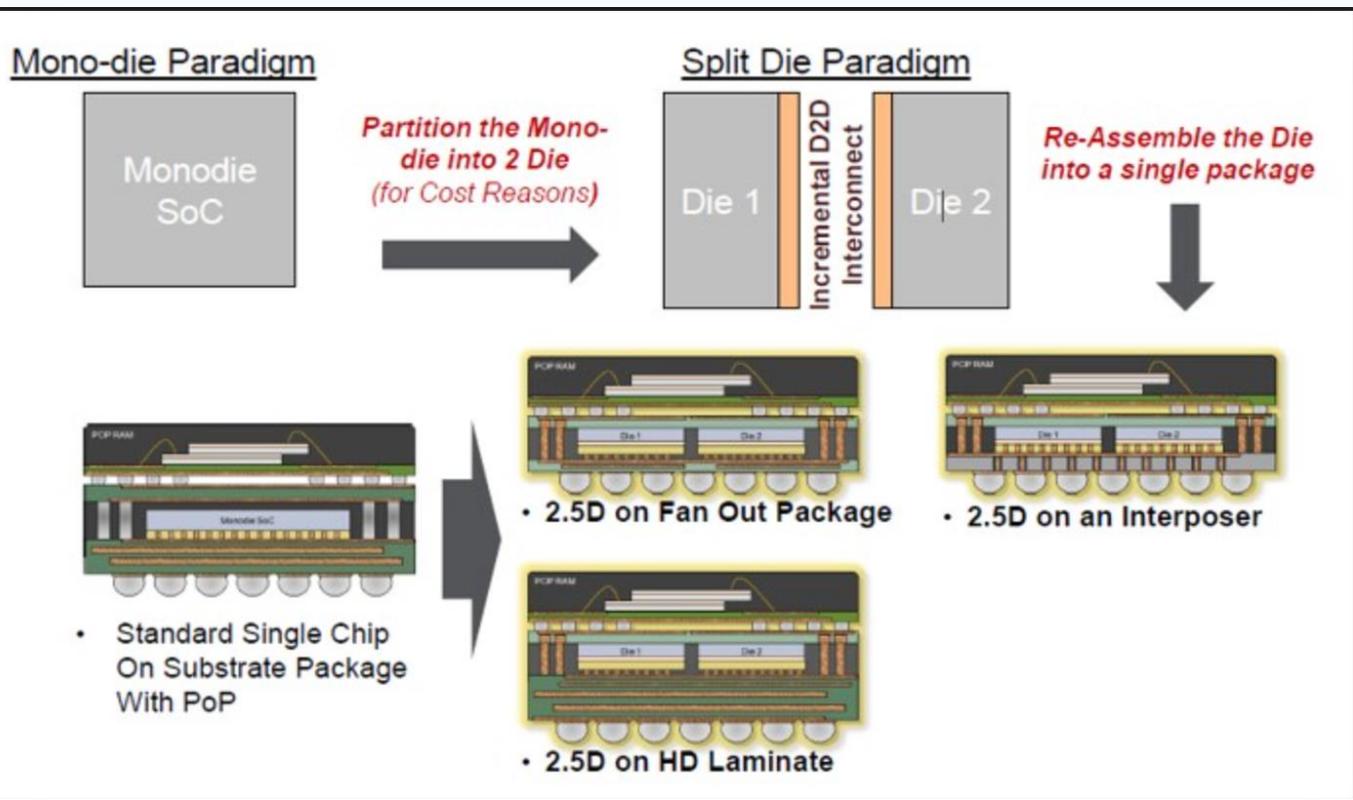
Cell Phones as a Packaging Technology Driver



- Many new packaging technologies are required to achieve improvements seen in cell phones
- Shrinking volume while vastly improving performance
- These include Package-on-Package (PoP), Through Silicon Via (TSV), and System in a Package (SiP).



Heterogeneous Die Packaging



- 2.5D/3D technologies can easily allow for integration of die of different technologies into a single package
- Cost of large die can now be reduced significantly by making smaller die and re-assembling in package.
- Transparent to end user



Evolution of the Substrate

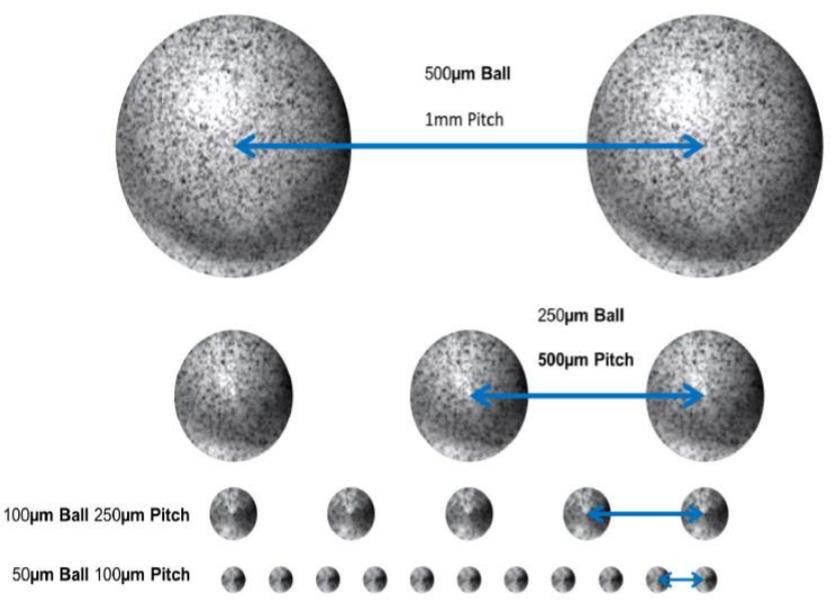
3D TECHNOLOGY LANDSCAPE					imec
wiring level	3D-SIC		3D-SOC		3D-IC
	Global	Semi-global	Intermediate	Local	FEOL
2-tier stack					
Contact Pitch	40 ⇒ 20 ⇒ 10 ⇒ 5 μm	5 ⇒ 1 μm	2 μm ⇒ 0.5 μm	200 ⇒ 100 nm	< 100 nm
Relative density:	$1/16 ⇒ 1/4 ⇒ 1 ⇒ 4$	4 ⇒ 100	50 ⇒ 400	5000 ⇒ 10000	> 10000
Partitioning	Die	blocks of standard cells		Gates	Transistors
		<p>Block-level partitioning</p> <p>Block size depends on R,C of the 3D interconnect structure</p>		<p>Partitioning/ placement → EDA problem</p>	<p>Standard cell design → device/cel l problem</p>

- As substrate technology evolves, it leverages wafer fab tools and materials
- It is natural for this to be provided by the wafer foundry are FEOL (Front End of Line)



Bump Size Scaling

Relative Solder Sphere Size and Pitch



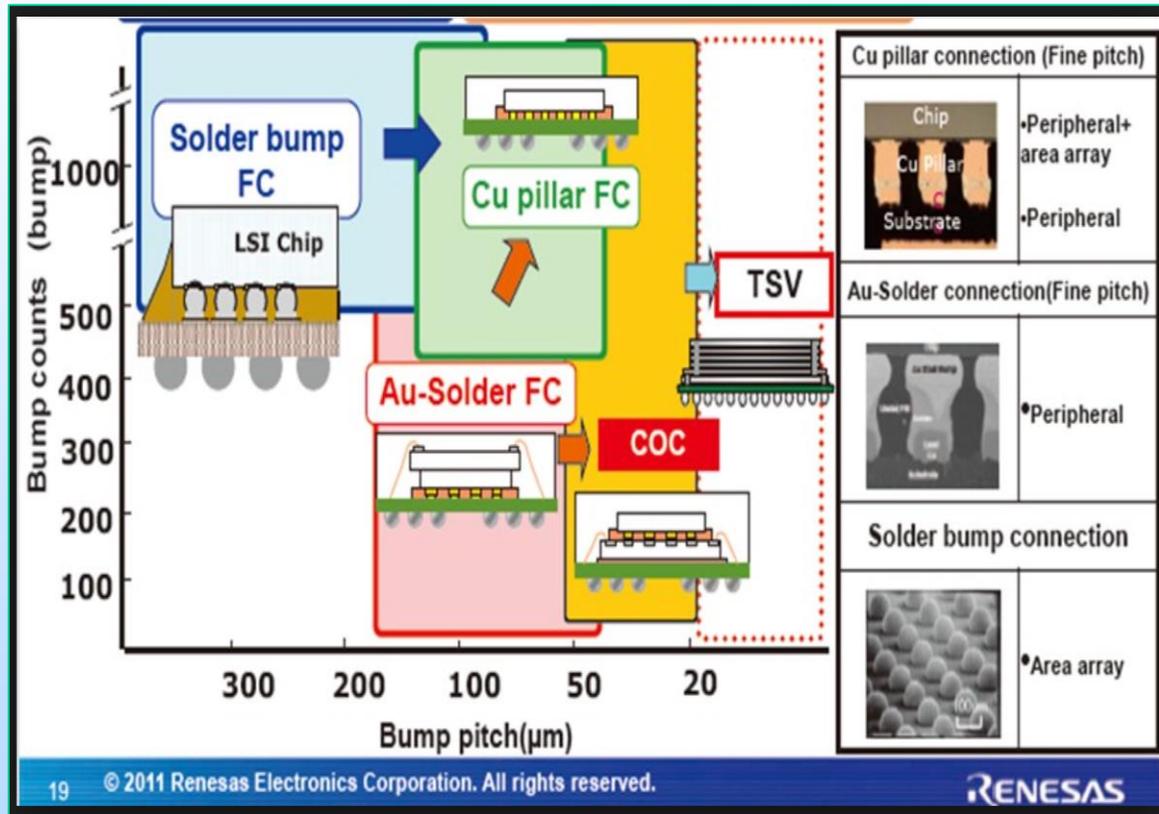
- Ability to make millions of bumps with a variety of materials properties and sizes is the new fundamental way to connection die to die and die to packages
- What are risks of not having ppb Quality levels?

	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu μ -Pillar + Pb-free Cap
Structure				
Diameter	75 – 200 μ m	75 – 150 μ m	50 – 100 μ m	10 – 30 μ m





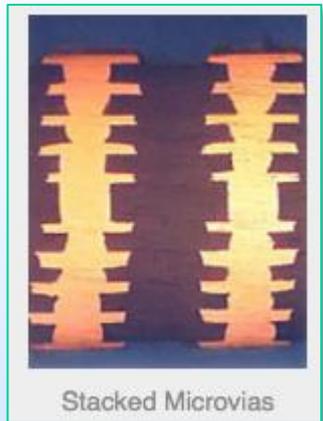
How Bumps are an Enabling 3D Technology



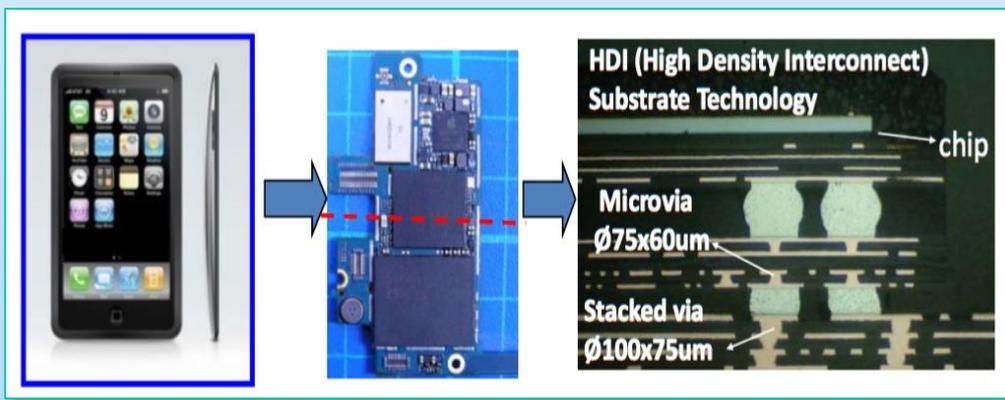
- As bump dimensions (both size and pitch) more and varied vertical technologies are enabled



High Density Interconnect Substrates - SiP



- HDI PCBs imply high-density attributes including laser microvias, fine lines and high performance thin materials.
- This increased density enables more functions per unit area.
- Possibility for custom solutions to NASA applications using heritage die

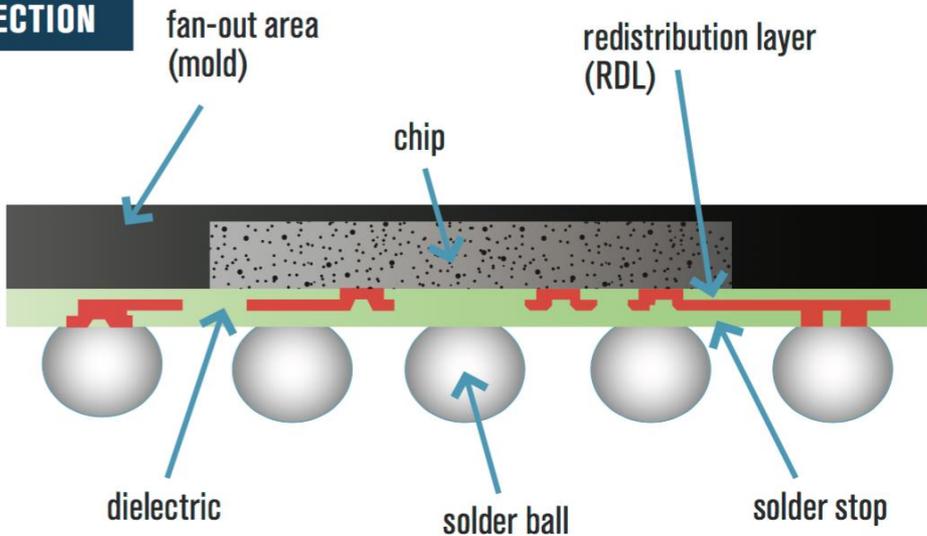




Fan Out - Wafer Level Package

A Simple Revolution

CROSS-SECTION



- Conventional WLP packages have I/O over IC area
- FOWLP embeds die in epoxy mold compound while allowing for additional I/O
- Use of Redistribution Layer (RDL) allows 10-20% reduction in thickness, speed increase and power dissipation and cost reduction
- Several different options
- Largest single growth technology in all of packaging
- \$200M -> \$2B

INTERCONNECT LEVEL	BGA	FCIP	eWLB
Resistance @ DC [mΩ]	76	7.5	3.2
Resistance @ 5Ghz [mΩ]	375	41	15
Inductance [nH]	1.100	0.052	0.018
PACKAGE LEVEL	BGA	FCIP	eWLB
Resistance @ DC [mΩ]	89	22	23
Resistance @ 5Ghz [mΩ]	629	248	91
Inductance [nH]	1.790	0.950	0.340



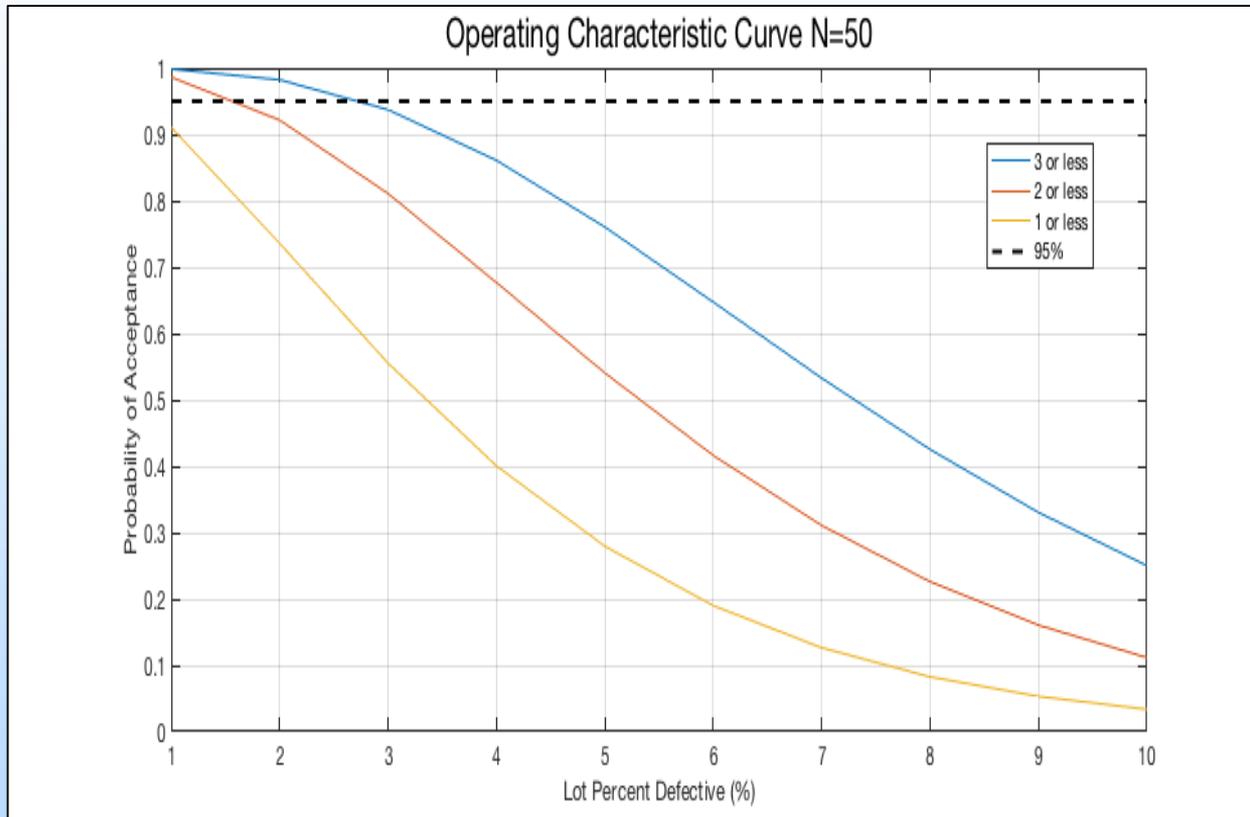
Best Practices issues

COTS 2.5/3D Packaging

- **Manufacturability**
 - Multiple, non-consecutive lot reliability data
 - Stability of process (Cpk data)
 - Root cause failure identification
 - How/why/when/where of burn in
- **Technology**
 - Known limitations
 - Package / board interactions
 - Wafer Level Reliability
- **System/Application**
 - Modes of operation
 - Original design goals
 - Temperature range
 - Susceptibility to variation in input conditions



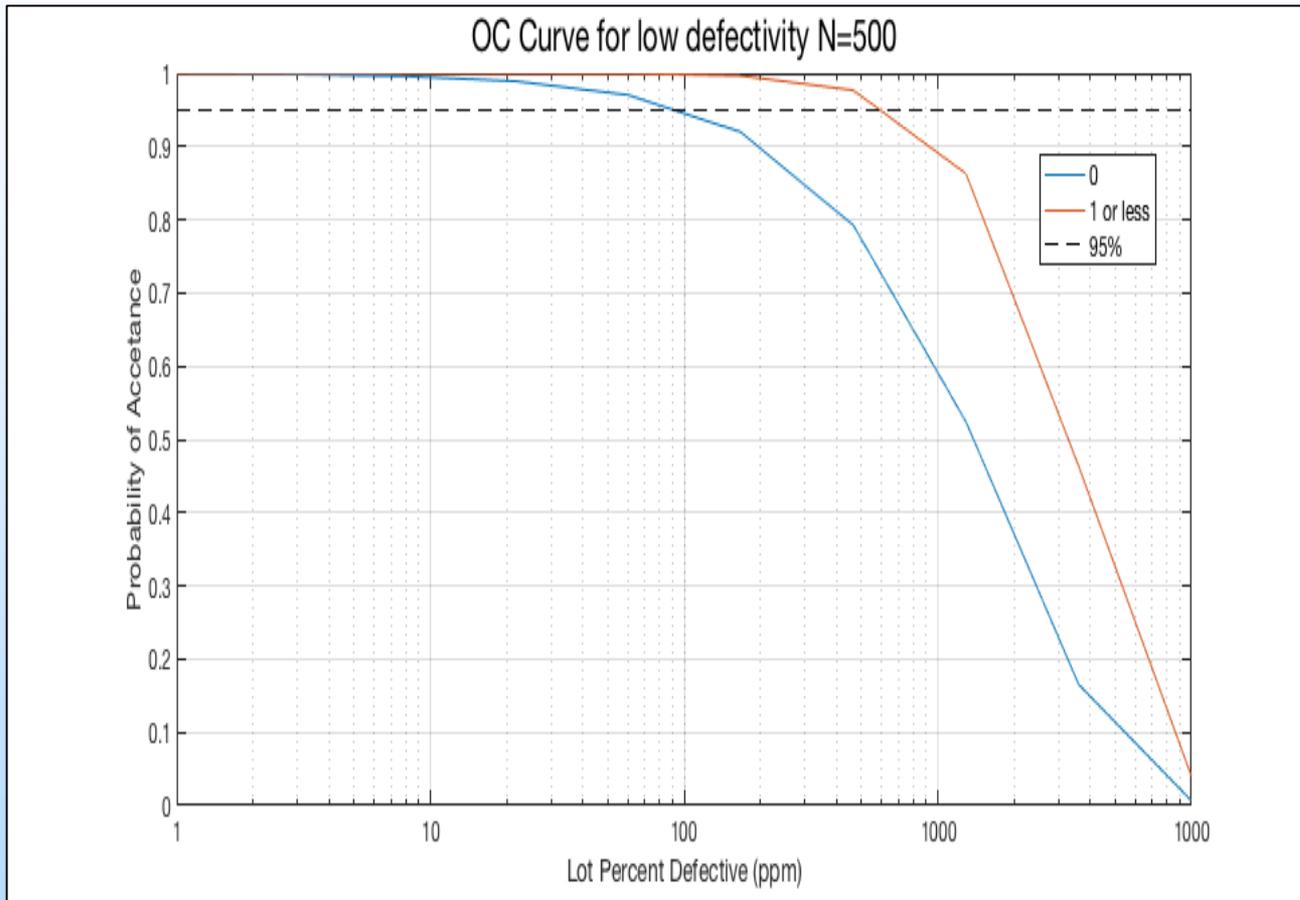
Operating Characteristic Curve



- Classical Reliability Analysis
- Type I error – rejection of a good lot
- Type II error – acceptance of a bad lot
- Example: 95% probability of accepting a lot with 2% defective if you have <3 failures out of 50 samples tested
- Useful with very high levels of defectivity (1%=10,000 ppm)



Operating Characteristic Curve II – ppm defect levels



- Even with 500 part samples, 0 failures does not ensure an ultra high reliability lot
- But it's a necessary condition
- Even 1 fail out of 500 samples means you might have a 95% chance of accepting a lot with 600ppm defectivity
- Need a more sophisticated approach

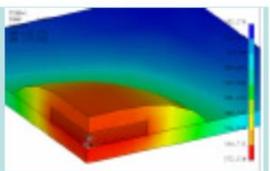


Reliability Concerns of 3D Technology

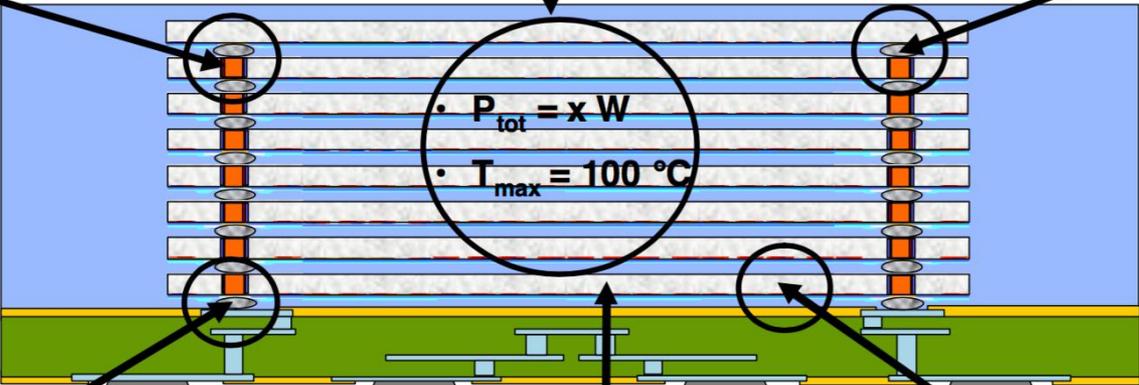
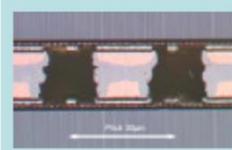
Thru-Silicon technology



Heat dissipation

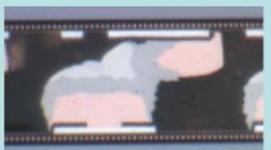


Interconnect μ Pitch Bumping



- $P_{tot} = x W$
- $T_{max} = 100\text{ }^{\circ}\text{C}$

Assembly Accuracy



Testing (e.g. KGD / e-Fuse)



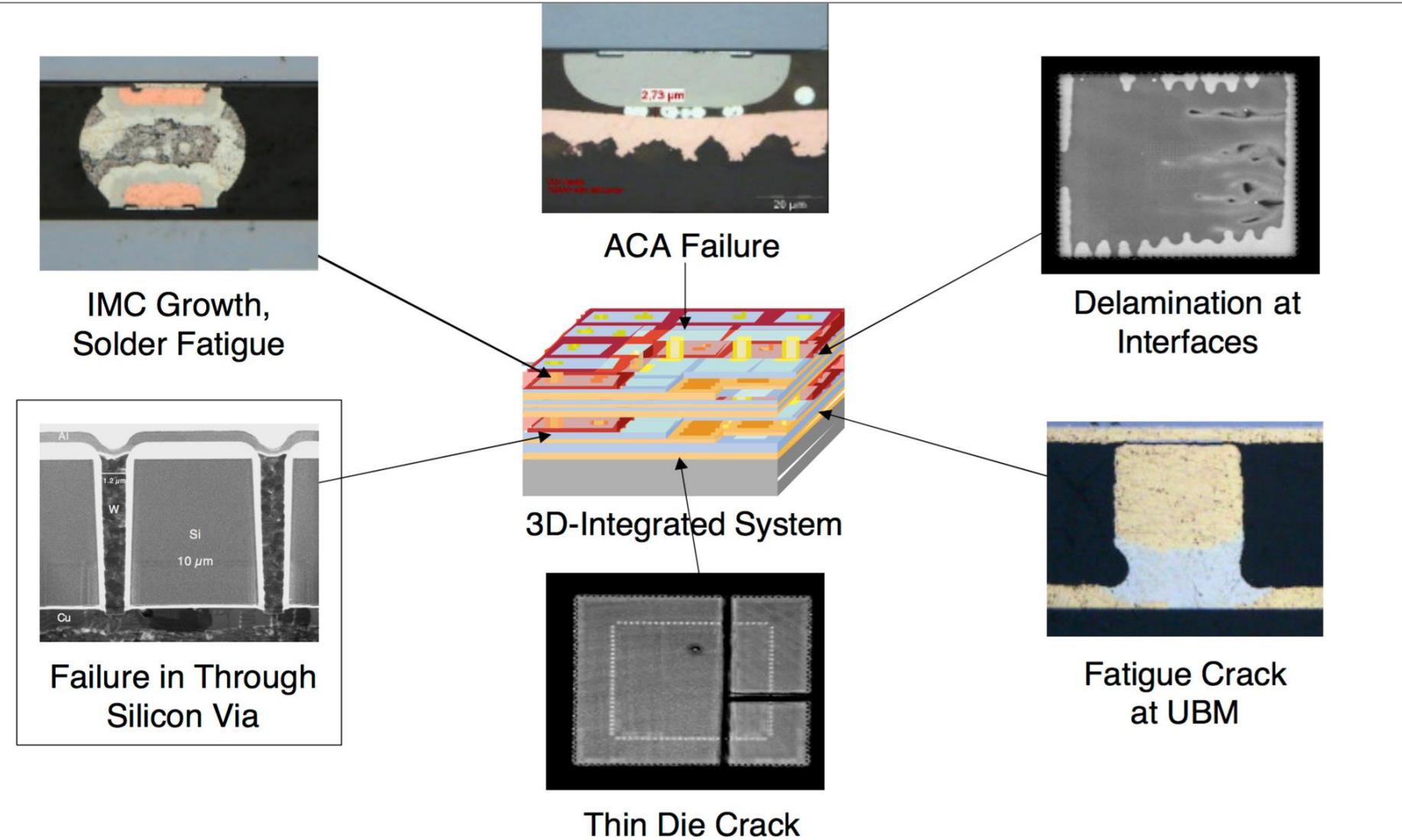
Thin Die

Reliability of 3D Technology - E. Kaufersch, B. Wunderle, D. Vogel, O. Wittler, R. Mrossko, B. Michel 2008

To be presented by Doug Sheldon at the 2017 NASA Electronics Parts and Packaging (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center, Greenbelt, MD, June 26-29, 2017.



Failure Mechanisms – 3D

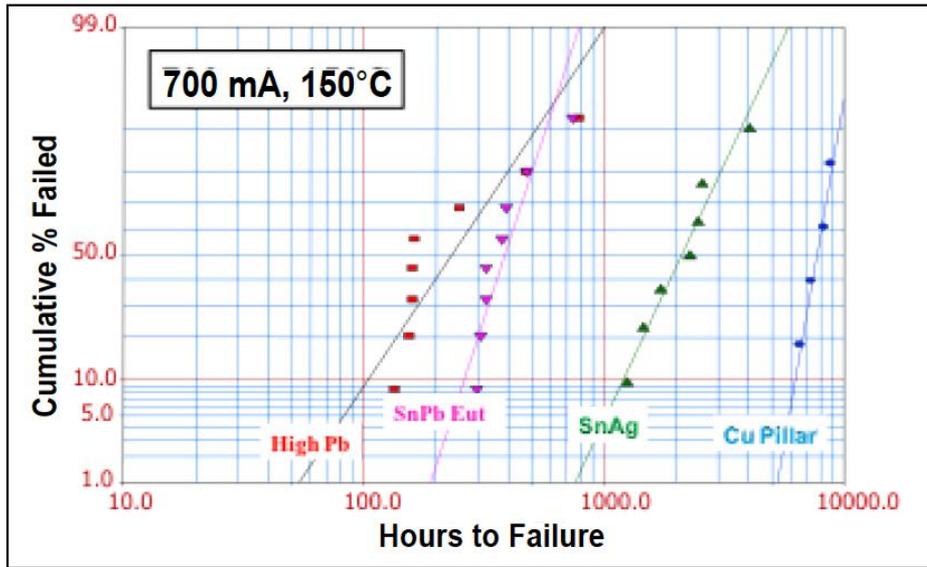


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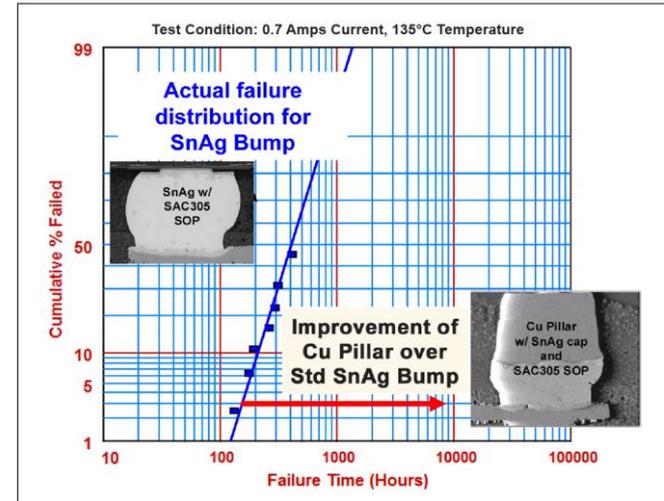
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Sample Industry Electromigration Results



Electromigration Reliability Comparison of Cu Pillar with SnAg Bump



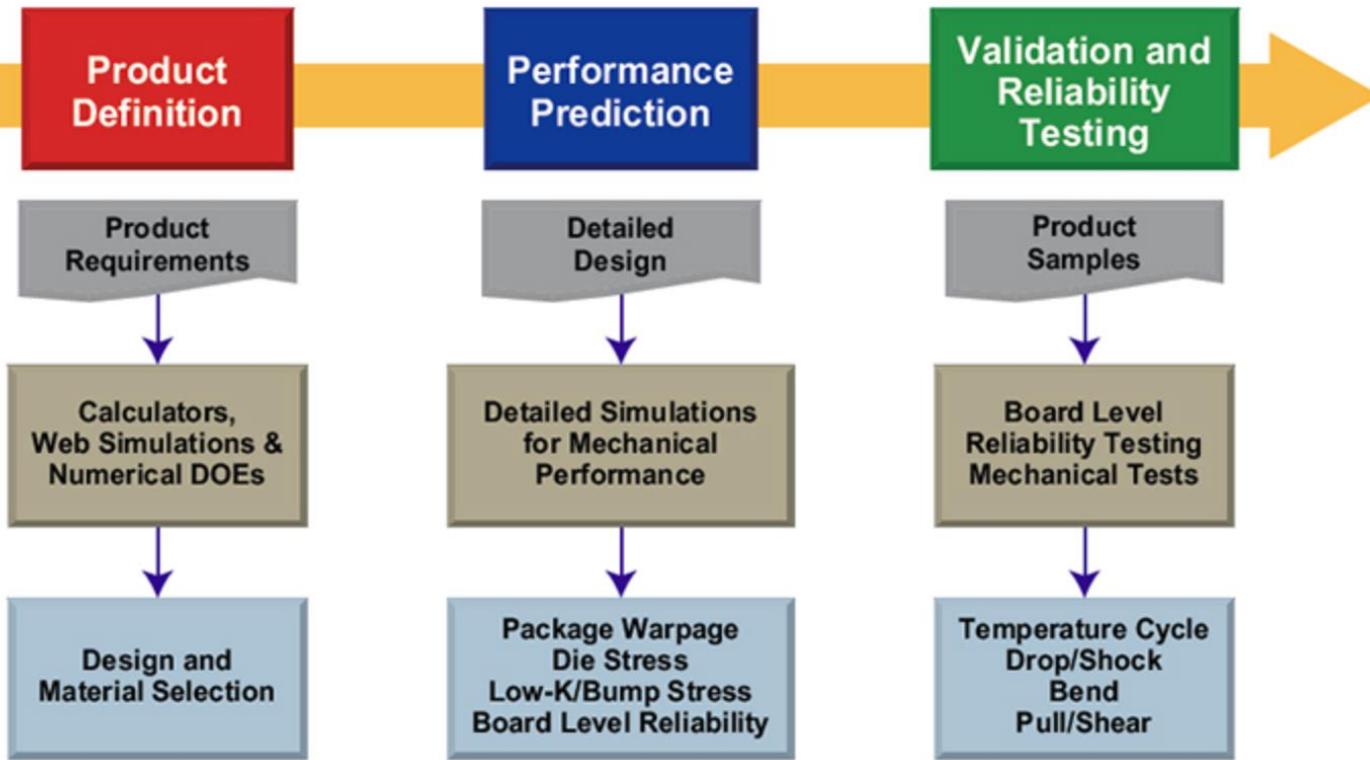
The above plot shows improvement in life for Cu pillar over SnAg bump for the same current/temperature condition and similar bump/UBM geometry. No failure was observed in Cu Pillar bump even after 8000 hours of testing at the same condition.

- Materials and structure selections can have orders of magnitude influence on reliability parameters
- Specialized test structures needed to correctly evaluate

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Board vs. Package Level Testing

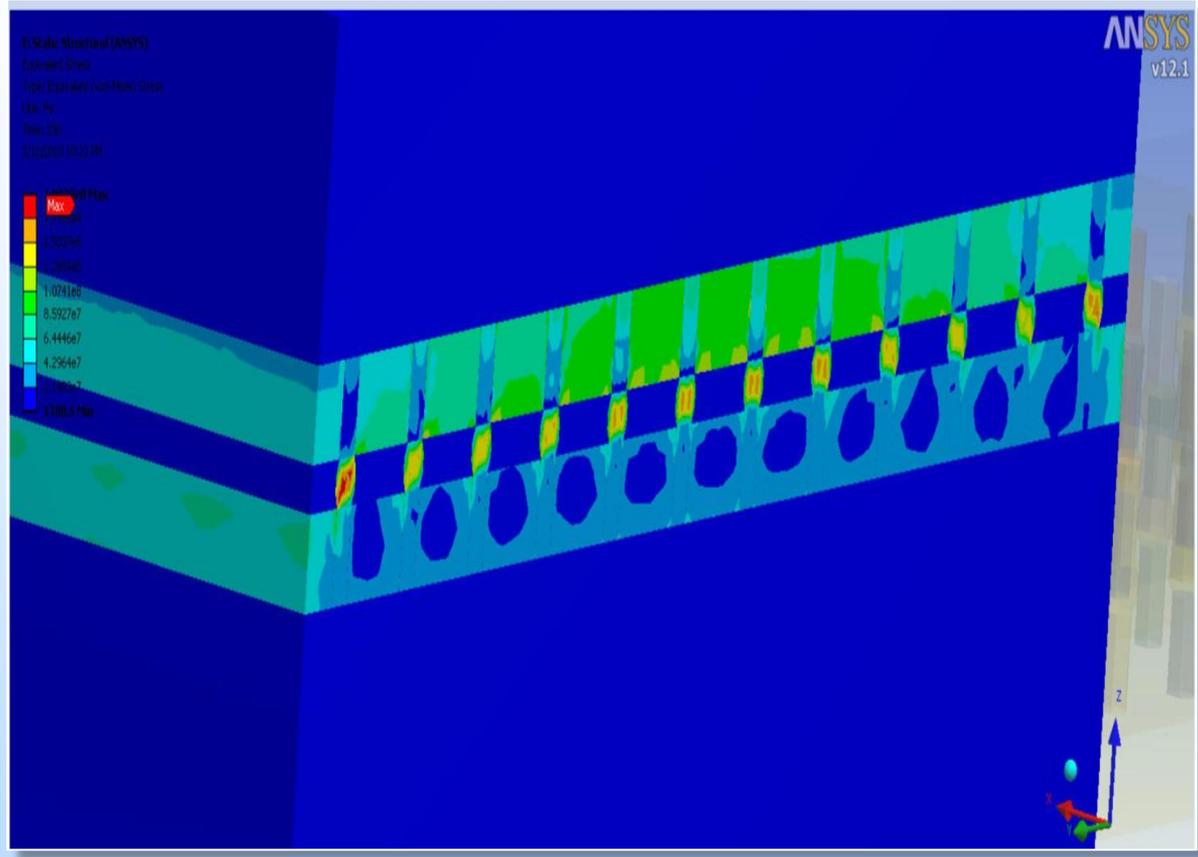


- Package vendors consider board level reliability a key benchmark of overall package reliability
- Technology choices are engineered and optimized to match die to board
- Opportunity for NASA requirements evolution

<https://www.amkor.com/go/turnkey-services/mechanical-characterization>

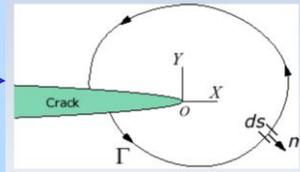


Reliability Modeling – Coarse vs. Fine Grain Analysis



- With micron scale dimensions and advance metallurgical interfaces, does historical Coffin-Manson fatigue approach apply?
- FEM tools allow for more sophisticated analysis (general energy released) but does this translate to product level differences?

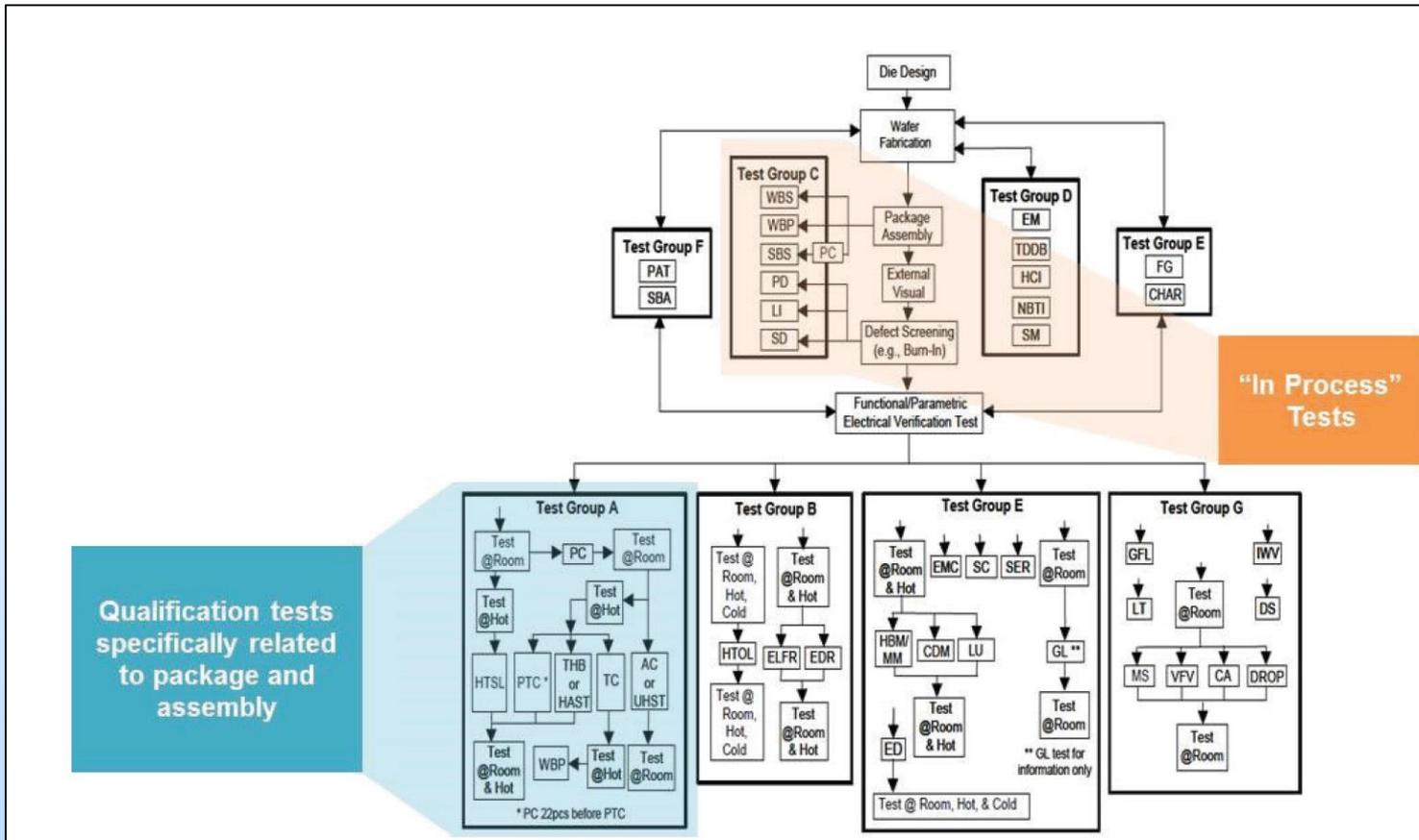
$$\frac{\Delta \epsilon_p}{2} = \epsilon'_f (2N)^c$$



$$J = \int_{\Gamma} \left(w dy - T_i \frac{\partial u_i}{\partial x} ds \right)$$



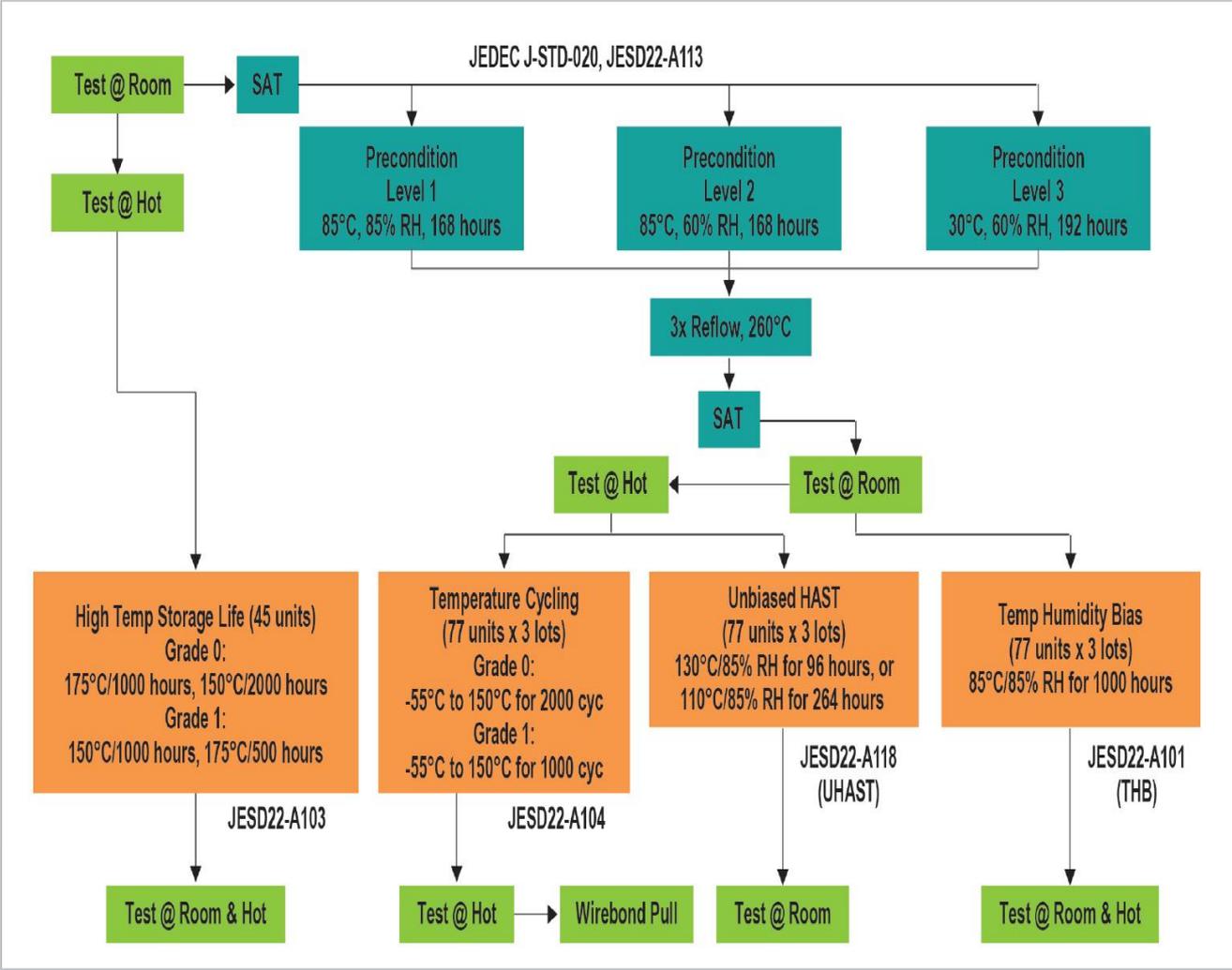
Leverage Automotive Package Quals



- AEC-Q100 Qual test flow
- Automotive market is beginning to demand benefits of modern packaging
- Not quite as quick as mobile phone market however



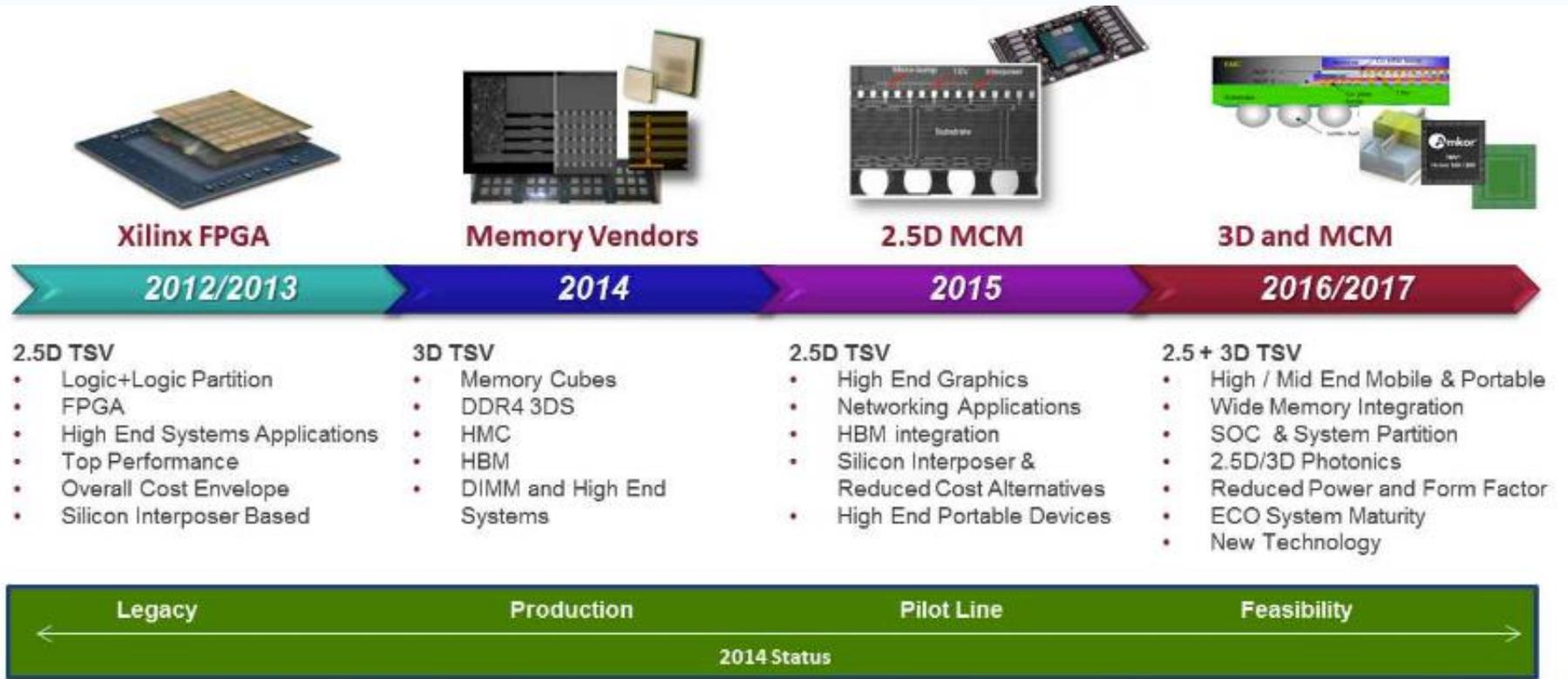
AEC-Q100 Group A



- A possible model for NASA Missions
- Amount of testing is expensive but possibility manageable



Where is it all headed?



- All aspects of semiconductor technology and devices are being impacted by 3D packaging technologies
- Heterogeneous die integration, optical/electrical, etc.



Plans

- **Evaluation of product and daisy chain technologies**
 - Determine root cause failures as much as possible
- **Integrate failure mechanisms into formal qualification requirements**
 - Collaborate with Aerospace on Automotive Qual applications
- **Continue partnerships for fundamental technology test structures**