The Mars 2020 Lander Vision System: Architecture and I&T results
IPPW 2017


June 15, 2017
Terrain Relative Navigation

TRN enables access to hazardous landing sites

Hazards in Landing Ellipse without TRN

Hazards in Landing Ellipse with TRN

TRN is implemented with LVS and STS

LVS provides improved horizontal position estimate

STS uses LVS position estimate to target safe landing site
Lander Vision System (LVS) Overview

**RAD750 Processor**
- Navigation Filter
- Data Flow

**CVAC Co-Processor**
- Image Processing
- Sensor Interfaces

**Memory**
- for map

**Vision Compute Element (VCE)**
- DIMU
- LCAM

**Rover Compute Element**
- 1553
- ICC/ITC

**Data Flow**
- IMU
- Image 1
- Image 2
- Image 3
- Image 4
- Image 5

**Outlier Residuals**
- time
- outlier threshold
- outlier

**Extended Kalman Filter**
- Propagate
- Batch update
- EKF update

**Rover Compute Element**
- Final Position Accuracy (40m 99% @ 2km)

**Vision Compute Element (VCE)**
- Remove Initial Position Error (3.2km 99%)

**Complete in 10 seconds**
- coarse landmark matching
- fine landmark matching
- Batch Initialization
- Extended Kalman Filter

**Sensor Interfaces**
- RS422
- UART
- LVDS

**CVAC Co-Processor**
- Image Processing
- Sensor Interfaces

**Memory**
- for map

**RAD750 Processor**
- Navigation Filter
- Data Flow
The Vision Compute Element (VCE) is a 3 slot 6U processor with a RAD750 general purpose processor, a power conditioning card (CEPCU1) and a new Virtex5 enabled Computer Vision Accelerator Card (CVAC).
Lander Vision System Camera (LCAM)

- LCAM must take crisp images under high attitude rates and velocities
  - Requires global shutter with short exposure time
- LCAM must provide images to VCE quickly to meet LVS image processing requirements
  - Requires low image latency
- LCAM must provide images that ensure enough landmarks are matched per image
  - Requires large FOV to image significant map area even when camera pointed up to 45° off-nadir
- LCAM must provide high quality information across each landmark for accurate and robust landmark matching
  - Requires detector with large number of pixels and high image SNR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Detector Type</td>
<td>Global Shutter and Grayscale</td>
</tr>
<tr>
<td>Number of Pixels</td>
<td>1024 x 1024</td>
</tr>
<tr>
<td>Field of View</td>
<td>90° x 90°</td>
</tr>
<tr>
<td>SNR</td>
<td>80 at half full-well depth</td>
</tr>
<tr>
<td>Exposure Time</td>
<td>~1ms</td>
</tr>
<tr>
<td>Latency</td>
<td>~100ms</td>
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</table>
LVS Data Flow & Processing

RAD750 Flight Processor
  VxWorks OS
  VCEFSWE
  Batch Init Estimator
  Extended Kalman Filter
  Image Processing Control
  Outlier Rejection

CVAC Co-Processor

Housekeeping (HK) FPGA
  cPCI I/F
  1553 I/F
  ICC/ITC I/F
  Timekeeping

Vision Processor (VP)
  FPGA
  Camera and IMU I/F
  Image Processing
  Functions

Memory
  map

Spacecraft init packet (p,q,v,A) (8 Hz)
  1553
  LVS Measurement Pkt (p,q,v) (8 Hz)

accel, angular rates (200 Hz)
grayscale image (~1 Hz)

DIMU

LCAM

Rover Compute Element
LVS Integration & Test Flow

Modeling

- LVS low level modeling
- Inputs from BB & EM lab & field tests
- LVS behavioral modeling

Breadboard

- LVS BB
- BTE

EDU/EM

- LVS EDU2
- LVS EDU4
- LVS EM1
- LVS FM
- LVS FS

FM

- Assembled and IPTO completed, no testing beyond IPTO

LVS Relevant Req. V&V Level

- 7 & 6
- 5 & 4
- 4 & 3

BTE

- GSE supports all venues except Cruise

LVS Team

- ATLO
  - Env Testing
  - LVS functional

GN&C / FS / ATLO / MS

- Cruise
  - LVS uses BIT
VCE I&T Status

• Breadboard
  – I&T complete
    • Initial testbed to develop test procedures and checkout CVAC design
    • Demonstrated that CVAC design is fundamentally sound

• EDU
  – I&T in progress
    • Completed majority of preliminary CVAC interface and functional tests
    • Detailed interface and functional tests continuing
VCEFSWE I&T Status

• Developed prototype that can execute end-to-end MRL sequence using VP functions on the VCE breadboard and EDU
  – Used canned input data for DIMU, LCAM and 1553 RT
  – Exercised coarse and fine mode IP functions in the VP FPGA
• Timing information provided key insights into improvements needed in the VP FPGA

• VCE CVAC Breadboard testbed
• No GSE sensor input supported
Key Upcoming LVS Milestones

• 2017
  • Continued LVS development activities; VCE, LCAM, VCEFSWE

• Q2 2018
  • EM VCE, EM DIMU, EM LCAM, VCEFSWE 2.0 delivered to LVS team
  • EM LVS I&T

• Q3 2018
  • EM LVS V&V
  • FM VCE, FM DIMU, FM LCAM, VCEFSWE 3.0 delivered to LVS team
  • FM LVS I&T/V&V

• Q4 2018
  • FM LVS delivered to ATLO
BACKUP
VCEFSWE and MRL Algorithms Data Flow

Radial Distortion Correction
Homography Warp
Image Normalization
Interest Operator
FFT Correlation
Spatial Correlation

Hardware

Device Driver/Library Module

Sensor

Task Module

Event w/ data

VCE RAD750

Driver Layer

LVS Meas_pkt

Camera_pose

tim

iplib

filterlib

dimu_pkt

img_exposed_time

imu_pkt

ML_pkt

batch_estimate

ML_update

init_pkt

VCEFSW Driver

MRL

RCE FSW

VCEFSW

RCE RAD750

DIMU

CVAC VP FPGA

DIMU MGR

LCAM

MGR

DIMU

RT MGR

CVAC HK FPGA

HSS

RC FSW

MCIC 1553 BC

MSIA ICC/ITC

14th International Planetary Probe Workshop

The Hague, Netherlands | June 2017
LVS Testbed

LVS Simulation

model

dynamics

HW

SW

GSE
### Key Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATLO</td>
<td>assembly, test, launch operations</td>
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<tr>
<td>BB</td>
<td>breadboard</td>
</tr>
<tr>
<td>BIT</td>
<td>built-in test</td>
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<tr>
<td>CEPCU</td>
<td>compute element power conditioning unit</td>
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<tr>
<td>CVAC</td>
<td>computer vision accelerator card</td>
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<tr>
<td>DIMU</td>
<td>descent inertial measurement unit</td>
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<tr>
<td>EDL</td>
<td>entry, descent, and landing</td>
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<tr>
<td>EDU</td>
<td>engineering development unit</td>
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<tr>
<td>EM</td>
<td>engineering model</td>
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<tr>
<td>EMC</td>
<td>electromagnetic compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>electromagnetic interference</td>
</tr>
<tr>
<td>FM</td>
<td>flight model</td>
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<tr>
<td>FOV</td>
<td>field of view</td>
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<tr>
<td>FPGA</td>
<td>field programmable gate array</td>
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<tr>
<td>GNC</td>
<td>guidance, navigation and control</td>
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<td>GSE</td>
<td>ground support equipment</td>
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<tr>
<td>HK</td>
<td>housekeeping (RTAX 2000) FPGA</td>
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<tr>
<td>I&amp;T</td>
<td>integration and test</td>
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<tr>
<td>IP</td>
<td>image processing</td>
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<tr>
<td>LCAM</td>
<td>LVS camera</td>
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<td>LVS</td>
<td>lander vision system</td>
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<td>LVSS</td>
<td>LVS simulation</td>
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<td>LVSTB</td>
<td>LVS test bed</td>
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<td>MRL</td>
<td>map relative localization</td>
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<tr>
<td>RCE</td>
<td>rover compute element</td>
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<tr>
<td>RT</td>
<td>remote terminal</td>
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<tr>
<td>SNR</td>
<td>signal to noise ratio</td>
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<td>VCE</td>
<td>vision compute element</td>
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<tr>
<td>VCEFSW</td>
<td>VCE flight software</td>
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<td>VP</td>
<td>vision processor (Virtex 5) FPGA</td>
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<tr>
<td>V&amp;V</td>
<td>verification and validation</td>
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Terminology

- **TRN** = Terrain Relative Navigation
  - All the new development to avoid known hazards in the landing ellipse

- **STS** = Safe Target Selection
  - Picks the safe landing site between a-priori hazards based on the position provided by LVS

- **LVS** = Lander Vision System
  - The system that performs Map Relative Localization

- **MRL** = Map Relative Localization
  - The algorithms that compute position relative to a map

- **VCE** = Vision Compute Element
  - The LVS processor containing three cards

- **RAD750** = processor card

- **CVAC** = Computer Vision Accelerator Card
  - HK = Housekeeping FPGA on CVAC
  - VP-E = re-programmable Virtex5 FPGA on CVAC with sensor interfaces and image processing

- **CEPCU1** = power conditioning card

- **VCEFSWE** = VCE Flight Software for EDL

- **LCAM** = LVS Camera, procured from MSSS