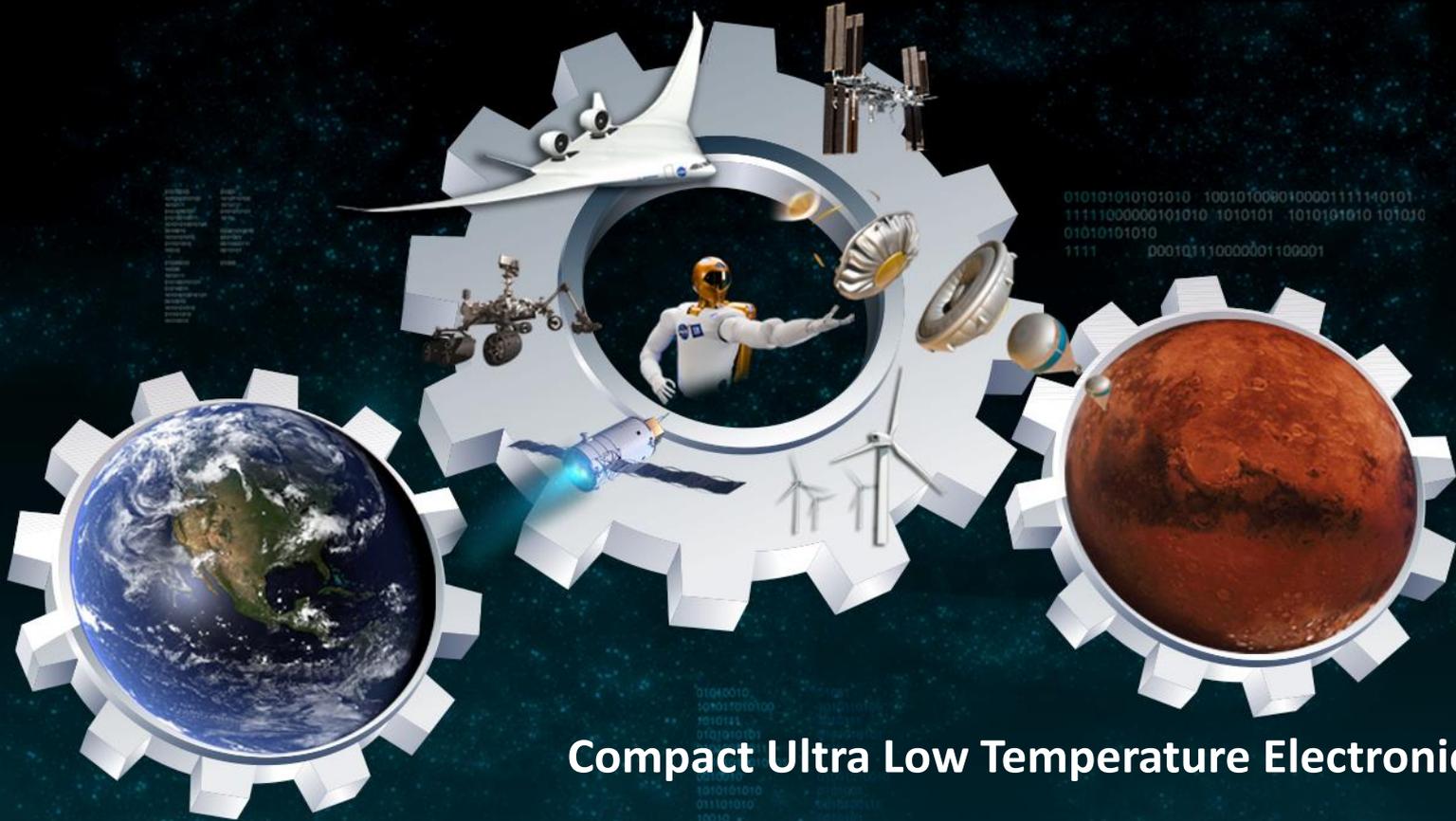


*Space Technology Mission Directorate
Game Changing Development Program
2016 Annual Program Review*

National Aeronautics and
Space Administration



Compact Ultra Low Temperature Electronics

Presented By: Gary Bolotin

Jet Propulsion Laboratory, California Institute of Technology

4/26/2017

TECHNOLOGY DRIVES EXPLORATION

Overview: Ocean Worlds Technology: Ultra Low Temperature Electronics



Develop a Next Generation Compact Avionics Package (Command & Data Handling, Power and Motor Control)

- Allow the conceptual Europa Lander to last longer on the surface or allow more room for additional science by reducing the volume, mass and power of its avionics and the amount of energy required to keep the avionics warm.
- This goal would be achieved through Advanced Electronic Packaging, low power computing and cold capable electronics.
 - Decrease the volume (10x), and mass (3x), of electronic assemblies through the use of chip scale packaging
 - Reduce the power (2x) by the use of an efficient processor and on-board power management

Integration with other projects/programs and partnerships

- This project is going on concurrently with Europa Lander Concept baseline.
© 2017 California Institute of Technology. Government sponsorship acknowledged.
- Project Plan: The project plan approved and completed on 11/12/15
- STMD Data Analysis Tool: TBD

Technology Infusion Plan:

- We are working closely with our potential customer, the Europa Lander Project. This includes being part of the project formulation process and working to the same set of requirements.
- Infusion of our technology will be facilitated by a series of demonstrations leading to a demonstration of TRL 6 prior to the project PDR.
- A selection between an Avionics system based upon this technology and the baseline Europa Lander design will be made prior to PDR.
- Can be used in other mass, power, and volume constrained systems.

Key Personnel:

Program Element Manager: Gary Bolotin

Project Manager: Tom Cwik

Lead Center: NASA Jet Propulsion Laboratory

Supporting Centers: N/A

NASA NPR: 7120.8

Guided or Competed: Guided

Type of Technology: Pull

2017 GCD Mid Year Review **Predecisional information for planning and discussion only'**

Key Facts:

GCD Theme: FPES

Execution Status: Year 2 of 1.5

Technology Start Date: 9/1/2015

Technology End Date: 2/1/2017

Technology TRL Start: 4

Technology TRL End: 6

Technology Current TRL: 4

Technology Lifecycle Phase: Formulation (Pre-Phase A)



Agenda



- Technology Overview
- Project Summary
- Project Goal
- Technical Performance
- Infusion
- Key Performance Parameters
- TRL Assessment
- Last Quarter's Assessment
- Lessons Learned



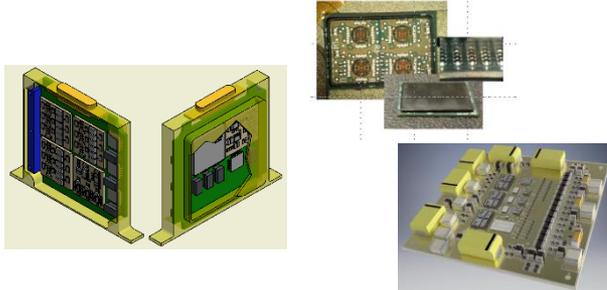
Compact Ultra Low Temperature Electronics Technology Overview



Leverage advanced packaging, cold capable electronics and system on a chip technology to maximize the science return from the baseline Europa Lander.

Advanced Electronic Packaging

Chip On Board Technology



Enables a >10X improvement in board density

High Density Connectors



Up to 500 pins per connector
3x density of standard micro-D

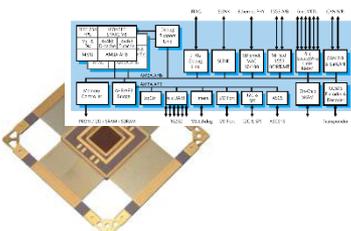
Slice Based Design



Eliminates backplane and chassis mass

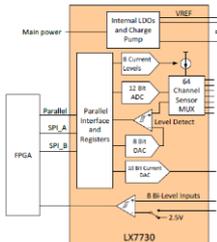
System On A Chip

Single Chip Computer



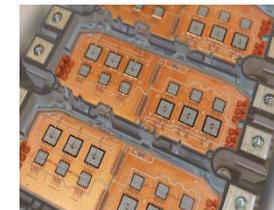
Allows for a single board command and data handling system

Single Chip Telemetry Collection



Cold Capable Electronics

Conductive Epoxy



Allows for -200C survival temperatures



Level 1 Project Goals



Level 1 Project Goals

Ocean World Europa Technologies (OWET)

ULTE

Goal #1

Develop technologies that reduce electronic packing volume and power requirements that enable extended operation lifetime for exploration missions to icy destination such as Europa.

The goal is to develop technologies that maximize the science return from the baseline Europa Lander. These technologies will allow the lander to last longer on the surface or allow more room for additional science instruments.

Notes:



Key Performance Parameters (KPP)



Key Performance Parameters

Ocean Worlds Europa Technologies (OWET)

Performance Parameter	State of the Art	Threshold Value	Project Goal	Estimated Current Value
Ultra-Low Temperature and Radiation Hard Electronics				
Volume (cc)	11250	<3000	1500	Volume: 1032 cc
Mass (Kg)	13.7	<6	4	Mass: 4.5 Kg
Power (W)	26	<15	13	Power: 12 W
Non-operational Temperature Range (C)	-55 to +125	-55 to +125	-100 to +125	-55C to +125 for CDH ¹ -180C to +125 outside
Operational Temperature Range (C)	-55 to +125	-55 to +125	-70C to +125	-55 to +125C for CDH ¹ -55 to +125C outside
<u>Notes:</u>				

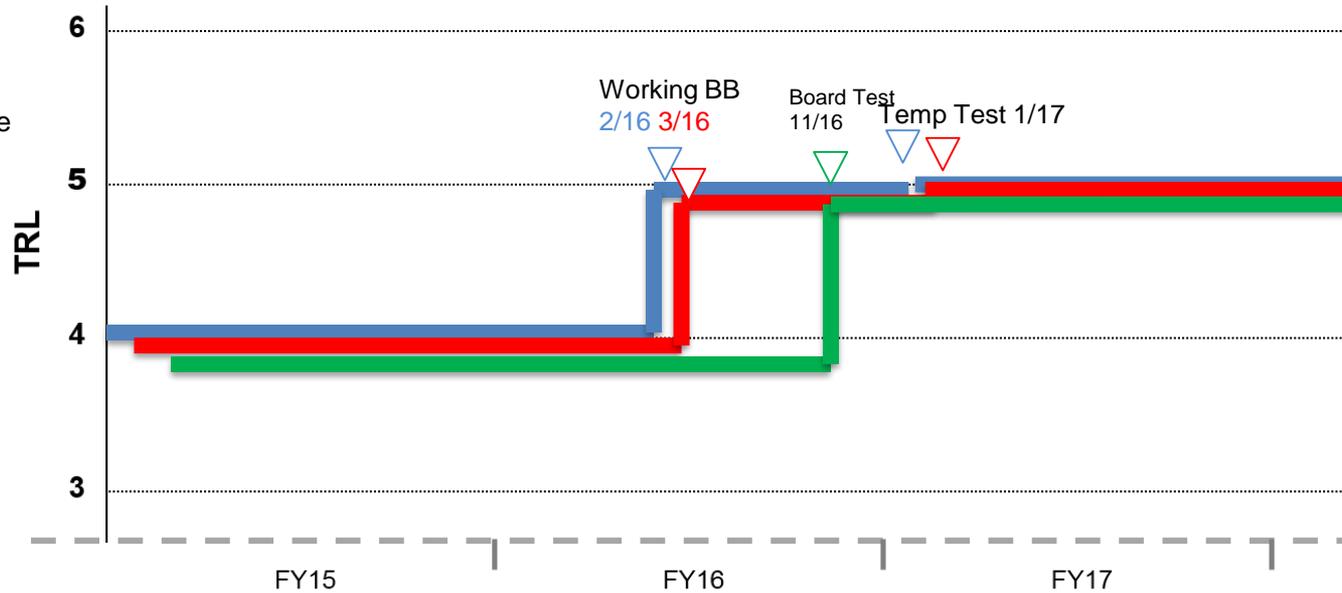
1. Europa Lander's vault would provides a protected thermal environment due to self heating of the electronic assemblies.
 2. Qualification was down to -180C
- Our cold capable electronics focused on survival of electronics in the ambient environment.



Technology Readiness Level (TRL) Assessment - ULTE



- Resolver Module
- Motor Driver Module
- Computer Card



Technology	Starting TRL	Ending TRL	Comments
Resolver Module	4	6	Module has been tested over temperature
Motor Driver Module	4	6	Module has been tested over temperature
Computer Card	4	5	SDRAM needs to be replaced with SRAM. RTG4 replace with RTAX to meet 300KRad requirement
Low Temperature Design Rules	4	5	Temperature cycle testing will need to be repeated. First test failed due to workmanship issues.

Key and Controlled Milestones



FY15 Key and Controlled Milestones		Baseline Completion Date	Actual Completion Date	Updated Milestone	Estimated Completion Date	Variance Explanation
<i>FY16 Q1 (Oct 1 through Dec 31)</i>						
A	Signed ULTB Technology Implementation Plan	10/29/2015	11/12/15			
AP_SE-01	Risk list complete	12/1/2015	12/1/15			
AP_LPMC-01	FSW framework selection	12/31/2015	2/28/16			
<i>FY16 Q2 (Jan 1 through March 31)</i>						
CCE-04	Cryogenic thermostat requirements complete	2/1/2016	2/1/2016			
AP_SE-02	Preliminary system design complete	3/1/2016	3/1/2016			
AP-01	Selection of candidate modules for validation	3/1/2016	3/1/2016			
<i>FY16 Q3 (Apr 1 through June 30)</i>						
AP_LPMC-02	Board ready for fab and assembly	3/31/2016	7/11/16	8/18/16		
CCE-01	Operational limits of key components identified	6/1/2016	3/23/16	6/1/16		
<i>FY16 Q4 (Jul 1 through Sep 30)</i>						
AP-02	Modules delivered from vendor to JPL	7/1/2016	Motor Driver: 9/26/16 Resolver 12/21/16	12/1/17		We are developing two modules. The first module (Motor Driver) is progressing on schedule. The second module is delayed about 3 months because of die availability and die contract negotiations.
AP_LPMC-03	Board STM/IPTO tests completed	8/15/2016	11/2/16	10/22/16		It took one month longer than expected to fabricate the computer card.
<i>FY17 Q1 – FY17 Q2</i>						
CCE-05	Design rules and recommendations complete	12/1/2016	12/5/16			The document on our design rules and recommendations has been generated
AP_03	Module testing completed – nominal temperature	11/1/17	Motor Driver: 11/4/16 Resolver : 12/21/16			Testing of both the Resolver and Motor Driver modules at nominal temperature is now complete
AP_SE-03	Final Report	02-01-17	4/20/17			

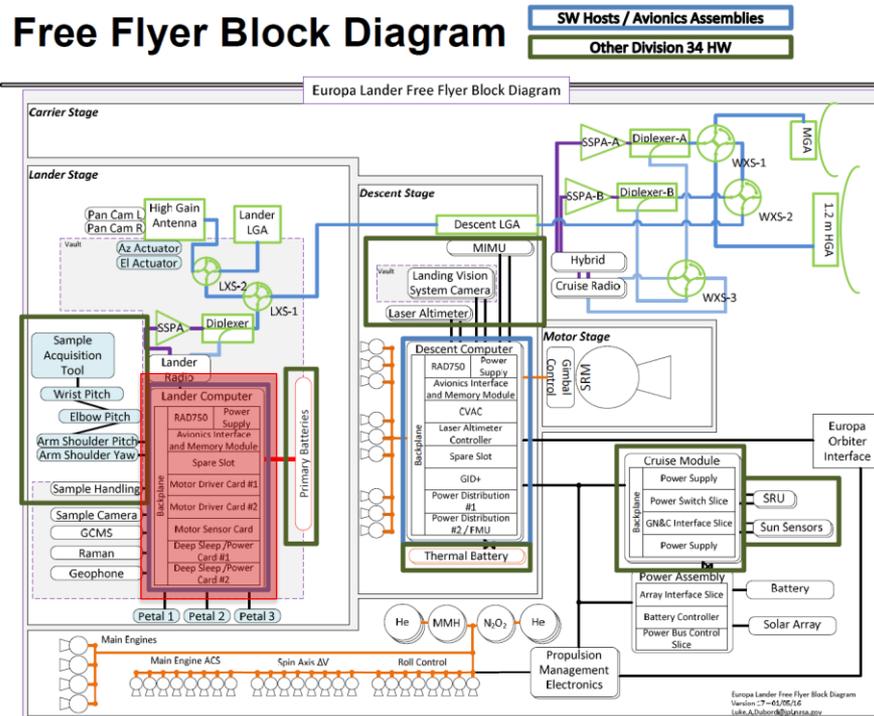
All Key and Controlled Milestones have been completed



Compact Ultra Low Temperature Electronics Europa Lander Concept Avionics Context



- Our requirement set was developed from the Europa Lander baseline design.
- We focused on the needs of the lander computer only.



Europa Lander Baseline

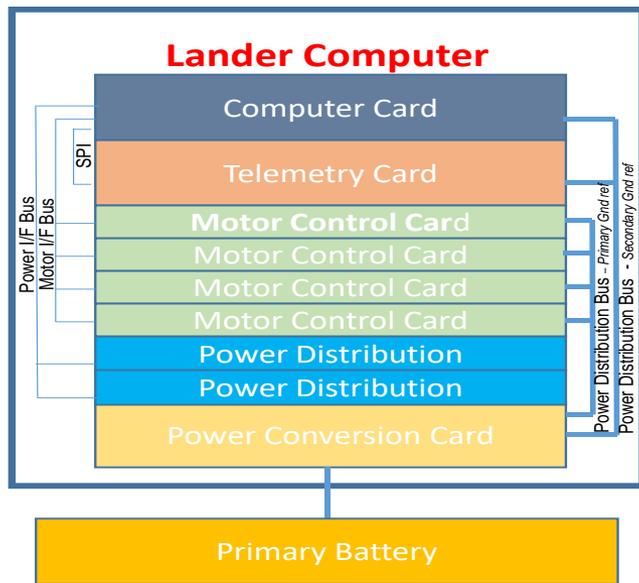


Compact Ultra Low Temperature Electronics Project Goal



This project would allow the Europa Lander to last longer on the surface or allow more room for additional science by reducing the volume, mass and power of its avionics and the amount of energy required to keep the avionics warm.

This goal is achieved through the use of advanced electronic packaging, low power computing and cold capable electronics.



Baseline Lander Avionics		
Mass	14.13	Kg
Volume	11250	cc
Power	26	W

Baseline Lander Avionics		
Survival	-55C to	+70C

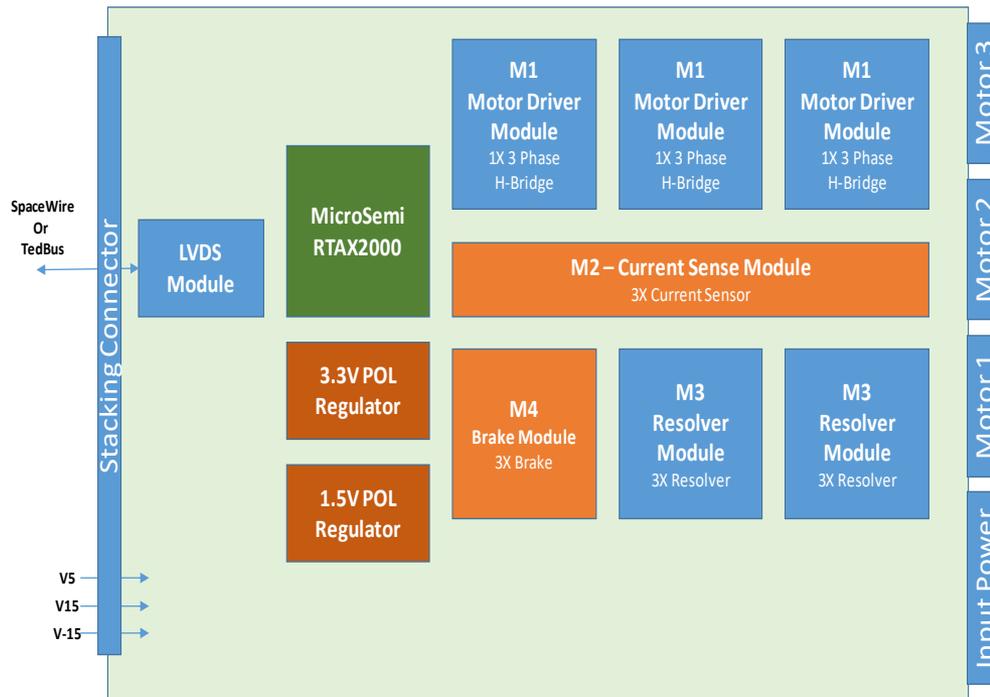


Tech Lander Avionics		
Mass	3.58	Kg
Volume	1159	cc
Power	13.44	W

Tech Lander Avionics		
Survival	-200C to	+70C



Compact Ultra Low Temperature Electronics Motor Control Card



Developed under OW GCT

- M1 Motor Driver Module
- M3 Resolver Module

Development under Europa Lander

- M2 Current Sense Module
- M4 Brake Module
- FPGA development

Development under COLDTech proposal / Europa Lander

- 3.3v POL Regulator
- 1.5v POL Regulator

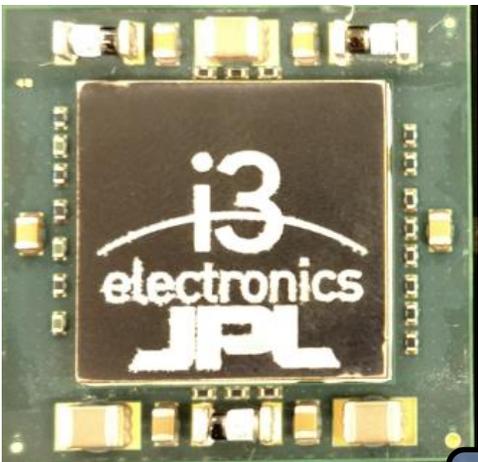
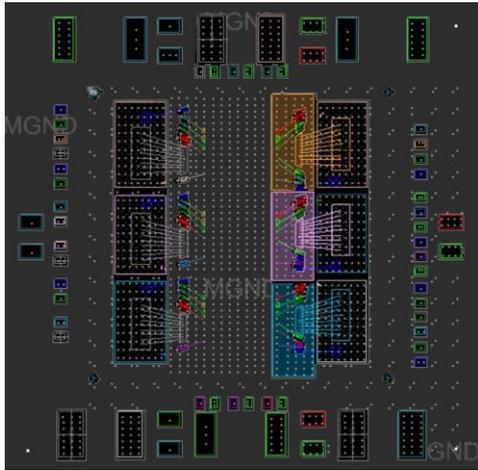
- This card is capable of controlling up to three 3A motors one at a time.



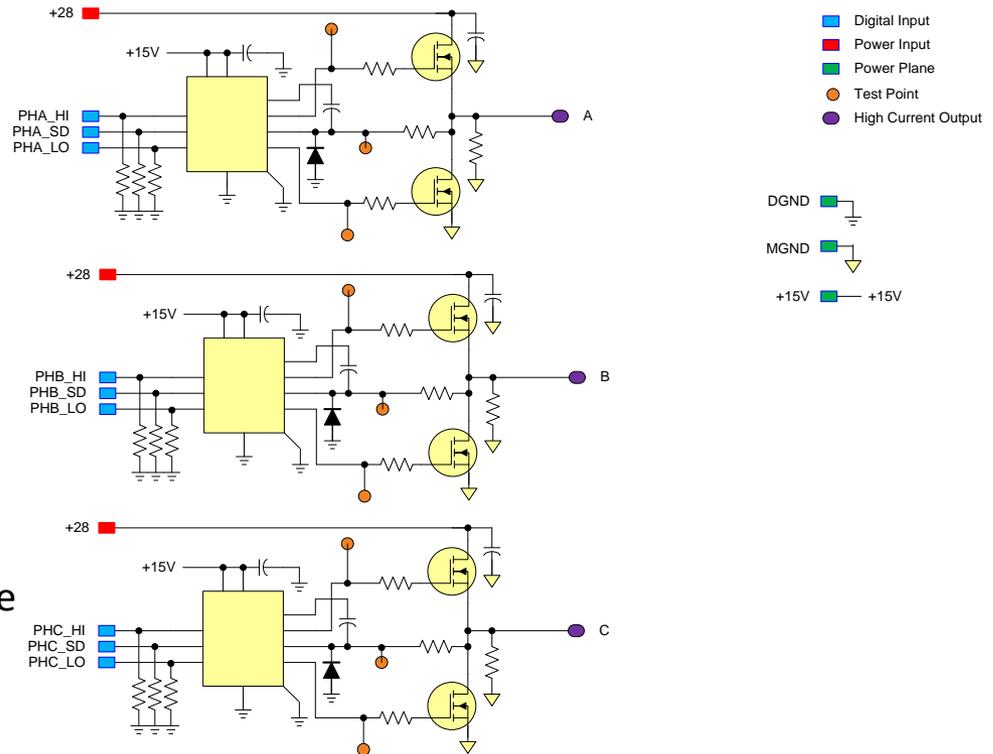
Compact Ultra Low Temperature Electronics - M1 Motor Driver



[link to agenda](#)



- S# - 001
- M1 Module



EUROPA LANDER
MOTOR CONTROL M1 MODULE
J. WATERS – Edited by Gary Bolotin
12 FEBRUARY 2016

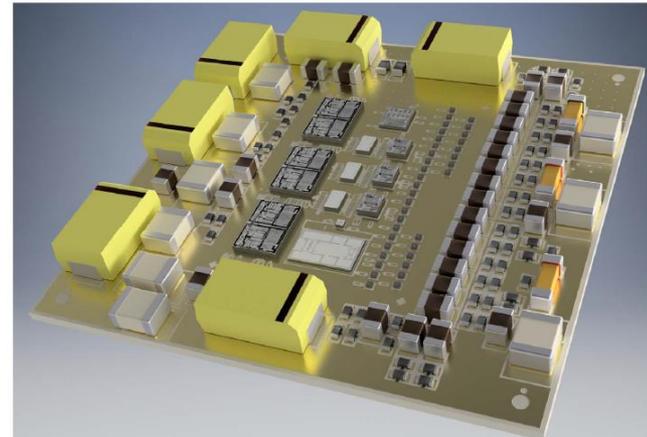
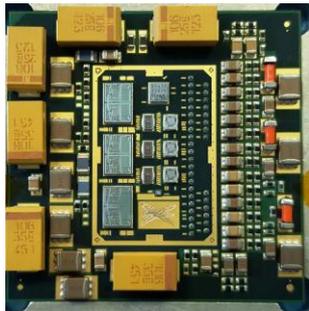
7cm x 7cm worth of circuitry reduced to 2.5cm x 2.5cm



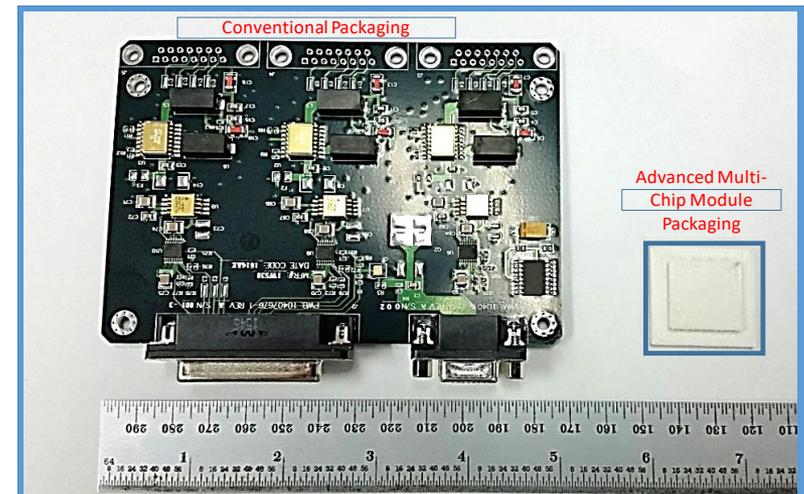
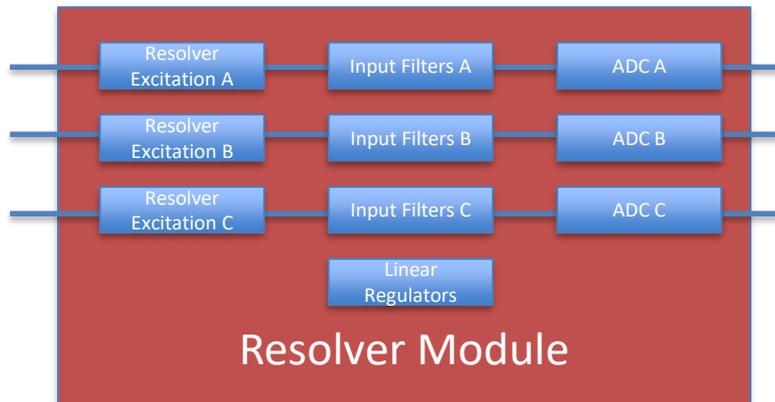
M3 Resolver Module First Module Complete



- **Advanced Packaging – M3 – Resolver Module**
 - Production of first module is complete. First part received at JPL 12/21/16.



- Single provides interface to 3 resolvers



Advanced Packaging Accomplishments and Technical Challenges



• Advanced Packaging

- Three modules are being developed
 - M1 Motor Driver Module
 - M3 Resolver Module
 - LVDS Module (design done by JPL's UNIBUS task)
- Each module design will go through the following process



M1

- **M1 Module completed temperature tests at -55C and +125C on 1/12/17**

M3

- **M3 Modules delivered to JPL on 12/21/17**
- **First module tested at room temp 12/28/16 and completed temperature tests at -55C and +125C on 1/12/17**

LVDS

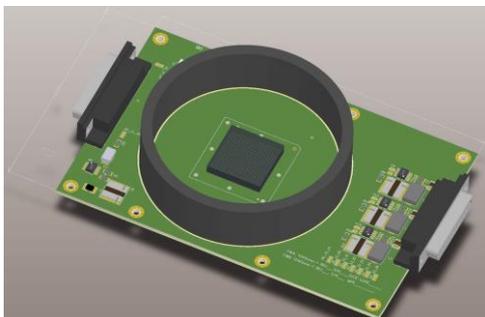
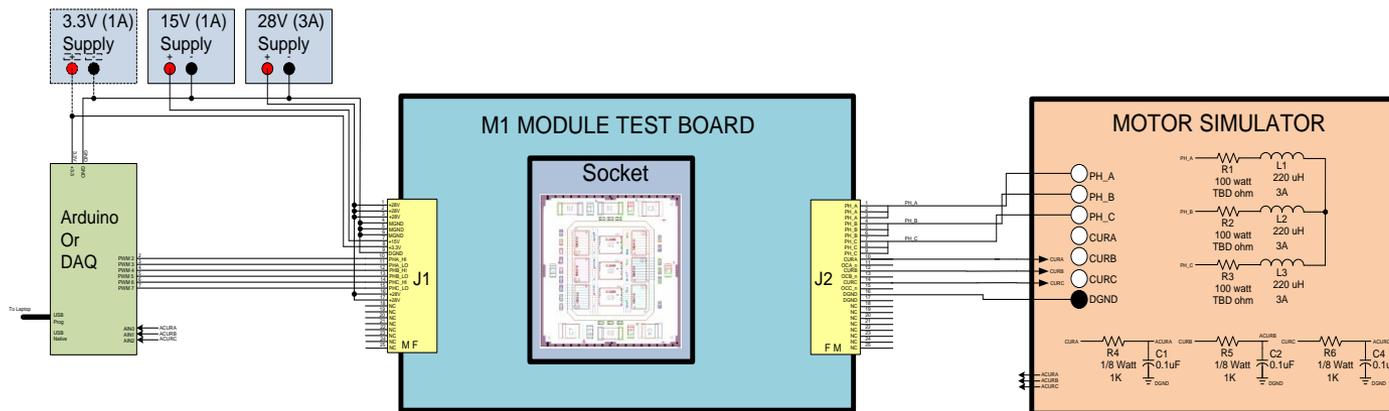
- **LVDS Modules room temp testing is complete.**
- **Module completed temperature tests at -55C and +125C on 1/12/17**



Compact Ultra Low Temperature Electronics - M1 Module – Testing



[link to agenda](#)



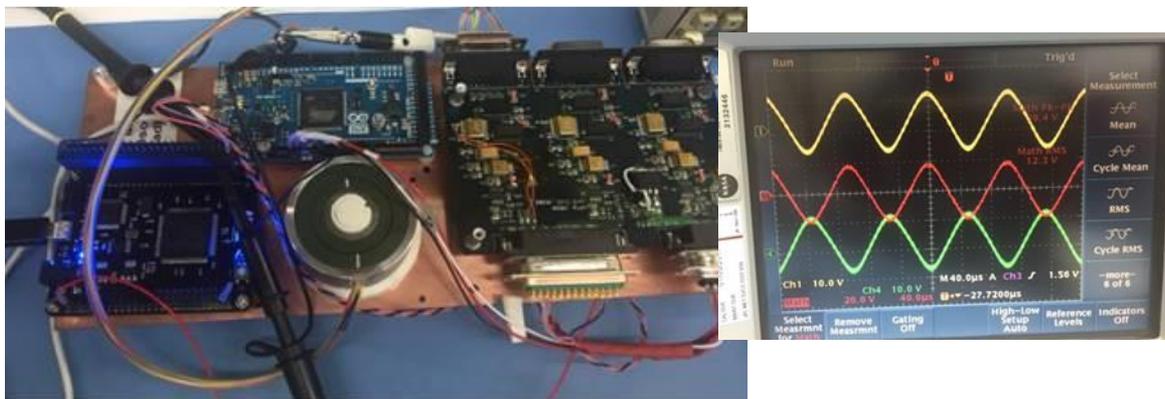
Module testing is complete



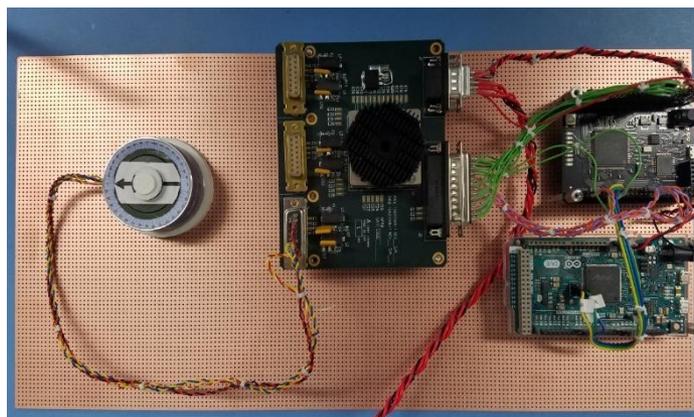
Compact Ultra Low Temperature Electronics — M3 Resolver Module – Testing



[link to agenda](#)



Resolver Module Breadboard



Resolver Module Test board

Module testing is complete



Compact Ultra Low Temperature Electronics Manx - Computer Card



[link to agenda](#)

Processor	Gaisler Cobham GR712, Sparc, Dual-Core
FPGA	Microsemi RTG4
Radiation Environment Target	300 kRad TID
Operating Voltage	5V
Input Voltage (recommended)	5V
Input Voltage (limits)	5-TBD V
Spacewire Links	10 (5 scoped for Motor Control)
UARTS	2 (FPGA)
Peripherals	ENET, I2C, SPI, GPIO, CameraLink
Housekeeping	8ch ADC (Voltage, Temp, Current)
Non-Volatile Memory	8GBytes NAND, 128KBytes X 2 bootloader
Processor Memory	400MBytes SDRAM
Processor Clock Speed	100 MHz (configurable)
Connectors	100 Pin VerSI, 160 Pin Mezzanine

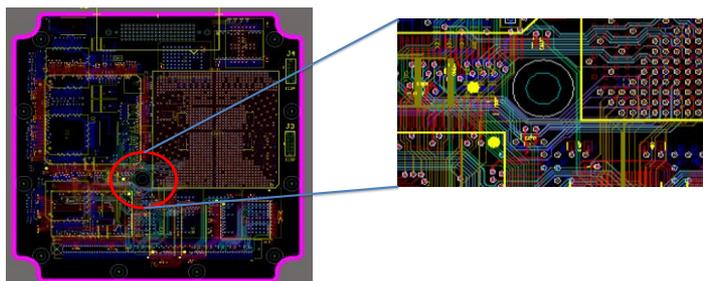
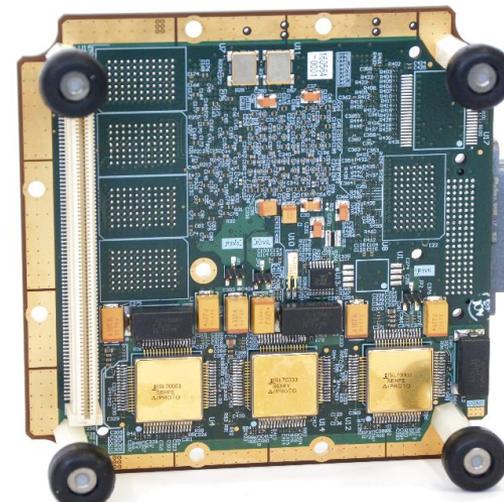
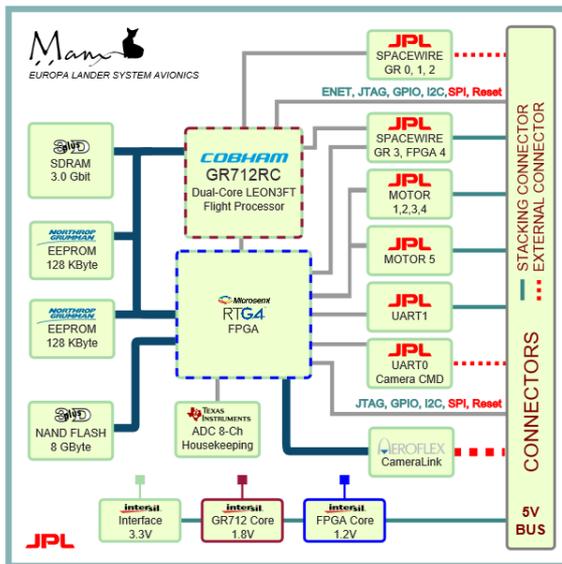


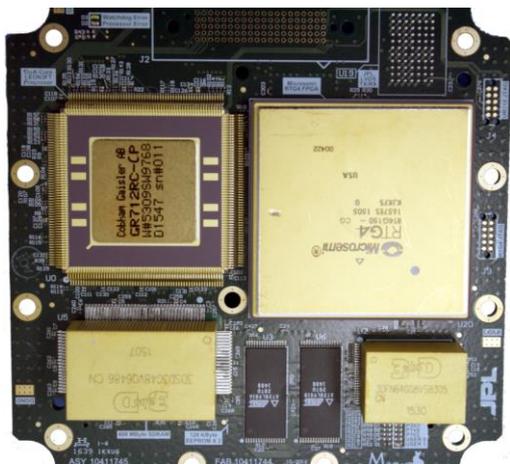
Illustration of Computer Card Wiring Density



Compact Ultra Low Temperature Electronics Manx - Computer Card Status



[link to agenda](#)



- Computer Card
 - Requirement Peer Review – 2/29/16
 - Conceptual Design Peer Review – 3/24/16
 - Schematic Review – 5/23/16 completed on 5/25/16
 - MEDALS CONTRACT
 - Layout Review – 7/14/16 – Complete
 - Board Released for fabrication – 8/15/16
 - Assembly Started – 10/3/16
 - Assembly Complete – 10/14/16
 - Board Power Up – 11/7/16
 - LVDS Modules Tested and Installed
 - Testing of most major interfaces complete 12/16/16
 - Testing of FLASH memory is all that remains
 - We are waiting on the FPGA core to be developed under the Sphinx development.



Compact Ultra Low Temperature Electronics Cryogenic Daisy Chain/Solder testing



[link to agenda](#)

Board #	Ablesstik Ablesstik adhesive	Eutectic Solder(63/37)	88/10/2 Solder
PC009-1	Y		
PC009-2		Y	
PC009-3			Y
PC012-1	Y		
PC012-2		Y	
PC012-3			Y
TB4-1	Y		
TB4-2		Y	
TB4-3			Y

Table 5: Board types and construction methods

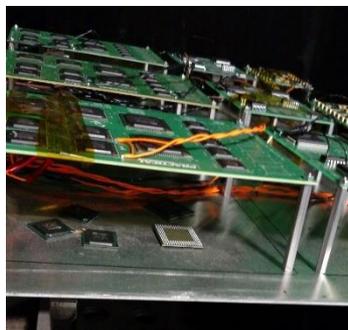


Illustration of components that had fallen off of the PC012 board (Ablesstik) observed after 30 cycles

This work will continue under JPL Advanced Concepts funding

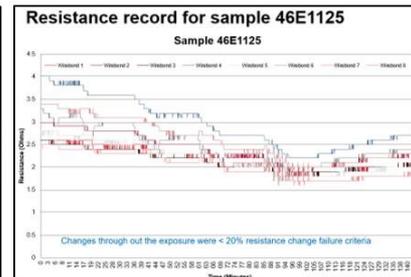
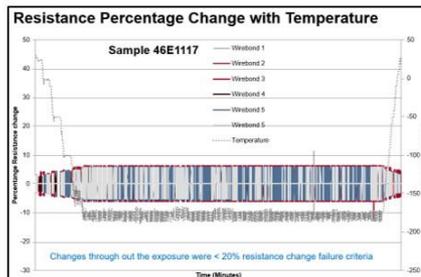
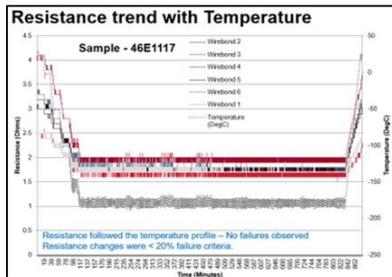
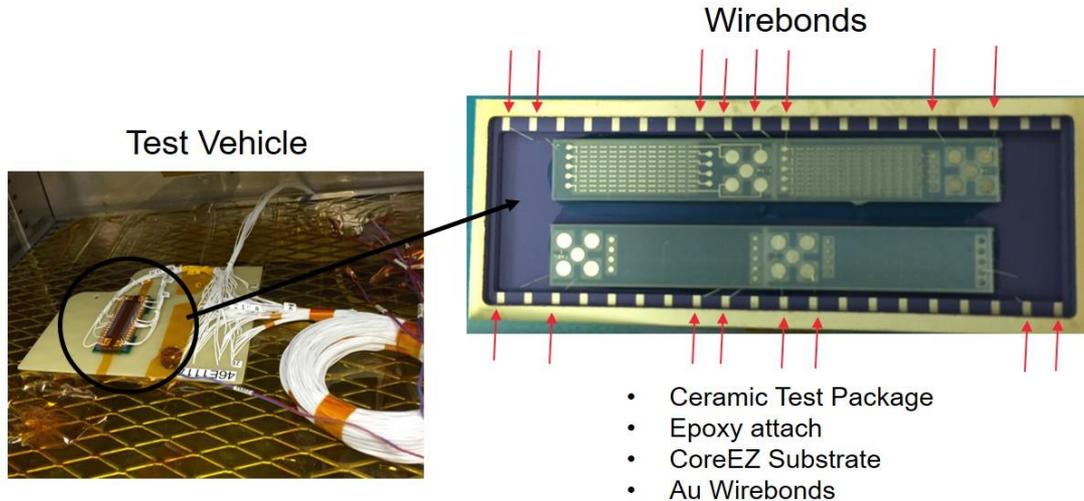


Compact Ultra Low Temperature Electronics Cryogenic testing of i3 CoreEZ substrate



[link to agenda](#)

Tests were conducted to test the effectiveness of the i3 CoreEZ substrate / ENEPIG finish / Gold and Aluminum wire bonds



No anomalies found over the temperature ranges 25C to 0C to -50C to -100C to -150C to -180C with (20 hr soak) back to 25C (15 dwell @ each temperature).

- pass criteria was no more than a 20% increase in resistance at a specific temperature

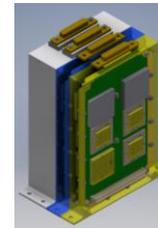
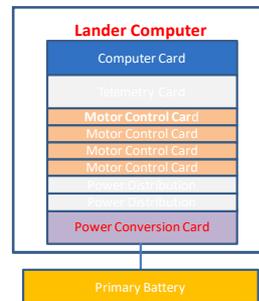


Compact Ultra Low Temperature Electronics Infusion Path Forward



- **Europa Lander Project Baseline**

- A standalone centralized motor controller based upon our technology is incorporated into the 4.0 baseline that will carry them through the MCR
- Project is taking advantage of our mass and volume savings
- Computer handles motor control functions.



100mm x 160mm x 74mm

- **The SMD COLDTECH proposal "Cold Survivable Distributed Motor Controller (CSDMC)" 2-year, \$1.2M, PI: Gary Bolotin, was selected.**

- This proposal is aimed at developing a distributed motor controller
- Proposal is based upon modules developed during this effort
- Funding is now at JPL. Work started March 1, 2017



Compact Ultra Low Temperature Electronics Infusion Path Forward - COLDTECH – Cold Survivable Distributed Motor Controller



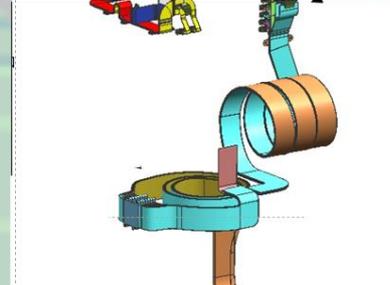
PROBLEM / SOLUTION



MSL Wiring Harness



MSL Robotic Arm

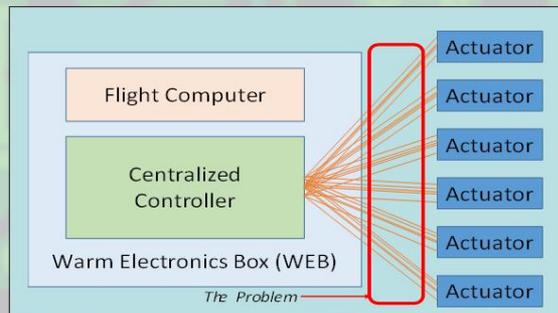


Robotic Arm: Wiring Complexity

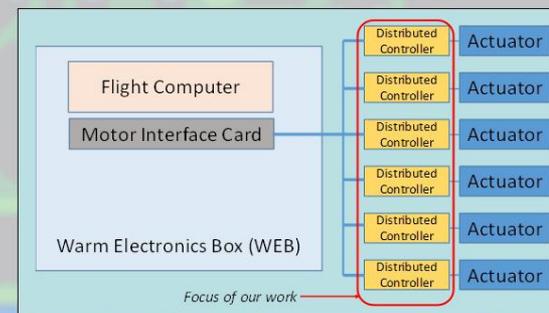


Integration and Test

Illustration of cabling mass and complexity in current landed mission architectures across all subsystems and phases of development



Current State of Practice: point to point wiring



Our Solution: Distributed Motor Control Electronics

Illustration of the solution to the problem: Distributing the controller electronics out at the actuators, and connecting them through a common power and interface bus

Ocean Worlds Technology: Ultra Low Temperature Electronics



- Standard 6U cPCI design
- Backplane and chassis required.
- High SWaP



MSL Rover RPAM

PROBLEM / NEED BEING ADDRESSED

Electronic assemblies take up a significant portion of spacecraft SWaP

PROJECT DESCRIPTION/APPROACH

- Decrease the volume and mass, of electronic assemblies through:
 - the use of advanced packaging.
 - Chip on board technology
- Reduce the power by:
 - the use of an efficient processor
 - on-board power management
 - minimizing power required for survival heaters.

QUANTITATIVE IMPACT

- Reduced mass and volume allows for either:
 - More room for science instruments or
 - More room for batteries enabling longer mission life.
- Reduced survival and operating temperatures allow for longer mission life.

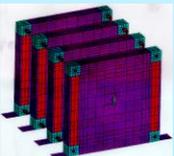
PROJECT GOAL

- Decrease the volume (10x), and mass (3x), power (2x) of electronic assemblies

STATUS QUO

NEW INSIGHTS

- Backplane free design
- Advanced packaging
- System on a Chip Processor
- CMOS tech can work cold



Backplane free chassis



Chip On Board Packaging