The Universal Space Transponder: A Next Generation Software Defined Radio

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***Abstract*—The Universal Space Transponder (UST) is a next generation transponder developed at the Jet Propulsion Laboratory to meet a large variety of telecom, navigation, and radio science needs for future deep-space and near-Earth missions. This paper details the UST software defined radio design and describes how the combination of a modular hardware architecture and in-flight reprogrammability enables a new level of flexibility and expandability for a space transponder. The UST uses common power and digital processing assemblies that can be integrated with a variety of RF modules and is capable of simultaneous, multiband operations with data rates up to 37.5 Mbps RX and 300 Mbps TX. This allows a single radio to support all the direct-to-Earth and relay communication requirements for even complex mission scenarios, reducing the total cost, mass, and power. The discussion includes a description of the current UST engineering models that have been built and tested, as well as details about the next generation capabilities supported by UST, including advanced link coding and modulation, radiometric techniques, and in-radio protocol handling. Details are also presented on RF modules and digital processing in development for radio science and astronomy purposes, including a bistatic radar receiver and broadband planetary emissions receiver. These will demonstrate the ability to integrate low-cost science instruments into the UST architecture, further expanding the versatility of the UST.**

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1. INTRODUCTION

With advent of extremely high density programmable digital hardware, the terrestrial communications industry has moved to software defined radio platforms for many applications. Key benefits of this change are the ability to meet evolving standards without hardware changes, lower re-spin costs, and reusable software and firmware. For space applications, NASA has two choices for the future: the traditional one-of-a-kind radios that are proprietary solutions with a high impedance to rapid technology infusion, or to implement and standardize software defined radios across missions, thereby creating multiple industry sources for communications hardware and software. Software defined radios of this type with associated standardization allow changes in the radio functionality to be made late in the spacecraft assembly and integration and test flow, and even during the mission.

Development of NASA software defined radios in the normal UHF, S, X, and Ka-bands typically follows the process in Figure 1. The requirements from the various systems (the Deep Space Mission System [1], the Near Earth Network [2], the Space Network [3], the mission being supported, the Space Telecommunications Radio Standard [4], and other outliers and unknowns) are combined in the process shown in the right of Figure 1, leading up to a family of radios.

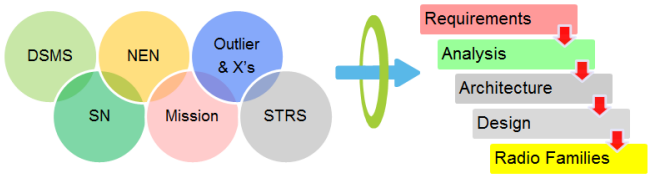

Figure 1 – NASA Radio Development

The first software radio developed for NASA missions under this model was the Electra family of radios at UHF and S-band. The UHF Electra radios form the basis of the Mars proximity communications network and have been extremely successful [8]. The S-band version is resident on the International Space Station as a communication testbed.

Around the time the first UHF Electra was flown on the Mars Reconnaissance Orbiter [5], a follow-on technology program to develop the next generation Universal Space Transponder (UST) was initiated. Key requirements on this next generation software defined radio family include significantly higher data rates, simultaneous multi-band and multi-channel operation, advanced modulation and coding techniques, support for new networking strategies such as Delay Tolerant Networking (DTN), and cutting-edge radiometric schemes. The radio architecture was also designed in a very modular manner, with core digital, power, and frequency hardware elements that could be configured with interchangeable RF front-end modules as required for

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each specific application. The radio software and firmware have also been developed in compliance with the NASA Space Telecommunications Radio System (STRS) standard for software defined radios, which improves interoperability of different digital processing functions.

Key applications of the UST radio will be to support NASA missions that require one or more simultaneous links, such as a Mars mission with simultaneous proximity (UHF and X-band) and direct to earth (X and Ka-band) communications. A single radio performing both functions can reduce cost, mass, and volume, and higher data rates could increase science data return. Targeted radiation design levels means that it could also be used on other outer planet missions with harsher radiation environments.

The remainder of this paper is organized as follows. There is a discussion of the UST architecture, including key trades performed to select this architecture, and details of different available configurations of the UST, including the integration of a bistatic radar receiver or a radio astronomy science module. The radio design is then presented, both the core digital, power, and frequency hardware, and the specific RF modules that have been developed. Finally, the status and performance of the current UST Engineering Model (EM) development are presented, followed by conclusions and future plans.

2. UST ARCHITECTURE AND CONFIGURATIONS

Hardware Architecture

The UST hardware design uses a stacked module (or "slice") configuration. Components and circuit boards are grouped by function into modules, then horizontally stacked and interconnected to form the complete radio assembly. A rear raceway contains a flex harness for inter-module power and signal lines, and several coax cables along the raceway and in the front of the unit route the inter-module RF signals.

All UST configurations start with the same bottom two modules. First, a Digital Processor Module (DPM) provides all the digital interfaces with the spacecraft, handles the UST's housekeeping functions and telemetry collection, and performs the baseband processing on all transmit and receive signals. Next, a Power Supply Module (PSM) connects to the unregulated spacecraft power bus to convert to and distribute secondary voltages to the other modules. The PSM also contains a Temperature Compensated Crystal Oscillator (TCXO) and distributes this main frequency reference to other modules. The PSM can alternatively be configured to accept and distribute a frequency reference from an external Ultra Stable Oscillator (USO).

Both the DPM and PSM were designed with expandability in mind and are capable of supporting RF modules with up to three transmit frequency bands and two receive frequency bands, as well as providing power to an external amplifier, LNA, and switch network. UST RF modules have been developed that support S-, X-, and Ka-bands, and the UST is compatible with the heritage UHF RF module from the Electra proximity radio. The desired set of RF modules can simply be stacked above the DPM and PSM and integrated into the unit. Then appropriate software and firmware can be loaded into the DPM to support the desired communication links and protocols.

Transponder Architecture

An important consideration in a software-defined radio transponder is the carrier tracking and turnaround approach. A purely analog carrier tracking and turn-around approach was ruled out due to the lack of flexibility and limited frequency agility. The Electra radio family uses a purely digital tracking and turn-around approach, with the RF module simply acting as a block downconverter and upconverter. However, this approach does not provide optimal phase noise performance because of the limited digital tuning range, which requires either fractional PLLs or a low frequency reference for the LO synthesizer in order for full frequency tunability. As an example, the Electra radio must divide its ~33 MHz frequency reference down to ~56 kHz in its RF synthesizers, which degrades phase noise performance.

The best transponder architecture was determined to be a hybrid digital/analog approach [6] with a direct digital synthesizer (DDS) tuning the RF downconverter and upconverter synthesizers. This allows the digital modem processor to track the received carrier via the final downconverter stage and tune the transmit frequency to maintain a desired turn-around ratio. Any additional up- or downconverter stages are simply block converters using the fixed TCXO reference. A block diagram of this architecture is shown in Figure 2.

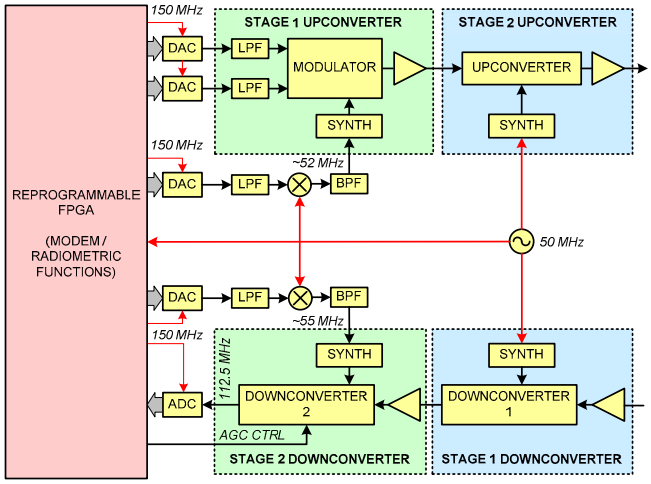

Figure 2 - UST Transponder Architecture Diagram

In order to optimize the phase noise performance, the DDS signals are mixed with the 50 MHz TCXO signal, rather than directly providing references for the synthesizer. As the DDS signals have higher residual phase noise than the TCXO signal directly, by mixing the DDS signals from ~5 MHz to

~55 MHz for the receiver and from ~2 MHz to ~52 MHz for the transmitter, the two-way and one-way transmit phase noise is improved. This can be seen in the simulated phase noise comparison of the UST baseline architecture and a case with the DDS fed directly into the synthesizers, shown in Figure 3. For frequency offsets out to 1 MHz, the baseline architecture provides ~20 dB improved performance.

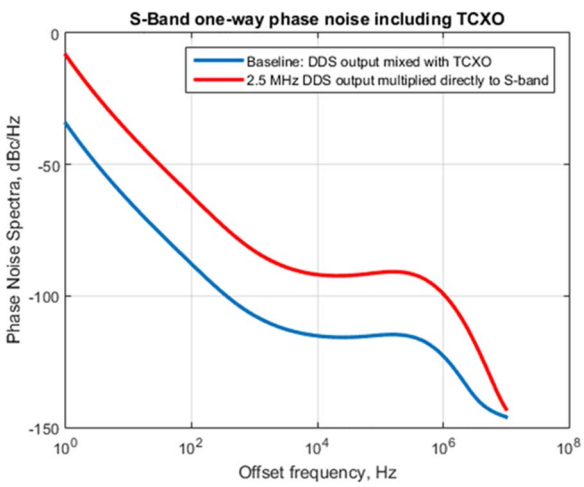

Figure 3 - Simulated Phase Noise Performance

Another UST architecture consideration was the approach for transmission at multiple frequencies. Being a modular architecture, the RF electronics can be optimized in order to provide multiple frequencies from the same slice by modulating the lowest frequency carrier and translating to higher frequencies using one or more upconverting mixers. This architecture requires that all RF outputs produce the same modulated data and typically finds the most use in radio science applications or for missions that require multiple RF links that are not operated simultaneously. A block diagram of this approach is shown in Figure 4.

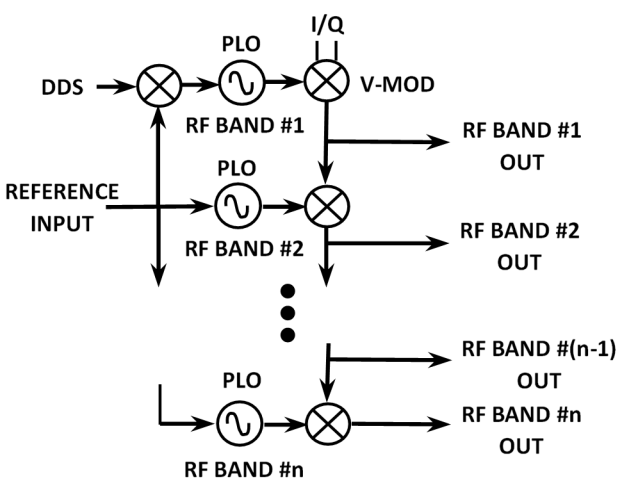

Figure 4 - RF Exciter Superheterodyne Architecture for Multi-Frequency Applications

If an application requires independent exciters to operate simultaneously with different IQ digital waveforms, this would require an architecture with independent direction modulation for each RF band, as shown in Figure 5. An application for this approach may be one in which the user would want to transmit to another spacecraft via a relay link and simultaneously downlink data to Earth.

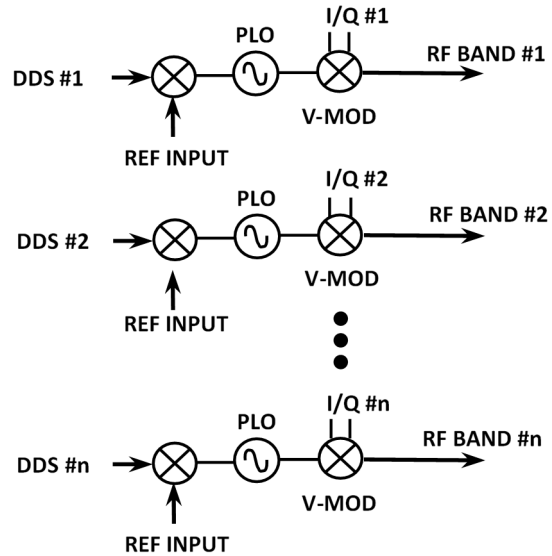

Figure 5 - RF Exciter Direct Modulation Architecture for Independent Multi-Frequency Applications

UST Configurations

With the flexible architecture of the UST, many hardware configurations are possible. A single frequency configuration (either S-band or X-band) is shown in Figure 6, and Figure shows a more elaborate configuration supporting receive at X-band and transmit at both X-band and Ka-band, as well as UHF transmit and receive for a proximity link. In addition, within a supported frequency band, simultaneous multi-channel operation is possible, as discussed in [7]. A full set of specifications for the range of UST configurations is presented in Table 1.

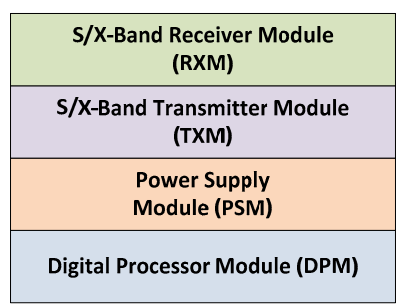

Figure 6 - Single Frequency UST Configuration

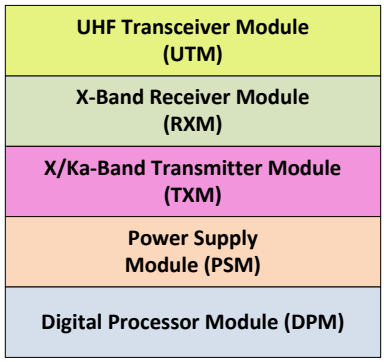

Figure 7 - Example Multi-Frequency UST Configuration

Table 1 – UST Specifications

TX/RX Specs	
TX Frequencies	UHF (390-450 MHz) S-band (2200-2300 MHz) X-band (8400-8500 MHz) Ka-band (25.5-27 / 31.8-32.3 GHz)
RX Frequencies	UHF (390-450 MHz) S-band (2025-2120 MHz) X-band (7145-7235 MHz) Ka-band (34.2-34.7 GHz)
TX Data Rates	10 bps – 300 Mbps
RX Data Rates	7.8125 bps – 37.5 Mbps
TX/RX Modulations	PCM/PSK/PM with Subcarrier PCM/PM with Biphase-L BPSK/QPSK/OQPSK GMSK/RRC pulse shaping Higher Order PSK/QAM
TX/RX Channel Coding	Convolutional RS/Turbo/LDPC Concatenated RS & Convolutional
TX Output Power	+12 dBm
Noise Figure	< 3.2 dB (S/X/Ka-band), < 3.9 dB UHF
Interface Specs	
Mass	4.3-5.4 kg for Single Frequency Band 5.4-7.6 kg for Multiple Frequency Bands
Volume	20 x 25 x 11-14 cm Single Frequency Band 20 x 25 x 14-18 cm Multiple Frequency Bands
Power Consumption	45 W for Single Frequency Band 50-65 W for Multiple Bands
Cmd/Tlm Interface	1553, RS-422, or Spacewire
High Speed Data Interface	LVDS (400 Mbps input, 100 Mbps output)
Power Interface	22-36 V Unregulated Bus
Environmental Specs	
Flight Allowable Temperatures	-20° to +50° C
Mechanical Environments	12.9 grms Random Vibration 2000 g Shock
Radiation	50 krad

Radio Science Expandability

Two additional RF modules are in development that could add advanced radio science and astronomy capabilities to the UST. An uplink bistatic radar receiver and a low-frequency planetary emissions receiver modules will exploit the UST's modular architecture in order to expand science capabilities beyond the standard transponder radio science, providing a low-cost standard telecom payload option with significant science signal processing capability to any mission.

The UST with an uplink bistatic radar receiver module can process dual-polarization signals at both UHF and S-band. Working with extremely powerful ground-based radar transmitters, such as the Arecibo Observatory and the Goldstone Solar System Radar, the UST can probe the surface and sub-surface layers of a planetary body, enabling investigations of surface roughness and subsurface composition, including the presence of volatiles. At UHF, uplink bi-static radar can be used to investigate regolith layering at 10's of meters depth, and at S-band, fine details of surface roughness and dielectric structure of the very top layers of the regolith can be determined.

The UST with a planetary emissions receiver module can capture radio emissions in the range of 10 kHz to 50 MHz, producing raw waveforms or spectrally processed data. With three orthogonal antenna inputs, the UST is also capable of determining source direction and polarization. The UST aboard missions to the giant planets (particularly Jupiter, which has the most complex and strongest family of radio emissions) could allow very affordable science investigations of the planetary radio emissions and the magnetosphere interactions that cause them.

The initial designs of these radio science modules have been completed and are being used to build and test prototype hardware by 2018. This could enable future space missions that may not otherwise have the resources for a standalone instrument to collect planetary emissions or perform bistatic radar observations through the use of a UST for both telecom and science purposes.

4. Radio Design

Digital Processor Module (DPM)

The core of the UST is the Digital Processor Module (DPM), an in-flight reprogrammable slice, which offers digitally-implemented modulation and demodulation functions, provides standardized link layer protocols, manages interfaces with the spacecraft avionics, and implements overall payload control. The DPM consists of two circuit board assemblies – the General Processor Module (GPM) and the Signal Processor Module (SPM) – that communicate over two board-to-board connectors. A high-level functional diagram of the DPM is shown in Figure 8.

To achieve the software-defined-radio (SDR) architecture, the DPM incorporates two key reconfigurable elements: a

Payload Controller (PC) based on a radiation-hardened 32-bit SPARC V8 Microprocessor and a Modem Processor (MP), which is implemented using a radiation-hardened space-grade Xilinx Virtex-5 reprogrammable FPGA. In addition, the DPM includes a Housekeeper (HK), which is a radiation-tolerant one-time programmable Actel/Microsemi RTAX-S FPGA, along with a substantial amount of dynamic and static memory.

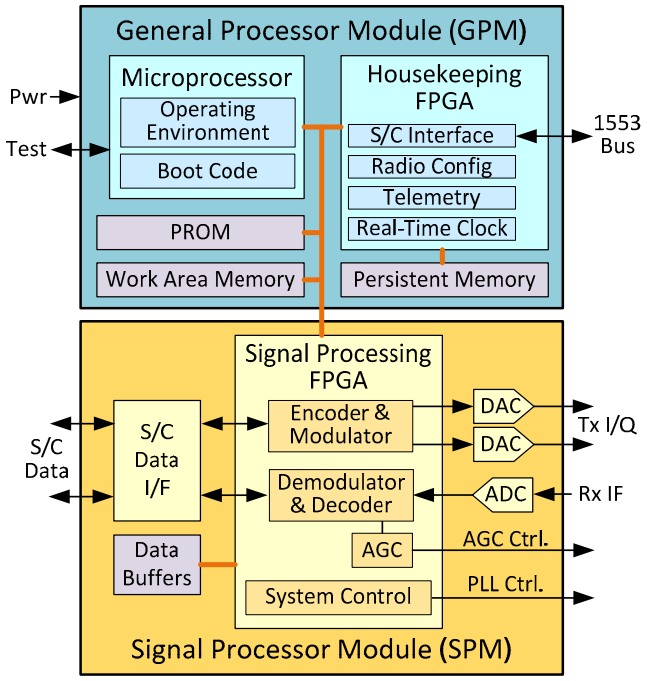

Figure 8 – UST Digital Processor Module Functional Diagram

Conceptually, one side of the DPM handles the spacecraft interfaces, which include MIL-STD-1553B interface, managed by the PC with the 1553 protocol logic housed inside of the HK FPGA interfacing with an industry-standard dedicated 1553 transceiver IC. The 1553 interface is the primary command and low-rate telemetry interface to the host spacecraft. In addition to the 1553 interface, the DPM also supports higher rate spacecraft command and telemetry interfaces, including SpaceWire over LVDS or RS-422 based serial protocols, which allows for speeds up to 200 Mbps. Three available optocoupler discrete inputs to the DPM could be used to receive direct commands from the spacecraft, such as Power-On Reset (POR) or a variety of other synchronization signals that may be required. A high-rate data input and output interface to the Solid State Recorder (SSR) is achieved via the MP PFGA interfacing to several LVDS transceivers. The DPM allows for dual-channel redundant LVDS interfaces, with up to four input data lines per channel from the SSR for burst rates up to 600 Mbps and a single data line per channel to the SSR for burst rates up to 150 Mbps. An LVDS flow-control line to the SSR is also available to facilitate handshaking and add robustness to the SSR to DPM data interface.

The other side of the DPM handles the interfaces to other slices of the radio stack, including controls for the Power Supply Module (PSM) and the RF modules. The Housekeeper FPGA provides the primary means for control and management of telemetry signals to and from the UST front-end, and the Modem Processor FPGA encodes and digitally modulates data from the SSR and provides I/Q and Direct Digital Synthesis (DDS) channels out to the RF slices as well as receives the digitized Intermediate Frequency (IF) – at 112.5 MHz – for demodulation and decoding. The DPM also provides a suite of differential and single-ended general purpose or spare inputs and outputs that are not being utilized in the existing design, but provide means for growth to meet future mission requirements while minimize cost and schedule associated with NRE.

The Modem Processor employs a register based Payload Controller interface, which allows for real-time reconfiguration of various features of the FPGA. Due to the ample variety of resources available inside the Xilinx Virtex-5 FPGA, the MP supports simultaneous dual-band modulation and demodulation functions as well as performs most of the signal processing at channel symbol rates up to 150 Msps and data rates up to 300 Mbps. The modulation chain within the FPGA includes a variety of the latest CCSDS compatible encoding implementations (e.g. scrambler, differential encoder, Reed Solomon, Turbo, convolutional, and LDPC encoders) with modulation techniques ranging from residual carrier BPSK without or without a subcarrier to QPSK and other higher-order modulations for increased bandwidth efficiency, DOR Tone modulation, ranging, and carrier turnaround. The final stage in the MP modulator also includes high-rate I/Q gain and offset adjustment logic, which facilitates fine tuning of the RF transmitter front-end for more effective carrier suppression and image rejection. The digital I/Q channels from the MP are fed into the on-board 10-bit Digital to Analog Converters (DAC) before interfacing to the RF transmitter module. Conversely, the 112.5 MHz receive IF is fed into the on-board 14-bit Analog to Digital Converter (ADC) from the RF receiver before entering the MP's demodulation and decoding chain. The MP is able to receive an equally broad range of modulations and encodings. The demodulation chain consists of a digital downconverter, carrier acquisition and tracking, subcarrier tracking, as well as symbol timing recovery and tracking. Recovered symbols are then fed into the MP's decoder block, where applicable CCSDS compatible decoders are enabled, including differential decoder, Viterbi decoder, LDPC decoder, and descrambler.

Along with bit stream data processing, a suite of link protocols, such as CCSDS Proximity-1 protocol for relay communications or NASA Deep Space Network (DSN) for direct-to-Earth communications, is implemented using a combination of software and firmware partitioned in such a way to minimize complexity and maximize throughput and performance. For example, the MP detects Proximity-1 receive frame boundaries, but the PC, for both forward and return links, takes care of data framing and assembly of

proper Proximity-1 headers as well as generating ACKs/NACKs for the incoming frames as necessary.

For operation in the long-term spaceflight environment, the DPM has several layers of built-in protection from radiation-induced SEUs. Extensive EDAC protection, inherent radiation hardness of critical low-level parts, and periodic "scrubbing" of the MP to eliminate any SEUs, which might affect the Xilinx FPGA configuration during operation, all combine to ensure that the UST can maintain basic functionality and reprogrammability for recovery, even in the face of severe SEU activity.

Photos of the DPM are shown in Figures 9 and 10 with key components labeled.

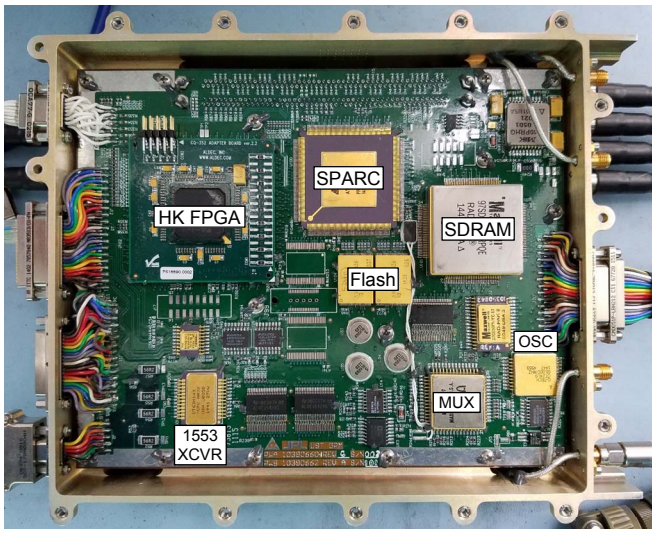

Figure 9 – EM DPM Slice Top (GPM PWA Side)

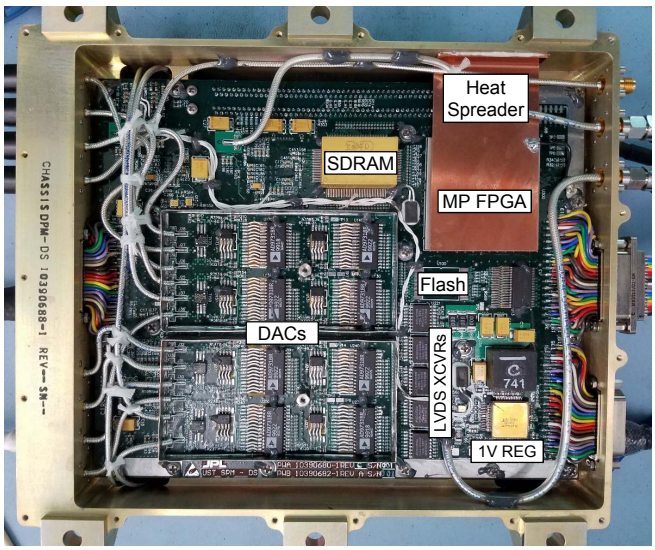

Figure 10 – EM DPM Slice Bottom (SPM PWA Side)

Firmware and Signal Processing Overview

A functional block diagram of the UST demodulator is depicted in Figure 11. The demodulator comprises the wideband front-end Analog Gain Control (AGC) interface module, the Digital Downconverter (DDC) and decimation stages, the Carrier Tracking Loop (CTL), the Subcarrier Tracking Loop (SCTL), and the Symbol Tracking Loop (STL). In addition, complex baseband turnaround ranging data is split off from the digital downconverter and passed over to the modulator (described subsequently) after filtering and scaling by a digital AGC. The master clock frequency is 150 MHz, and the typical intermediate frequency (IF) input is centered at 112.5 MHz.

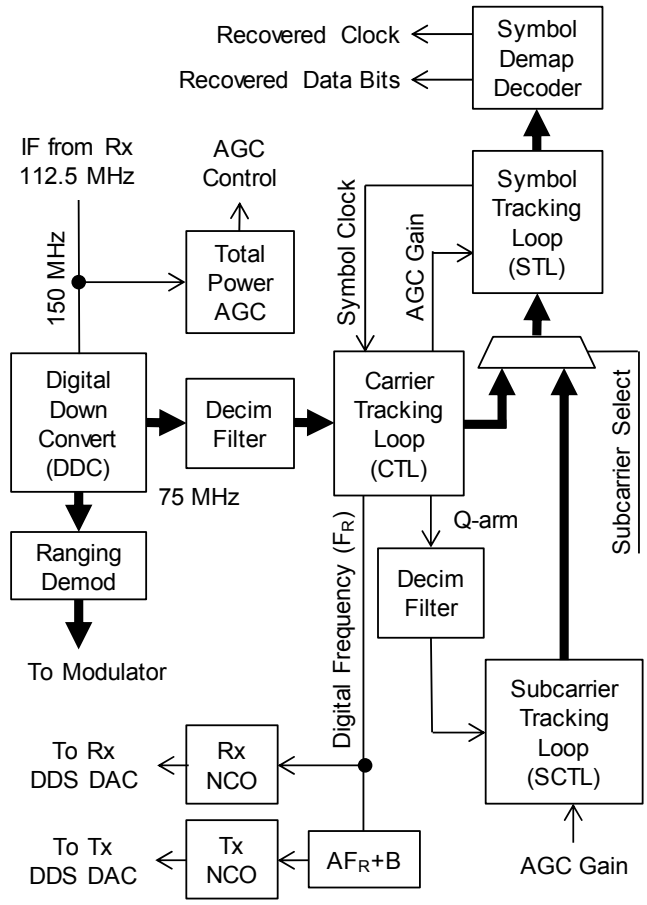

Figure 11 – UST Demodulator Implementation

In order to maintain an optimal signal power level at the ADC input, the wideband AGC controls the voltage level input to the ADC with a control signal generated digitally in the FPGA. The digital downconversion and decimation are performed on the input data from the ADC as shown in Figure 11 and reduce the sample rate by powers of 2, i.e., $f_s \equiv 75\,\mathrm{MHz}/2^{\ell}$. The UST CTL is designed to track the frequency and phase of the received carrier. The carrier portion of the signal can be suppressed or residual carrier BPSK, suppressed carrier QPSK or unmodulated (other

modulation formats are possible but have not been implemented). The CTL is based on a second-order loop design with accumulator and subsample arm filters. In the case of carrier modulated BPSK or QPSK data, the arm filters are timed by the symbol clock derived from the symbol tracking loop. In the unmodulated carrier case, a fixed clock, which is a submultiple of the ADC clock, is used to drive the CTL arm filters. The CTL is fully programmable (loop bandwidths, arm gains, etc.) and incorporates a digital AGC to regulate the loop bandwidth. Furthermore, the output of the digital AGC is distributed to the subcarrier tracking loop, with appropriate scaling to accommodate the modulation index, as well as to the symbol tracking loop for gain control. The frequency word output from the CTL drives the receiver digital Numerically Controlled Oscillator (NCO) circuit. The NCO output, in turn, is converted to an analog waveform via the DAC and used to generate a coherent LO for down-mixing the RF input to IF.

Similar to the CTL, the UST SCTL is fully programmable, second order, and is used to track out the subcarrier (nominally 16 kHz offset from the carrier). The subcarrier portion of the signal can be either suppressed or residual carrier BPSK. The symbol tracking loop is based on an early-late gate architecture and can be programmed for either BPSK or QPSK modulated waveforms. The symbol demapper and decoder depicted in Figure 11 are standard functions and thus are not discussed here.

The UST modulator architecture is depicted in Figure 12. The modulator is fully programmable and accommodates several different transmission modes including direct carrier modulation, subcarrier modulation, differential one-way ranging (DOR) tones, as well as sequential ranging turnaround. The latter utilizes the 75 MHz, complex baseband output from the digital downconverter (Figure 11) and filters this data with either wideband (6-7 MHz) or narrowband (2-3 MHz) lowpass ranging filters. A digital AGC (independent of the digital AGC in the CTL) is applied to this filtered data and, after scaling by the ranging modulation index factor, fed to the modulator as shown in Figure 12.

The digital in-phase and quadrature signals are then filtered and conditioned to minimize various spurious products and fed to the DACs. The in-phase and quadrature DAC outputs are mixed to S-band via a vector modulator in the RF modulator slice. The LO port of the vector modulator is also driven by the output of the transmitter NCO. The scale factor A together with the offset factor B are applied to the receiver digital frequency from the CTL for coherent two-way operation. For one-way operation, a fixed frequency offset is routed to the transmitter NCO instead.

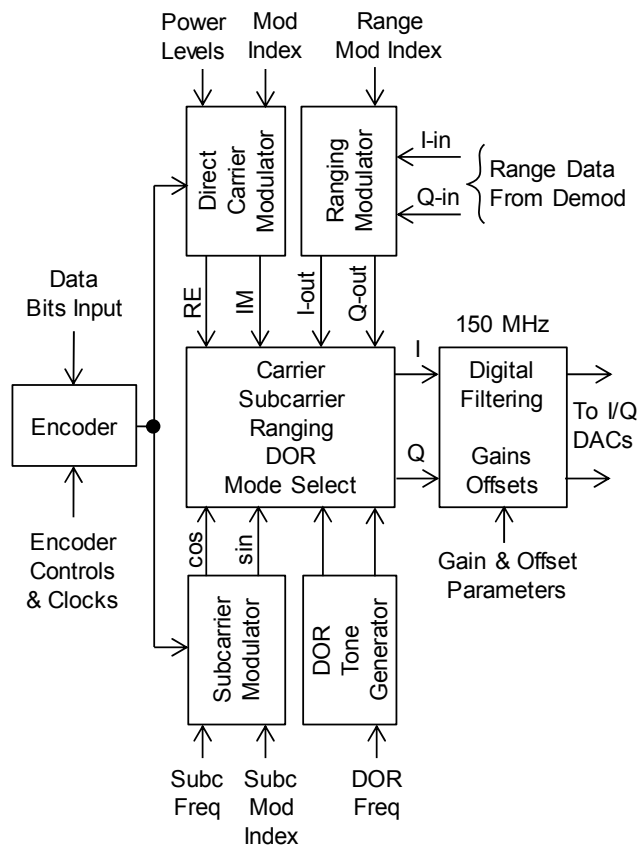

Figure 12 – UST Modulator Implementation

Software Overview

The Space Telecommunications Radio System (STRS) architecture for software defined radios [4] provides a common, consistent framework for hardware abstraction of complex reconfigurable and reprogrammable radio systems. The standard calls for generalized and modular hardware designs, and provides an open architecture design to accommodate the various mission-specific needs envisioned by NASA missions. The UST software is primarily developed in accordance with a software management plan that adheres to the STRS platform.

The UST comprises of two main modes of software operation, transitioned by commands or resets to the unit. Figure 13 provides a simplified software mode transition diagram. In a reset or power-on condition, the Boot Code Software (BCSW) is loaded to the SPARC processor from the on-board one-time programmable PROM, and the UST is brought to a pre-defined safe state. The BCSW is an interrupt-based, single-threaded application that interacts directly with the hardware peripheral devices in order to provide full command and control of the unit, collects and reports engineering telemetry for health and safety, configures and programs the signal processing hardware, and also performs built-in self-tests for debugging and troubleshooting purposes. It is in this mode that the software and signal processing functions (outside the context of the

BCSW) can be reconfigured and reprogrammed to provide post-launch in-flight changes to the UST. Operating out of the PROM is also commonly referred as the Safe Mode. In case of a fault, the Safe Mode could be used as a recovery console to reprogram or correct the configuration of the DPM as necessary.

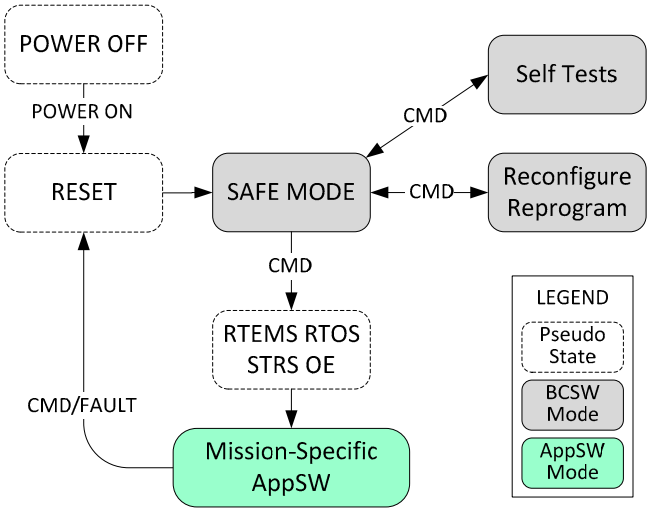

Figure 13 – UST Software Mode Transition Diagram

The BCSW developed for the UST is baselined from various successful JPL flight radio designs such as the Electra units for MRO/MAVEN, the CoNNeCT SDR as part of NASA's Space Communications and Navigation (SCaN) testbed, as well as the Digital Electronics Assembly of the Terminal Descent Sensor of the Mars Science Laboratory. Commands supplied via the 1553 bus interface (or serial debug interface, and in the future, the SpaceWire interface) will allow the UST to transition to an STRS Application Software (AppSW) mode, where mission-specific signal processing needs can be loaded and executed.

In the STRS AppSW mode, the POSIX-compliant application layer specific to the UST is executed on top of the STRS Operating Environment (OE). For example, the AppSW for a UST intended for direct-to-Earth communications and navigation would require, on top of the basic BCSW features, configuring the signal processor parameters to the desired data rates, channel coding types, and modulation schemes. The STRS OE provides standardized multi-platform features through Application Program Interfaces (APIs) that initialize and configure the hardware platform as well as provide controls for file/memory handling. An Operating System (OS) is also an integral part of the STRS OE, and the Real-Time Executive for Multiprocessor Systems (RTEMS) Real-Time OS is built to provide the fast, low overhead context switching and deterministic scheduling mechanism.

The developed software codes are mostly written in C/C++ with some assembly code. The code base is also highly memory efficient, and current memory utilization margins are over 90%, which allows for greater expansion capabilities and easier code upgrades.

Power Supply Module (PSM)

The PSM provides regulated secondary DC power to other UST modules, as well as distributes a frequency reference. The PSM design is based on a heritage architecture, with the spacecraft power bus passing through an EMI filter and then distributing to various DC/DC converters. Switches controlled by the DPM are on certain secondary powers, allowing the option of lower power modes with some RF modules powered off. Additionally, the bus voltage is routed through a controlled switch to an external connector. This allows the option of an external SSPA and switch network powered and controlled by the UST. The design is shown in Figure 14.

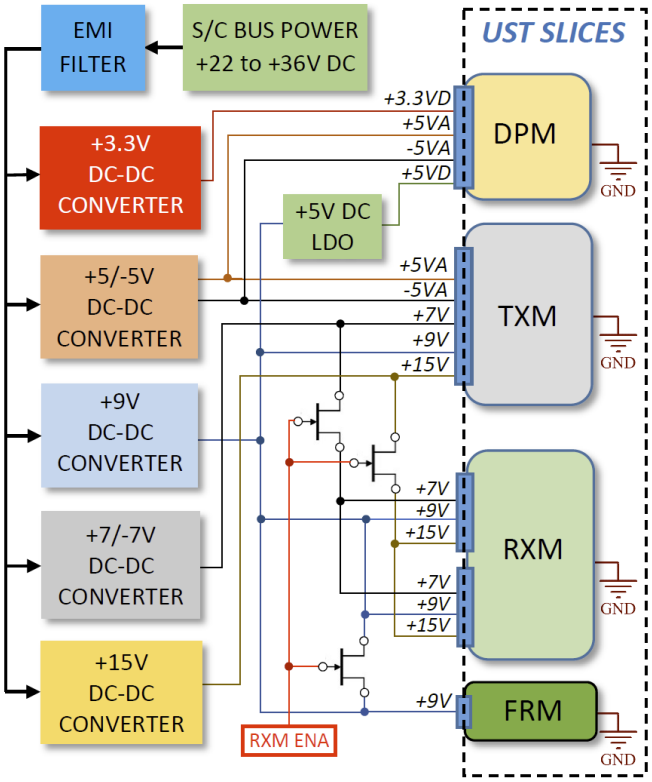

Figure 14 – UST PSM Block Diagram

The module has a split chassis design that places DC/DC converters and the frequency reference PWB on one side of a common floor and the power PWB on the other side. The assembled module is shown in Figure 15.

The frequency reference board is composed of a temperature compensated crystal oscillator (TCXO), a 4-way power divider, and power conditioning circuits. This provides the RF slices with a common reference for phase locking purposes and in some applications provides a clock to the digital processor module. A block diagram of the frequency reference board is shown in Figure 16 for a 50 MHz application.

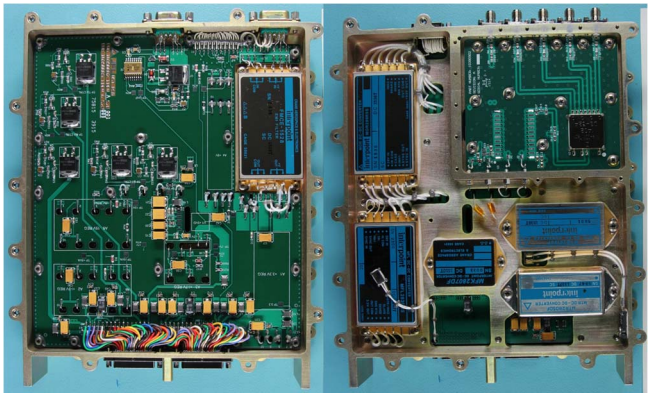

Figure 15 - Power Supply Module

The frequency reference board is designed to distribute either the on-board TCXO reference or a spacecraft provided Ultra-Stable Oscillator (USO) reference to the other UST modules. The selection of either source is done prior to flight using a select-in-test resistor network. The assembly is designed with the intent of supporting a broad frequency bandwidth of TCXO and USO options. A functional block diagram is presented in Figure 16

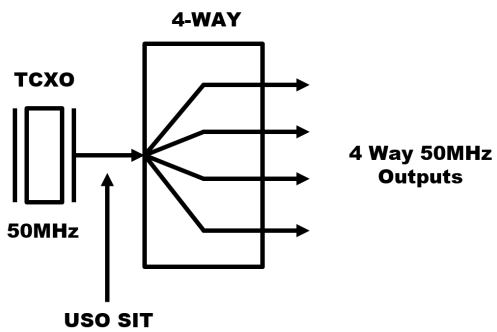

Figure 16 – Frequency Reference Board Block Diagram

The frequency reference board resides in an RF isolated cavity in the PSM chassis and utilizes high reliability, radiation hardened components. A plot of the phase noise using the built-in TCXO is shown in Figure 17.

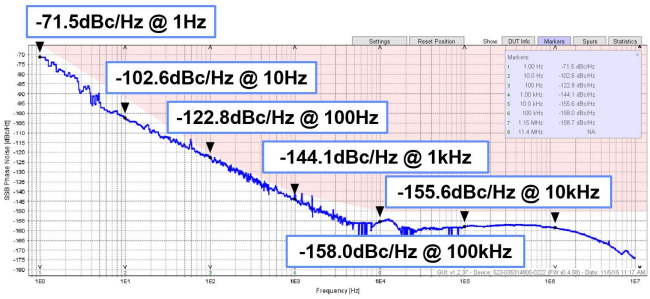

Figure 17 – FRM Phase Noise Test Results

S/X-Band Transmitter Module (TXM)

An S/X-band exciter module has been developed for the UST EM, and the block diagram for this module is shown in Figure 18. The 50 MHz TCXO input is actually fed to the exciter from the PSM, but shown here for clarity.

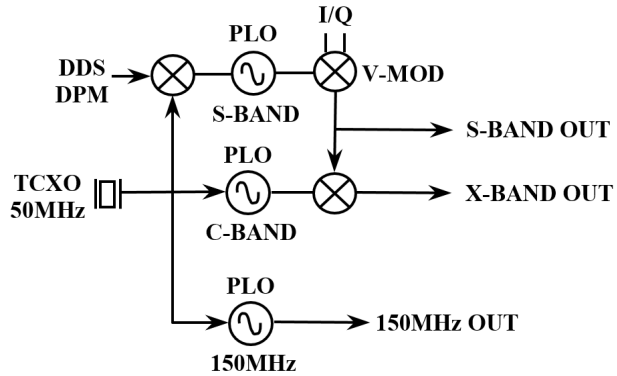

Figure 18 – UST S/X-Band Deep Space Multi-Function Module Diagram

The S/X-band exciter utilizes a superheterodyne architecture in which the S-band output carrier is modulated by in-phase and quadrature (IQ) digital waveforms from the DPM. The modulated S-band output then splits off to an output connector for S-band applications as well as the IF port of the X-band upconverter. The LO input of the up-converter is fed by a C-band phase locked loop (PLL) synthesizer. The X-band output is then amplified, filtered, and fed to the output connector. A 150 MHz PLL synthesizer feeds the digital processor module (DPM) clock input and is used for the FPGA processing and to provide a clock for the I/Q and DDS DACs. The reference input of the S-band PLL is a mixing product between the DDS signal from the DPM and the TCXO input from the PSM, while the C-band PLL and the 150 MHz PLL are phase locked directly to the TCXO input.

Both the S- and X-band exciters are packaged in one chassis and on one single printed circuit board (PCB) assembly. This approach was taken in an attempt to reduce the overall assembly cost and hardware volume. The top of the assembly contains the RF power conditioning and the 150 MHz PLL synthesizer. Figure 19 is a photograph of the top view of the assembly. The interconnection from the PCB to the SMA connectors is in the form of small press-in connectors, which allows for ease of testing at the board level prior to placing the board into the chassis.

A bottom view of the assembly is shown in Figure 20. The bottom of the PCB assembly contains the RF electronics including the S- and C-band PLL synthesizers and the X-band up-converter. In order to decrease crosstalk amongst the various circuits, the internal floor of the chassis is pocketed to help isolate circuits based on their functionality and noise sensitivity. Having all of the sensitive RF circuits packaged on the bottom side in this way removed the need to have any internal covers and reduced the number of machined metal parts.

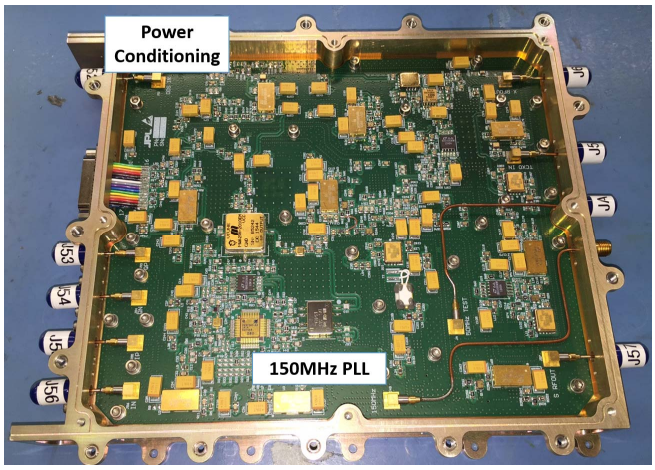

Figure 19 – UST S/X-Band Exciter EM Assembly (Top View)

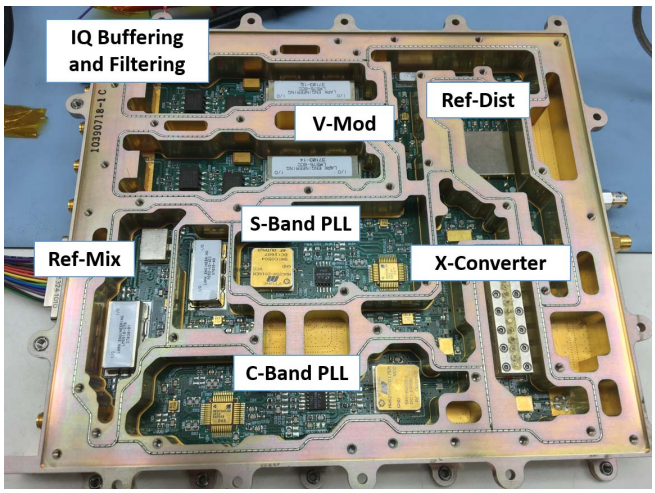

Figure 20 – UST S/X-Band Exciter EM Assembly (Bottom View)

The use of all SMT components avoids having exposed chip and wire assemblies at the PCB top assembly level which helps to ease the handling and foreign object debris (FOD) requirements. In order to realize an all SMT approach for this assembly, we utilized custom high frequency leadless chip carrier (LCC) modules from KCB Solutions [9]. One example of this was the X-band up-converter circuit. This MCM LCC contains the RF mixer, LO amplifier and RF amplifier MMICs in an SMT hermetic package as shown in Figure 21.

All of the components in the UST RF electronics are capable of meeting most deep-space applications. The components are selected to withstand a total ionizing dose (TID) of at least 100 krad (Si) and are single event effect (SEE) tolerant at a minimum. All parts are capable of being screened to Class S space level when applicable.

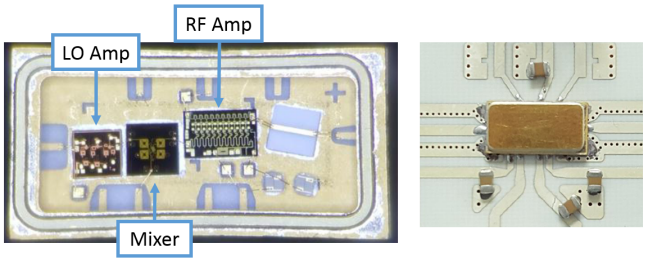

Figure 21 – X-Band Up-Converter MCM (Left) and Corresponding Assembled Evaluation Board [10]

S/X-Band Receiver Module (RXM)

An S/X-band receiver module has all been developed for the UST EM. It is a multifunction module composed of an X-band heterodyne double down-conversion to S-band and then to intermediate frequency (IF), a C-band programmable fractional phase locked loop (PLL) frequency synthesizer, and an S-band programmable fractional PLL frequency synthesizer. A simplified block diagram of the RXM is shown in Figure 22.

The X-band front end, after filtering and low-noise amplification of the input signal, downconverts the nominal 7190 MHz (+/- 45 MHz) input to a 2072.5 MHz (+/- 45 MHz) intermediate frequency. After additional filtering and amplification, the S-band signal is downconverted to the final IF of 112.5 MHz. The IF chain provides additional amplification and filtering along with the AGC function, controlled by the DPM, for setting the output level to the DPM – nominally at -6 dBm. The IF bandwidth is set primarily by the two SAW filters in the IF chain and is minimum IF +/- 19 MHz.

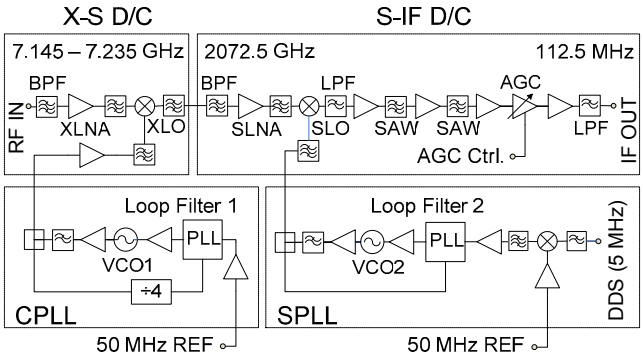

Figure 22 – RXM Multi-Function Module Block Diagram

The C- and S-band PLLs provide the local oscillator (LO) for the X- and S-band downconversion stages in the RXM. The reference 50 MHz input to the RXM is fed by the TCXO in the PSM. The C-band PLL synthesizer is phase locked to this TCXO input. For the S-band PLL synthesizer, the 50 MHz reference is mixed with the filtered DDS input (5 MHz +/- 100 kHz) from the DPM and the PLL is phase locked to the upper sideband of the mixed reference signal (55 MHz).

As part of the architectural evaluation, Agilent Genesys RF system tool was used for end-to-end performance predicts. ADS-Momentum and Sonnet were utilized for microstrip filter designs.

All of the components in the RXM were selected with the path to flight in mind in order to meet the reliability, radiation, and the RF performance requirements for most deep-space applications. The majority of components are selected to withstand a total ionizing dose (TID) of at least 100 krad (Si) and are single event effect (SEE) tolerant. The remaining few components should be capable of meeting these levels pending radiation testing.

In addition to parts reliability, the printed circuit board (PCB) assembly packaging approach was also based upon improving the overall reliability of the RXM assembly. For example, ceramic microstrip filters are installed directly in their associated PCB cavities, reducing the overall assembly complexity and improving the reliability (Figure 23). Other PCB components utilize standard surface mount technology (SMT) assembly processes.

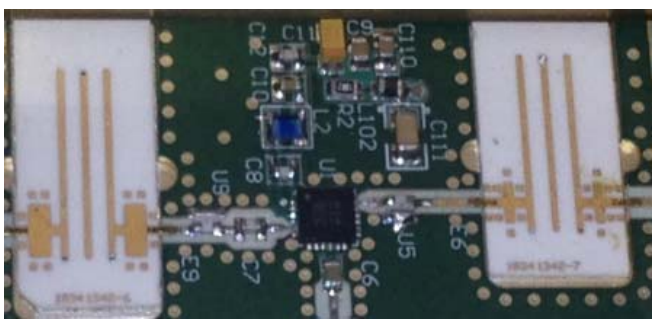

Figure 23 – RXM Ceramic Filter Assemblies

The top and the bottom views of the RXM chassis with all PWAs installed as well as the bottom side with the internal cover installed are shown in Figures 24, 25, and 26.

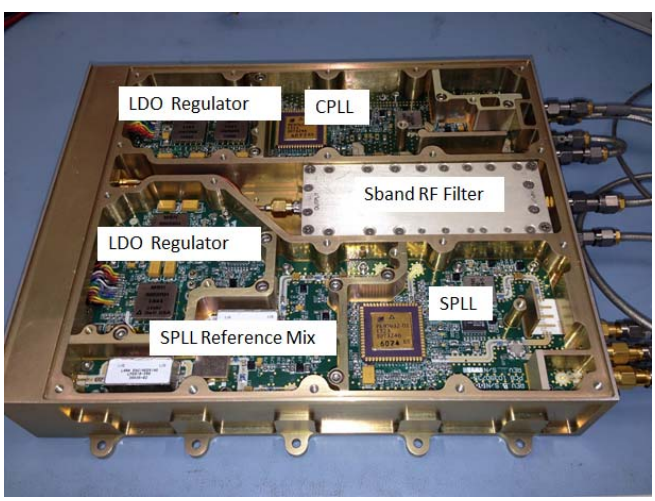

Figure 24 – RXM Slice Assembly (Top View)

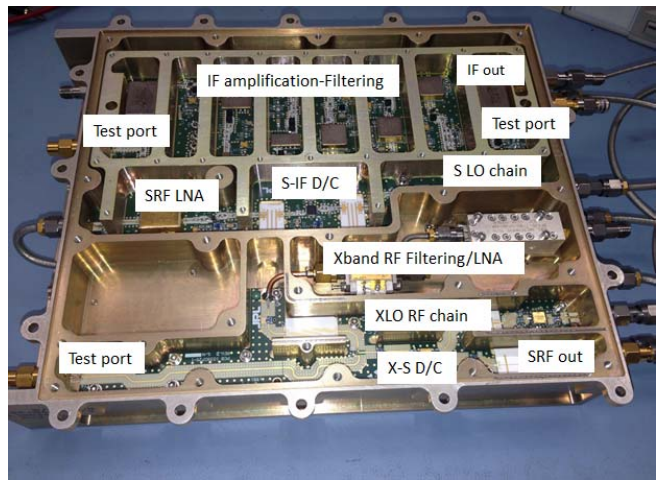

Figure 25 – RXM Slice Assembly (Bottom View)

In order to decrease crosstalk amongst the various circuits, channelization and internal isolation walls are utilized. An additional internal cover is also used in the S-band to IF section of the RXM.

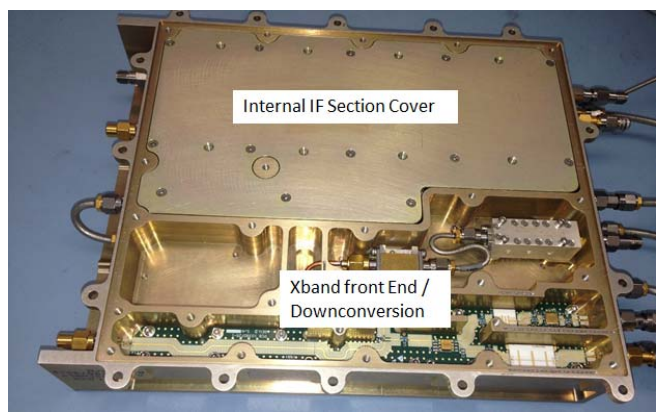

Figure 26 – RXM Slice Assembly (Bottom View) with Internal IF Cover

3. UST DEVELOPMENT STATUS

Two UST engineering modules (EM) units have been built and tested at JPL, and are considered to be at a NASA Technology Readiness Level (TRL) of 6. The first is a transponder that can operate in the deep-space or near-Earth frequency bands (see Figure 27). The RF transmit and receive modules have been developed using S-band as intermediate frequency for X-band in a manner that allows them to operating in either band, or even transmit in both bands simultaneously. The radio is frequency agile, even in-flight, and can be tuned across the entire deep-space and near-Earth frequency bands. The DDS architecture allows transponding with any desired turn-around ratio, while still providing excellent phase noise performance.

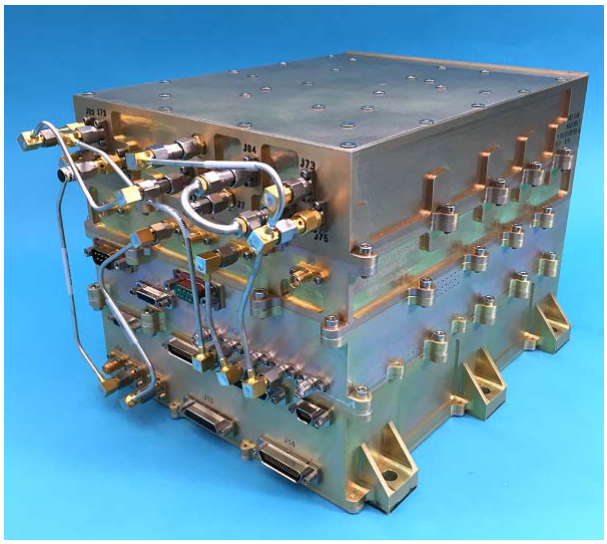

Figure 27 - UST S/X-Band Engineering Model

In this configuration, the UST supports transmit data rates from 10 bps to 150 Mbps and receive data rates from 7.8125 bps to 37.5 Mbps. It is fully compatible with the NASA Deep Space Network (DSN) and Near-Earth Network (NEN) signaling standards, and supports a wide variety of coding and modulation types. The receiver has a noise figure of 2.1 dB and a dynamic range of -152 to -60 dBm.

The second EM unit that has been developed is a high-rate modulator at near-Earth Ka-band (see Figure 28). Targeted towards Earth orbiters with extremely high data volume return requirements, it is capable of supporting transmit rates up to 1.74 Gbps with 7/8 rate LPDC encoding.

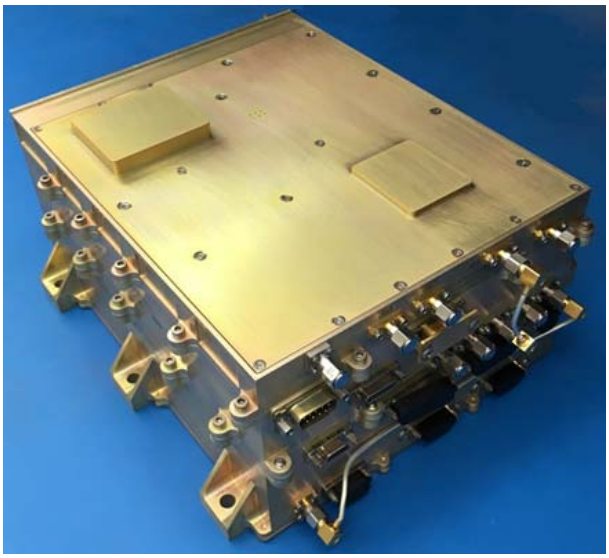

Figure 28 - UST Ka-Band Modulator Engineering Model

5. Conclusions and Future Plans

The modular architecture and reprogrammability of the UST product line allow it to provide a wide variety of radio services. It can support a variety of frequency configurations, including simultaneous in-situ relay and deep space link support, with improved modulation, coding and data rate capabilities. All data management, protocol, coding/decoding and modulation/demodulation functions are pre-launch and post-launch reprogrammable providing extensibility for special support scenarios.

Additional development work is planned with the current UST EM units. This includes the integration of a heritage UHF RF module to demonstrate simultaneous operations of a DTE X-band link and a UHF proximity link. A bistatic radar receiver and a low-frequency planetary emissions receiver are also in development and will demonstrate the ability to perform advanced radio science and astronomy with the UST.

Flight units of the near-Earth Ka-band modulator version of the UST are currently being built for the NASA-ISRO SAR (NISAR) mission, scheduled to launch by 2021. Additionally, a version of the UST supporting UHF, X-band, and Ka-band is currently baselined for NASA's Next Mars Orbiter (NeMO) concept.

6. References

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[9] KCB Solutions website: www.kcbsolutions.com

[10] Photo Courtesy of KCB Solutions

7. BIOGRAPHIES

Michael Pugh *received his M.S. in Electrical Engineering from University of Southern California and his B.S. from Harvey Mudd College. He has been with NASA's Jet Propulsion Laboratory since 2007 where he is a Telecommunications Engineer in the Spacecraft Reconfigurable Communication Systems group. He is the Cognizant Engineer for the UST EM development, as well the NISAR UST Ka-band Modulator, and served as System Engineer for the ExoMars TGO Electra payload.*

Igor Kuperman *is the supervisor of the Spacecraft Reconfigurable Communication Systems group at the Jet Propulsion Laboratory and has over 15 years of experience ranging from digital signal processing (DSP) design and analysis to FPGA development and implementation of DSP, coding, and other data processing algorithms. Mr. Kuperman received his M.S. from University of Southern California in 2005 and his B.S. from California State Polytechnic University, Pomona, in 2001, both in Electrical Engineering. Recently, he was the cognizant engineer for the digital subsystem of the MSL landing radar as well as the FPGA lead for the latest Electra UHF radio firmware deliveries for the MRO and MSL projects. Mr. Kuperman is currently serving as the Product Delivery Manager for the ExoMars Trace Gas Orbiter Electra communication subsystem and as the Task Manager for the Universal Space Transponder EM development.*

Fernando Aguirre *received a B.S. (2002) and an M.S. (2007) in Electrical Engineering from UCLA. He has been with NASA's Jet Propulsion Laboratory since 2008 where he is a Microwave Design Engineer in the Spacecraft Reconfigurable Communication Systems group. He has worked on hardware for various JPL flight and research projects. Most recently he is the RF Design Engineer for the UST exciter modules and the Frequency Reference Module. Prior to joining JPL he was a Microwave Engineer at REMEC Defense and Space where he designed microwave synthesizers and amplifiers for military applications.*

Hadi Mojaradi *received his B.S. (1980), his M.S. (1982), and his Ph.D. (1987) in electrical engineering from the University of California, Los Angeles. He has been with NASA's Jet Propulsion Laboratory since 1999 where he is a Senior RF Microwave Communication Design Engineer in the Spacecraft Reconfigurable Communication Systems group. He has worked on hardware for various JPL flight projects, including MRO, MSL, CoNNect, DSAC, MarCO, and DHFR. He is currently supporting RF electronics development for NISAR and M2020 projects.*

Carl Spurgers *received his B.S. and M.S. in Electrical Engineering from the University of Texas at Dallas with a focus in RF and microwave design. Prior to JPL, he supported digital and RF hardware design efforts for several military applications while at Rockwell Collins and L-3 Communications, including conformal composite UHF phased array antennas. He arrived at JPL in 2013 and has since supported a variety of programs including NISAR, SWOT, DSOC, FINDER, Mars ADT, Mars 2020 Rover, and Mars Helicopter Scout. Assignments include design of digital electronics for the NISAR UST – KaM radio, capable of downlinking data to earth over Ka-Band at 1 Gsps OQPSK, and piezoelectric transducer amplifier and receiver electronics for use in an acoustic modem to support down-hole wireless communications.*

M. Michael Kobayashi *received his B.S. (2006) and M.S. (2007) in Electrical Engineering from UC Irvine, and joined the Jet Propulsion Laboratory in 2007 as an RF Microwave Engineer. He has worked on various microwave flight hardware deliveries to MSL and SMAP, and has been involved in developing the Iris Deep-Space Transponder software-defined radio to support various JPL CubeSat projects such as INSPIRE, MarCO, and Lunar Flashlight. Recently, he has been involved in developing the digital slice of the UST, and system engineering for NISAR.*

Edgar Satorius *is a principal member of the technical staff in the Flight Communications Systems Section of the Jet Propulsion Lab. He performs systems analysis in the development of digital signal processing and communications systems with specific applications to blind demodulation, digital direction finding and digital receivers. He has published over 90 articles and holds two patents in the field of digital signal processing and its applications. In addition, he is an Adjunct Associate Professor at the University of Southern California where he teaches digital signal processing courses. He received his B.S. in engineering from the University of California, Los Angeles and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, California.*

Thomas Jedrey *received his B.S. in Mathematics from the University of Maryland, College Park, Maryland, in 1979. He received his M.A. in Probability and Statistics from the University of Maryland in 1982 and his M.S. in Electrical Engineering from USC in 1990. He worked at the U.S. Army Harry Diamond Laboratories and at Gould Electronic Systems before joining JPL in 1986. He led the successful development of the Electra Proximity Radio, and he is now the Deputy Manager of the Communications, Tracking and Radar Division at JPL.*

8. ACKNOWLEDGEMENTS

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