Jet Propulsion Laboratory
California Institute of Technology

Recent Advances in Commercial Memories and Potential Contribution to GN&C Miniaturization

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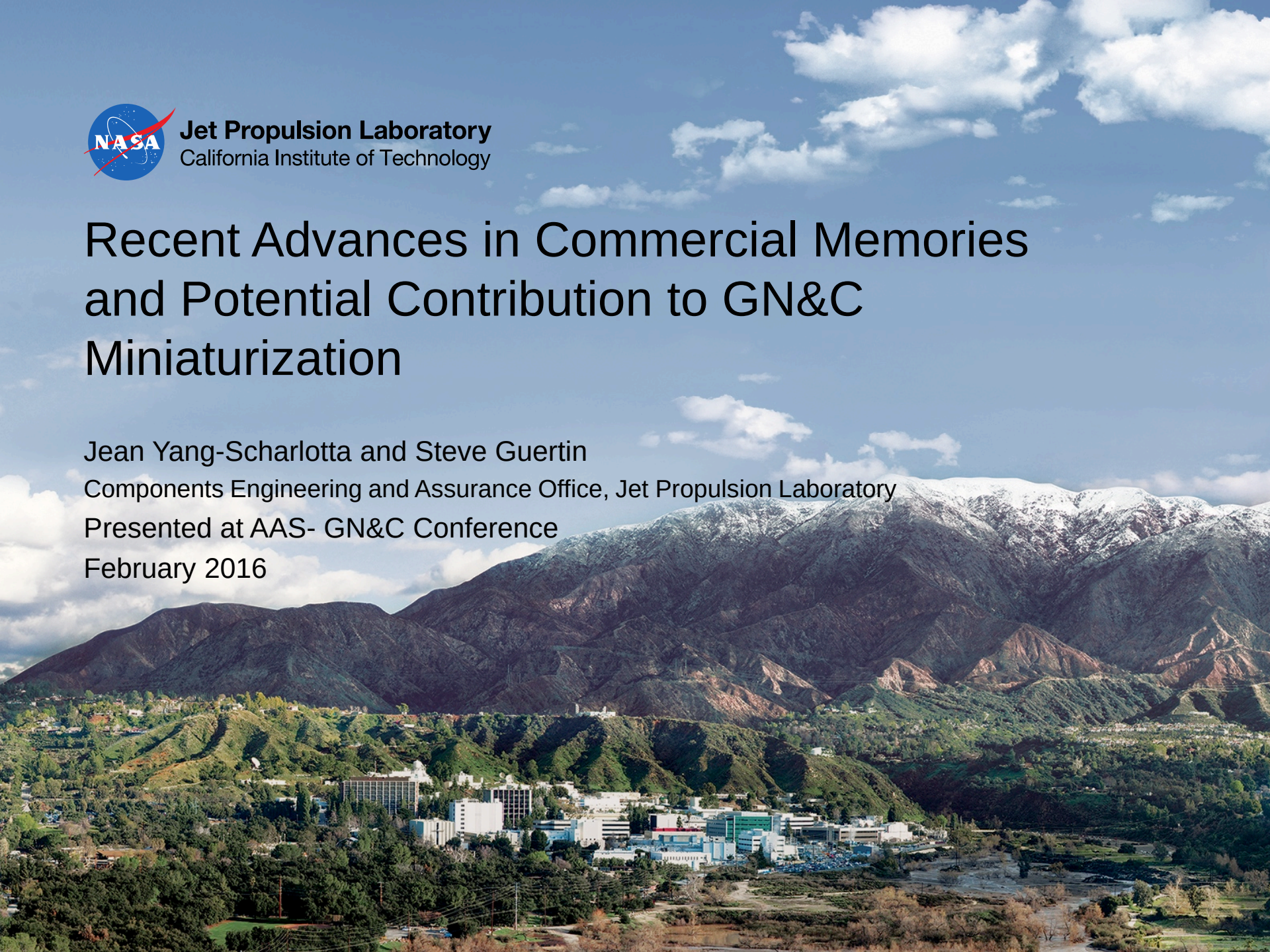
Presented at AAS- GN&C Conference
February 2016



Why DRAM and NAND?

- Competition in smart phones features have accelerated advancement in memory technologies
  - Cell phones today- capture pictures and videos, execute verbal commands, voice navigation information, full suite of entertainment
  - Cell phones 5 years ago- take pictures, play music
  - Cell phones 10 years ago- manual address book entry , text
- Mobile DRAM- LPDDR series enable higher density and faster data speed to be used for complex computing duties in handheld devices
  - 16Gb of LPDDR4 DRAM
- MLC/TLC NAND- high density storage of image and sound files benefit from storing multiple bits per cell.
  - 1Tb (128GB) of TLC NAND

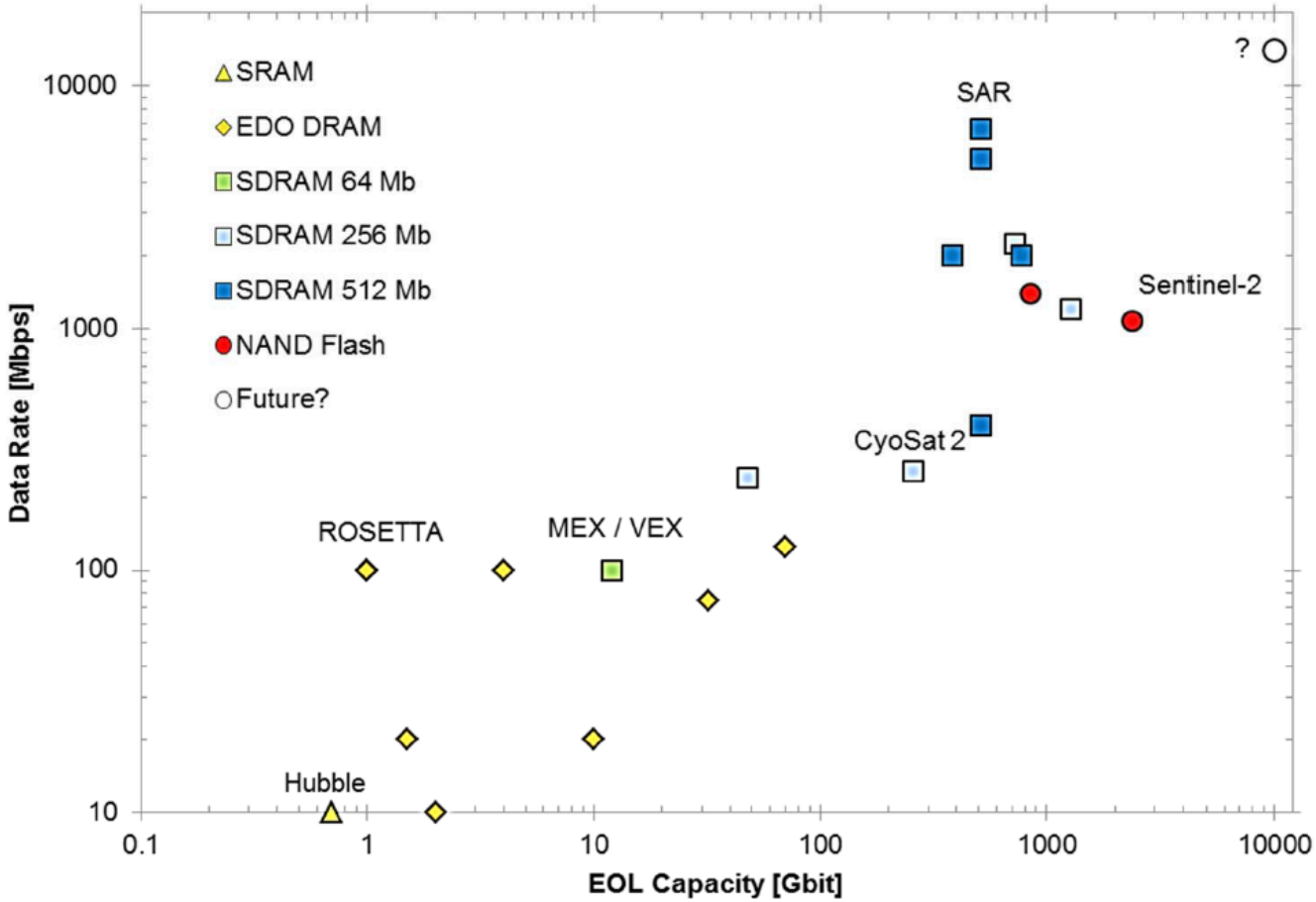
http://dayintechhistory.com

<u>Judicious use of consumer targeted technologies can bring huge capabilities to spacecraft</u>

Outline

- **Spacecraft Memory Uses**
- DRAM
  - Technology Trend
  - Performance Trend
  - Radiation and Reliability
- NAND
  - Technology Trend
  - Performance Trend
  - Radiation and Reliability
- Conclusion

Spacecraft Memory Use

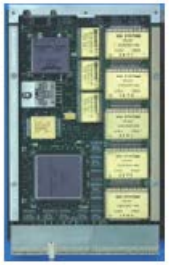


H. Schmidt, M. Hermann, and F. Gliem, "Radiation Hard Memory-Radiation Testing of Candidate Memory Devices for Laplace Mission," in CNES/ESA Radiation Effectc Final Presentation Days, 2015, March 10,.

- Both data capacity and data rate needs are Increasing: Tb and Gbps ranges needed
- Current SOA rad hard memories have densities of 10's of Mb

Memory Space Use Trends

- DRAM is primarily paired with processors
  - High data rate desired/required for next generation space processors
    - BAE Rad750 paired with SDR DRAM (up to 200MHz) lower power than rad hard SRAM, Rad5500 will be paired with DDR2/DDR3
    - NASA/Air Force High Performance Space Computing/ Next Generation Space Processor expected to be paired with high rate memory such as DDR3/4 or beyond
- NAND is primarily for solid state recorders
  - Store Flight data and instrument data
  - Buffer for smart radios
  - Data storage connected with processors
- Both needed to support computation and data intensive technologies:
    - Adaptive and autonomous systems
    - Hyper spectral imagers
    - High-rate RADAR
    - Image based navigation
    - Flash LIDAR



RAD750 3U

- TRL-9 since 2005
- 128 MB DRAM with SECDED and nibble ECC

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- **DRAM**
  - Performance Trend
  - Technology Trend
  - Radiation and Reliability
- NAND
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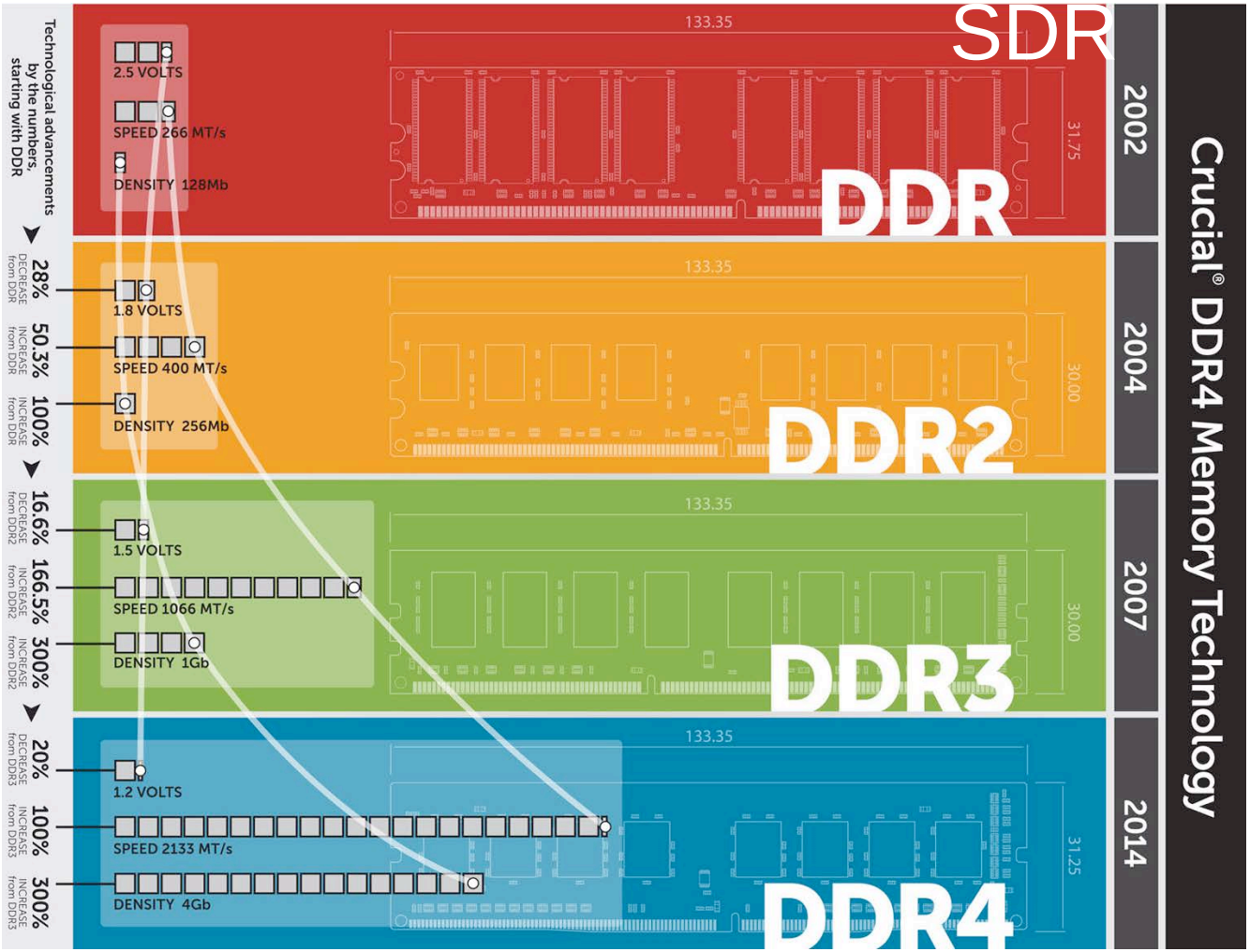
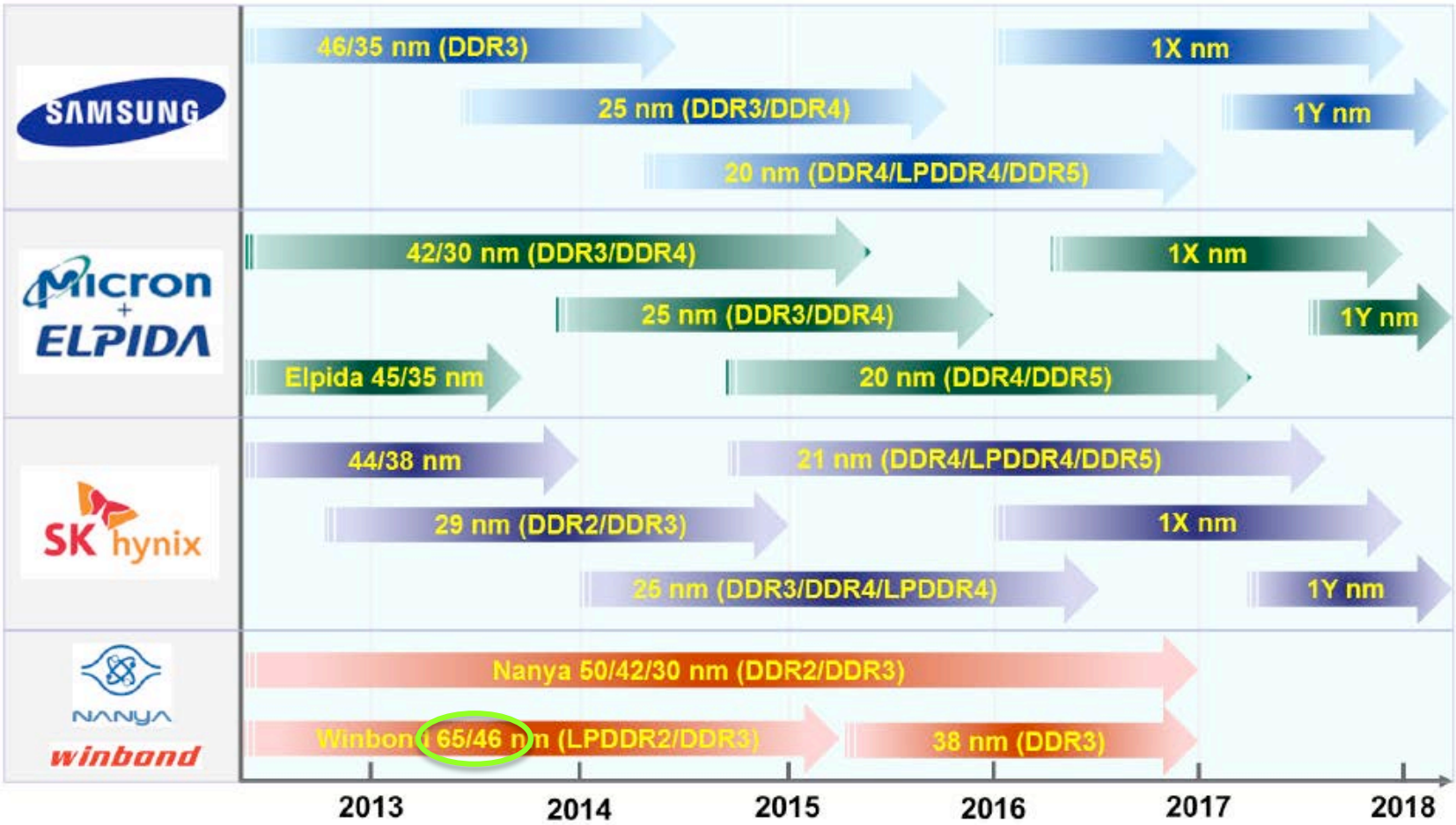
DRAM Performance Trend



www.crucial.com

- DRAM data rates have increased by 8x, capacity by 31x and supply voltage by 50%
- SOA rad hard processors are paired with single data rate (SDR) memory

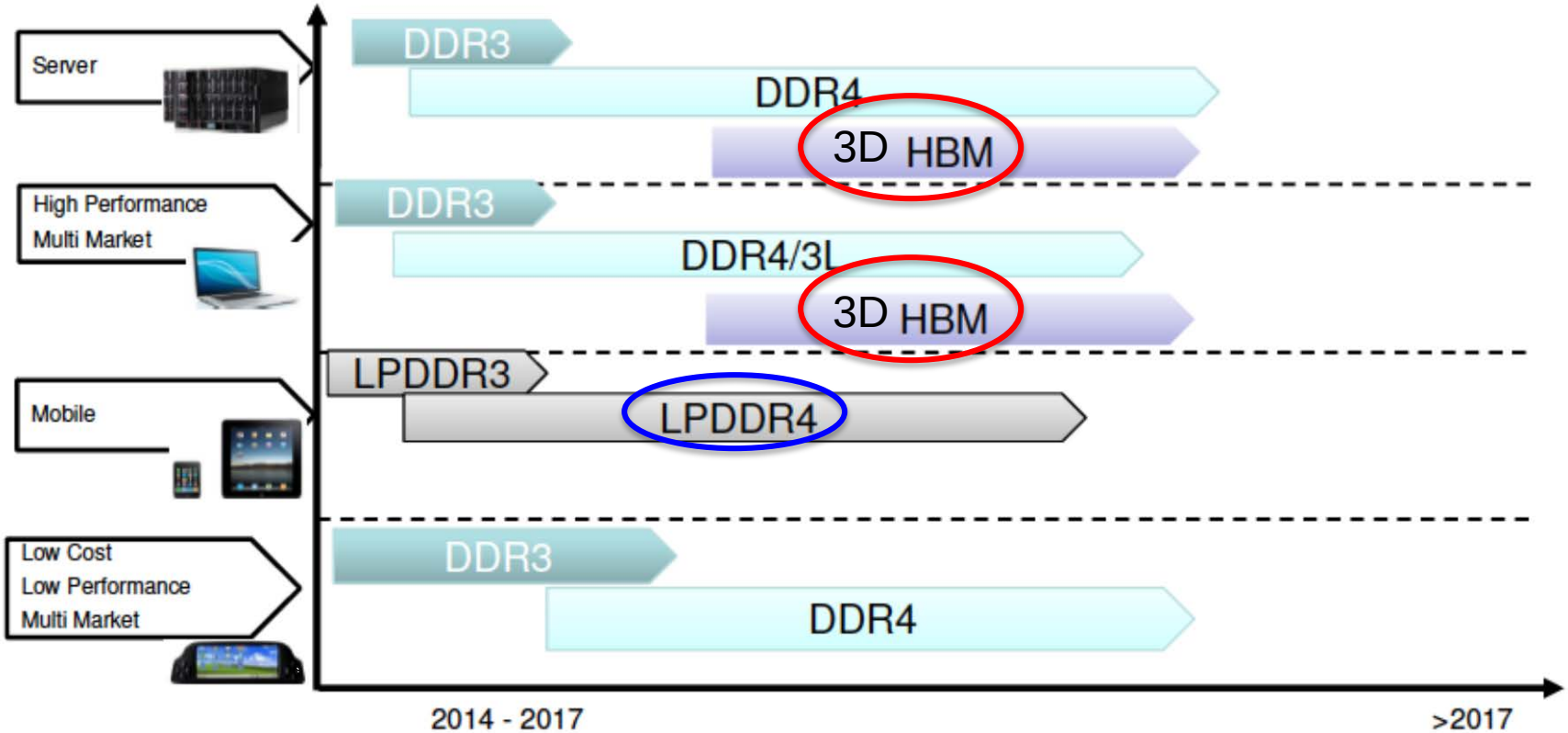
DRAM Technology Progression



http://techinsights.com

- DRAM has been more performance driven so technology progression 50nm-> has not been as aggressive as NAND

DRAM Technology Trend

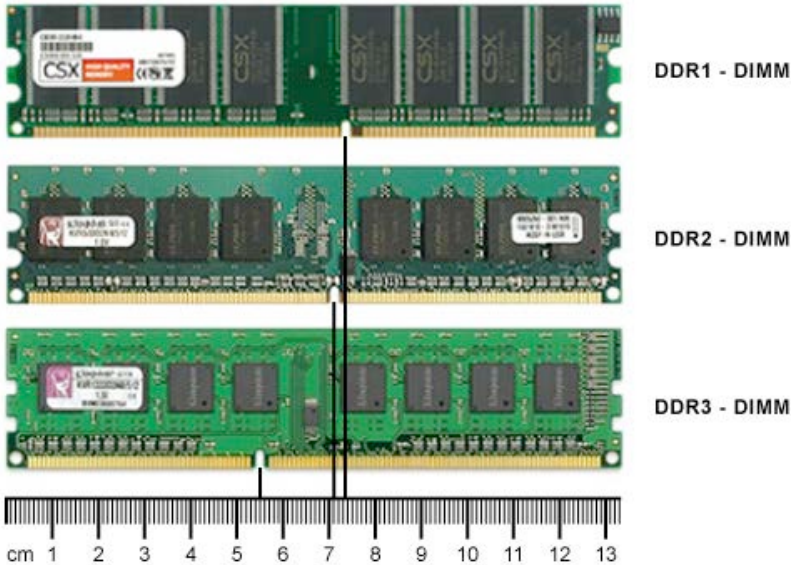


K. K. Yee, "Transitions : A Roadmap to Low-Power Memory A Look at History Last three decades – PC driven," MEMCon Presentation, October 15, 2014.

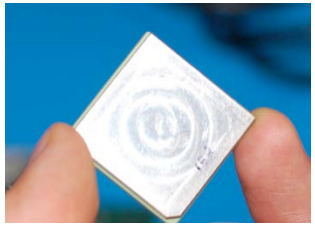
- DRAM technology/performance is driven by mobile sector as well as computing
- 3D versions have started engineering sampling for high performance computing

3D Memory Stacks

2D – DDR3 DRAM

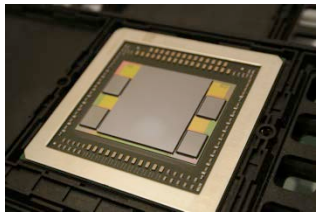


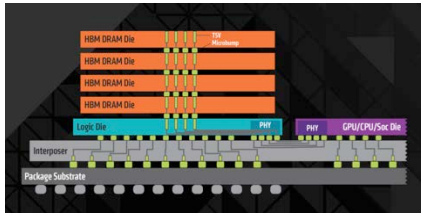
3D DRAM: Hybrid Memory Cube



www.Micron.com

3D DRAM: High Bandwidth Memory





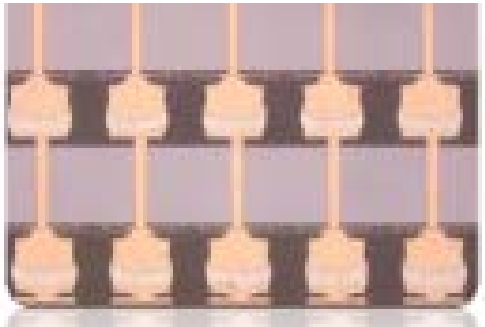
www.AMD.com

	2D DDR3 DRAM	3D Hybrid Memory Cube
Size, CM	2.0 x 13.0	1.6x 2.0 or 3.1x3.1
Capacity	Up to 4GB	Up to 4GB
Data Rate	10x lower	120GB/s or 160 GB/s
Power	100%	44%

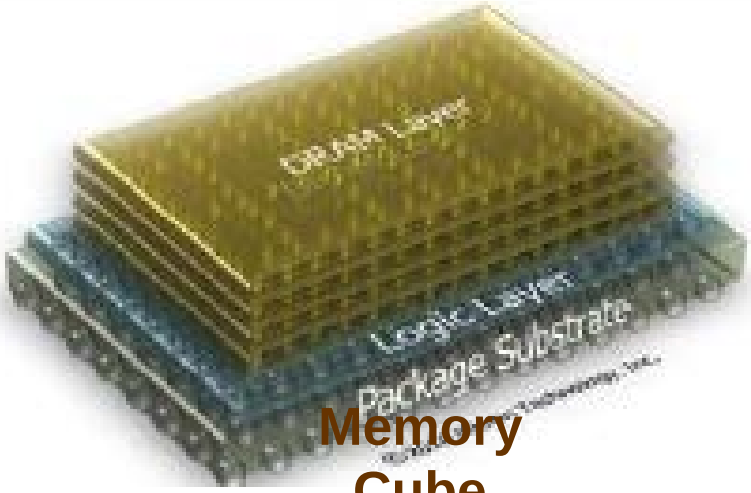
3D addresses the noise, delay and power consumption due to PCB level routing

3D Integrated Circuit Technology

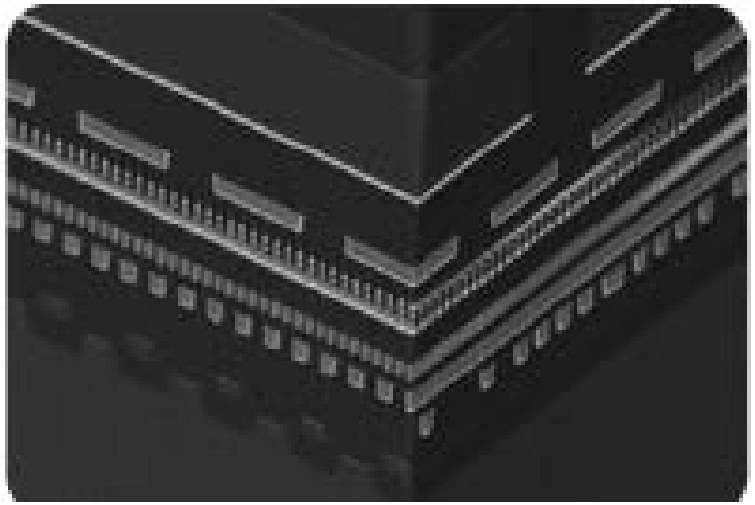
Bumps



TSV



Memory Cube



DRAM Reliability

- 2015 JPL study of >600 DDR3 DRAMs
  - Tested as single package or DIMM
  - generally good reliability
  - <1% out of family when operating within data sheet limits

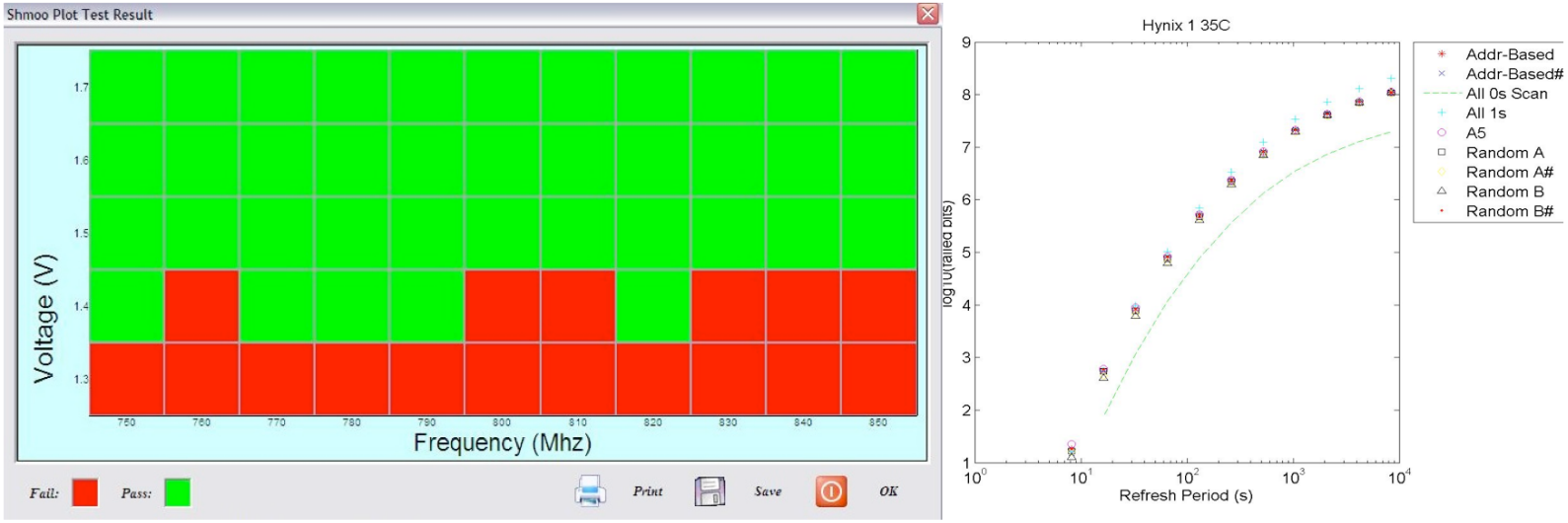
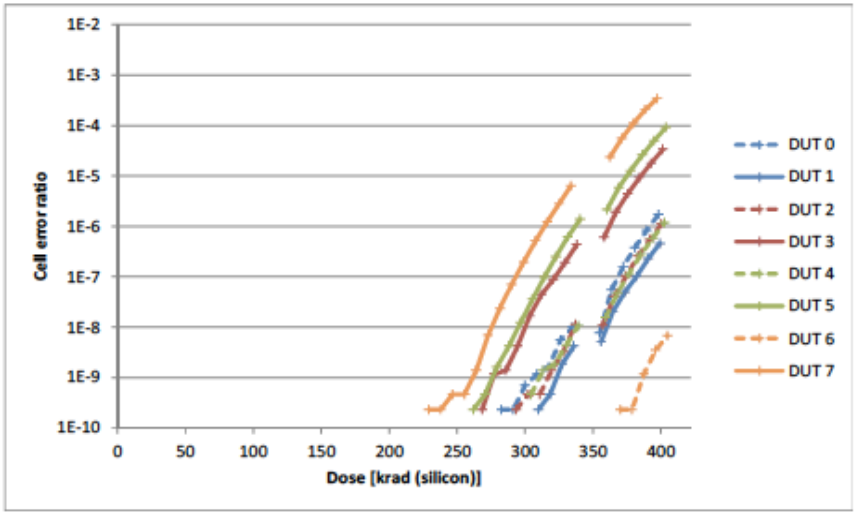


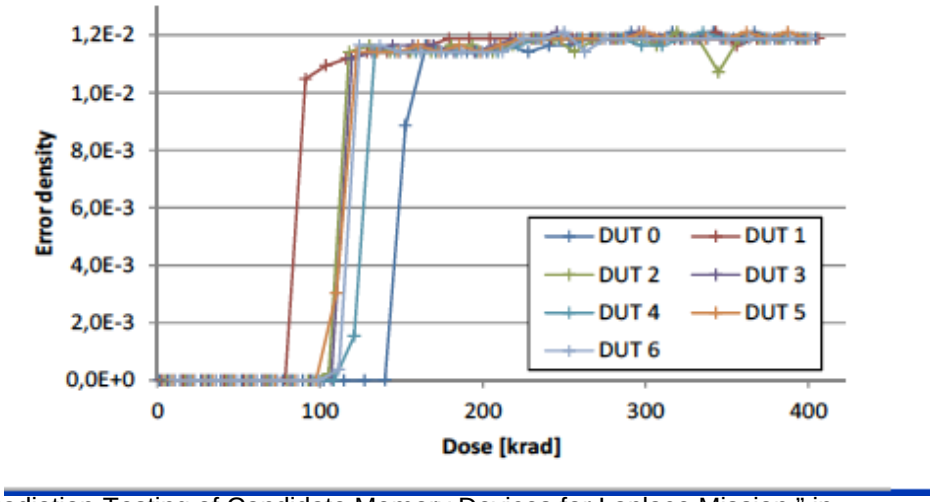
Figure 1. DDR3 Reliability (L) Shmoo plot for and (R) Retention Error vs. Refresh Period for a Hynix Die[19]

S. Guertin, and S.Vartanian, "NEPP DDR3 Device Reliability FY15 Test Report," Jet Propulsion Laboratory, NASA. 2015.

Total Ionizing Dose Radiation Tolerance

DDR3 SDRAM





H. Schmidt, M. Hermann, and F. Gliem, “Radiation Hard Memory-Radiation Testing of Candidate Memory Devices for Laplace Mission,” in CNES/ESA Radiation Effections Final Presentation Days, 2015, March 10.

- DDR3 DRAM has good TID radiation tolerance: initial error start at 70krad(Si)-250krad(Si)
- Single event effects must be considered on a case by case basis

Outline

- Spacecraft Memory Use
- DRAM
  - Technology Trend
  - Performance Trend
  - Radiation and reliability
- **NAND**
  - Technology Trend
  - Performance Trend
  - Radiation and reliability
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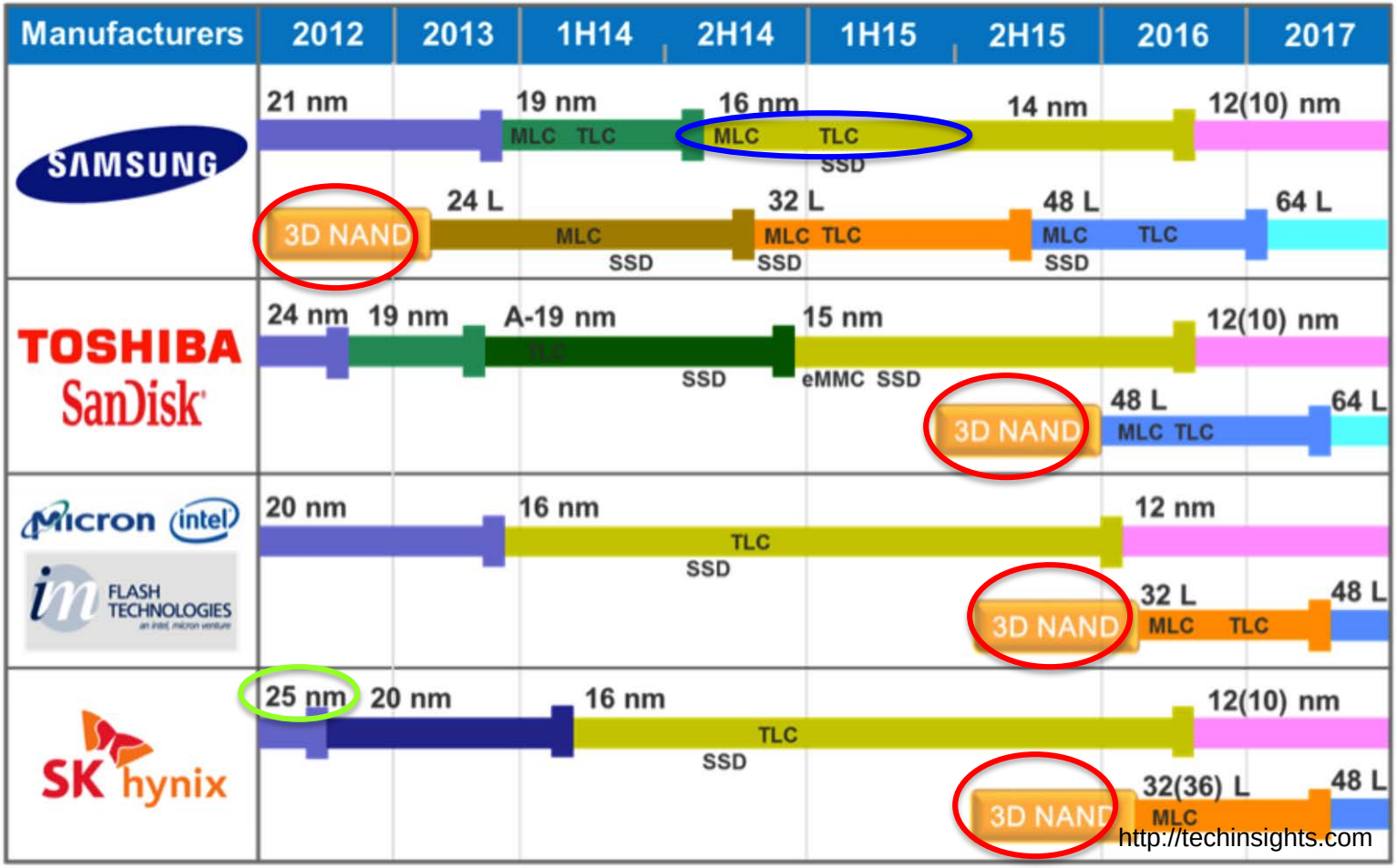
NAND Technology Progression



- NAND has become process technology driver due to market sensitivity to density
- Multi-bit per cell (MLC/TLC) has doubled and tripled data storage density
- On wafer 3D technology has been commercialized

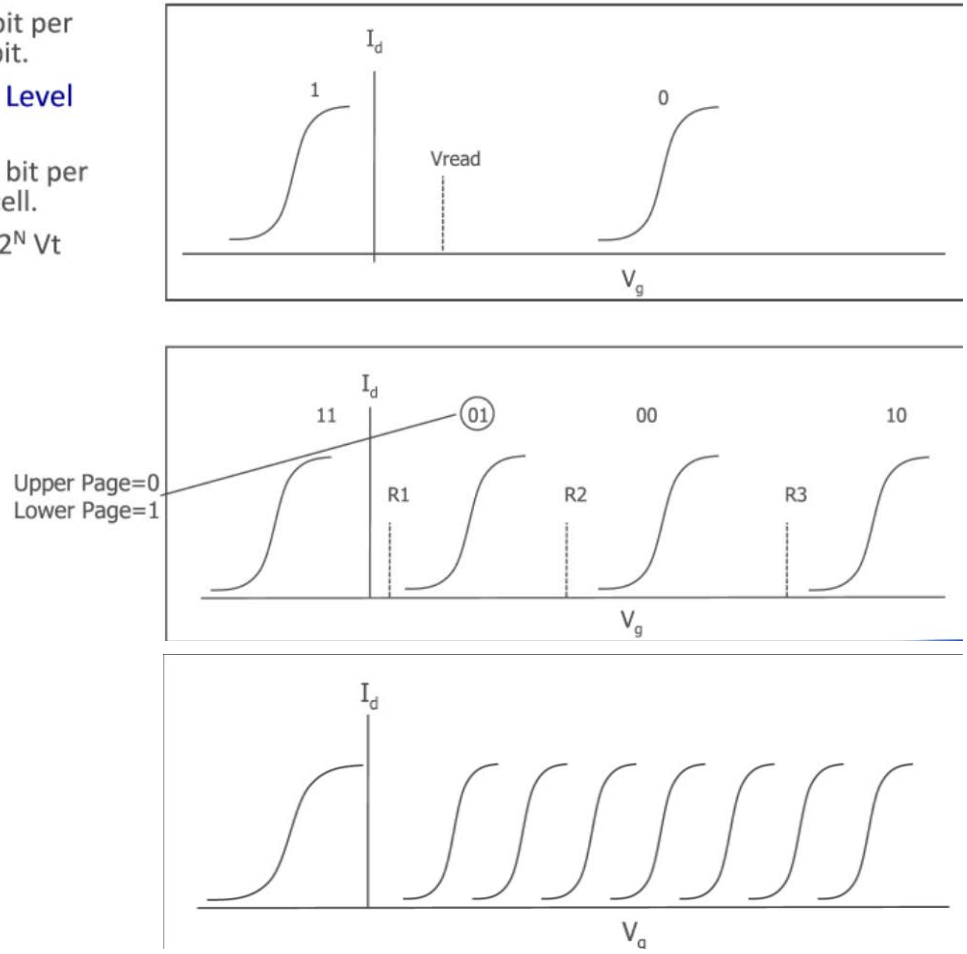
NAND Multi-Level Cell

SLC-Single Level Cell.

- 1 logical bit per physical bit.

MLC-Multi Level Cell.

- >1 logical bit per physical cell.
- Requires 2^N Vt levels

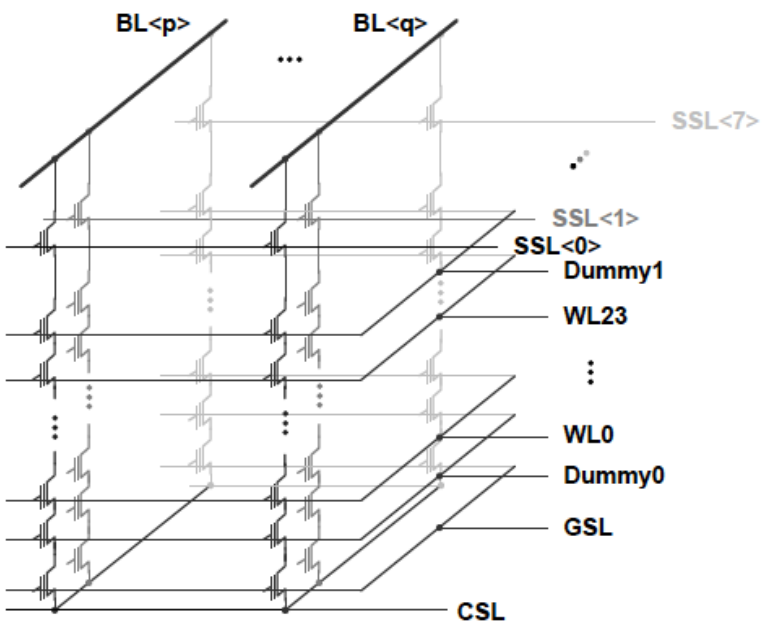


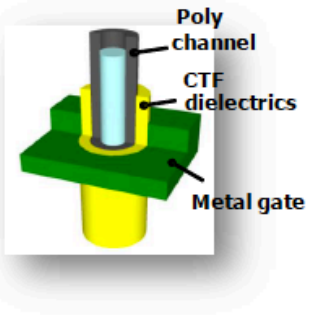
- Multi-level cell (MLC) technology allows for storage of multiple data bits in a single physical cell.
- MLC stores 2 bits of data in 4 distinct Vt levels
- TLC stores 3 bits of data in 8 distinct Vt levels
- Programming and read multiple bits require much more precision: slower, more power use, more errors
- MLC/TLC NAND can be used but error rates must be managed by error correction code (ECC)

T. Marquart “Practical Approach to Determining SSD Reliability,” in Flash Memory Summit, 2015, pp. 1–48.

3D NAND Array Architecture

- ✓ Advanced V-NAND Technology with Damascened Metal Gate
- ✓ Cell : All-around Gate Structure + Charge Trap Flash
- ✓ String : 24-WL + 2-DWL + 2-Select WL
- ✓ Block : 8 Strings with Shared BL (8KB)

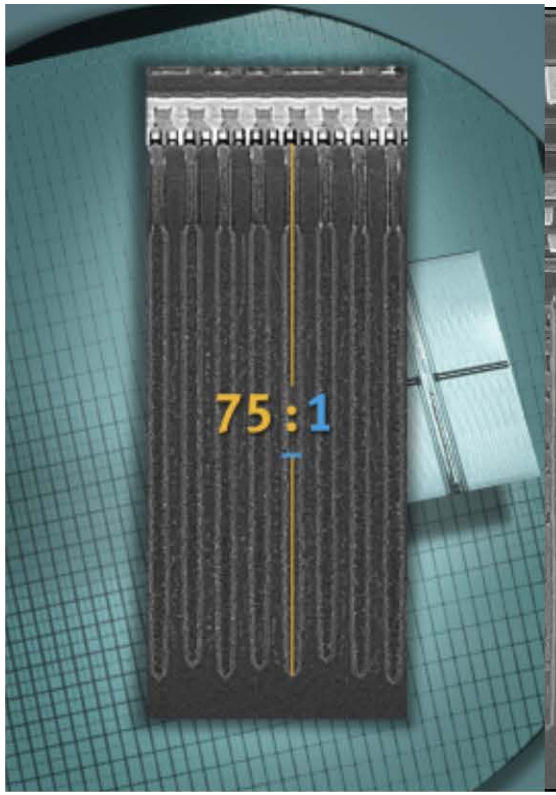


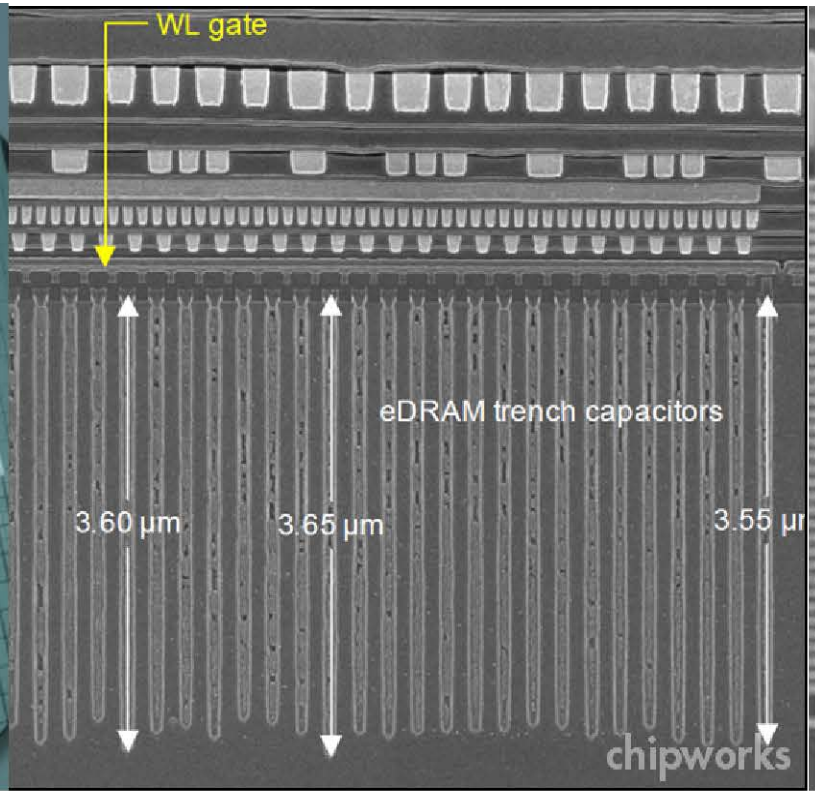


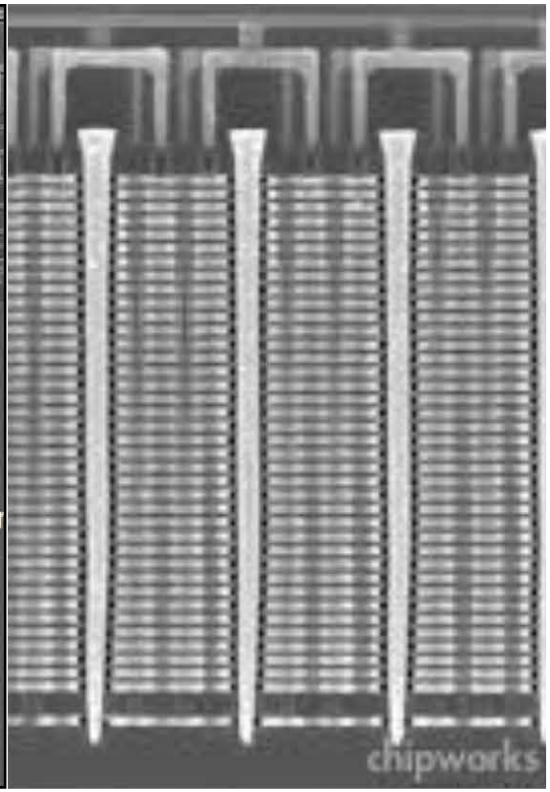
Park et al, ISSCC 2014

- 3D NAND is not TSV, but a single wafer process forming a 3D memory array
- Entered market late 2014 with 24 layer, new products are 32 layers and TLC

3D NAND and DRAM Similarities



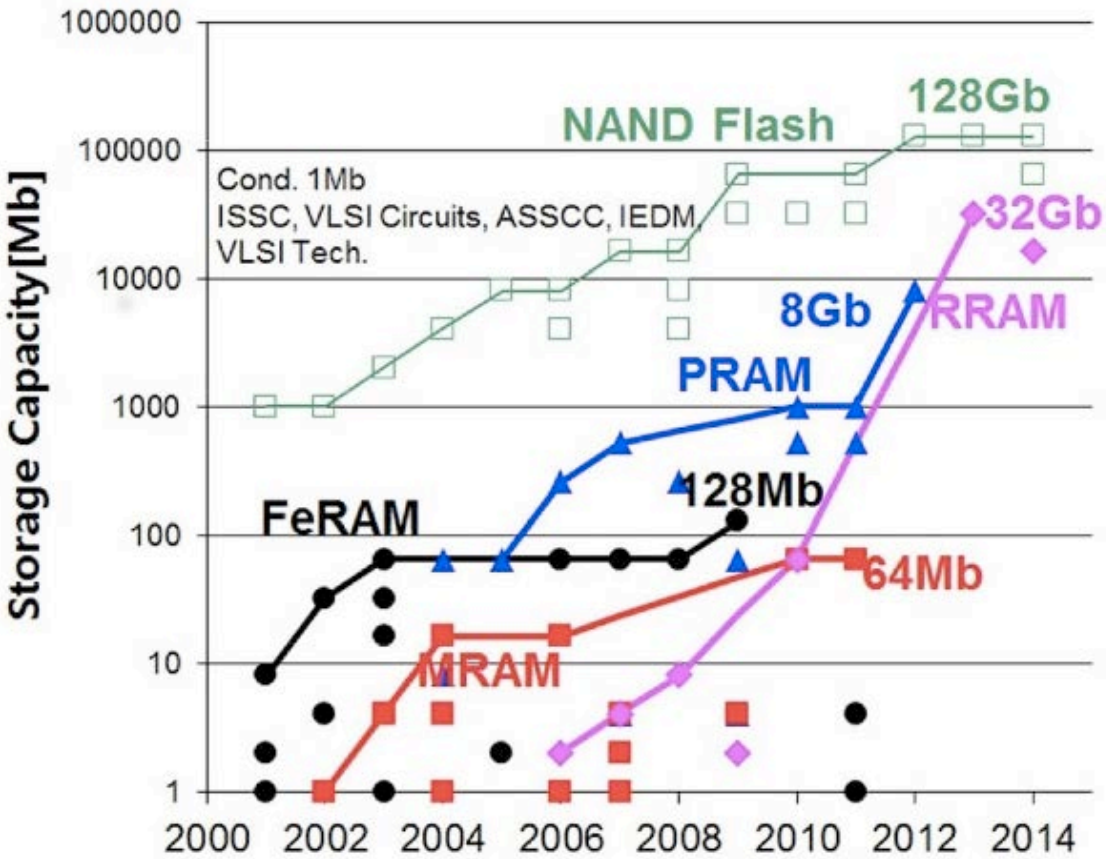




\http://www.infineon.com/cms/en/about-infineon/press/press-releases/2004/132221.html.
http://chipworksrealchips.blogspot.com/2014/02/intels-e-dram-shows-up-in-wild.html.
https://www.chipworks.com/about-chipworks/overview/blog/second-shoe-drops-%E2%80%93-samsung-v-nand-flash

- Deep trench technologies developed in DRAM is part of processes enabling 3D NAND technology
- 3D NAND took about 10 years from first papers to products

NVM Density Progression



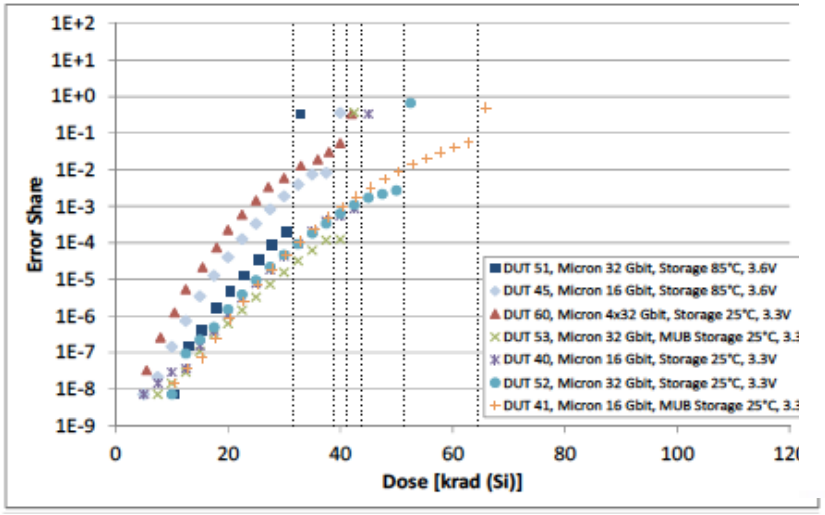
Storage capacity trend of emerging non-volatile memories. http://eetimes.com

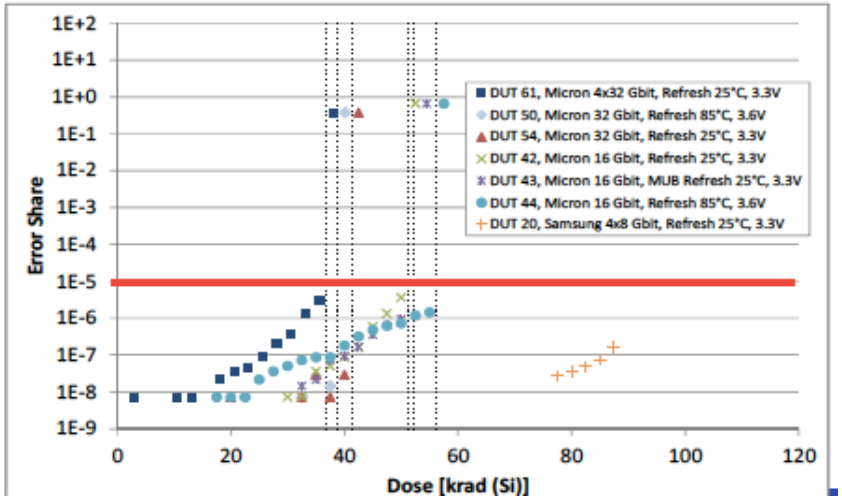
Source: ISSCC

- NAND flash has been density driven and experienced a 100X increase in density in ~15yrs
- Multi-chip per package-> 1Tb per package

Total Ionizing Dose Radiation Tolerance

NAND-Flash





H. Schmidt, M. Hermann, and F. Gliem, “Radiation Hard Memory-Radiation Testing of Candidate Memory Devices for Laplace Mission,” in CNES/ESA Radiation Effections Final Presentation Days, 2015, March 10.

- 32-25nm node SLC NAND experiences single bit errors in total ionizing dose.
- Without re-programming error rate reaches 1% at ~30krad.

MLC Sensitivity to Radiation

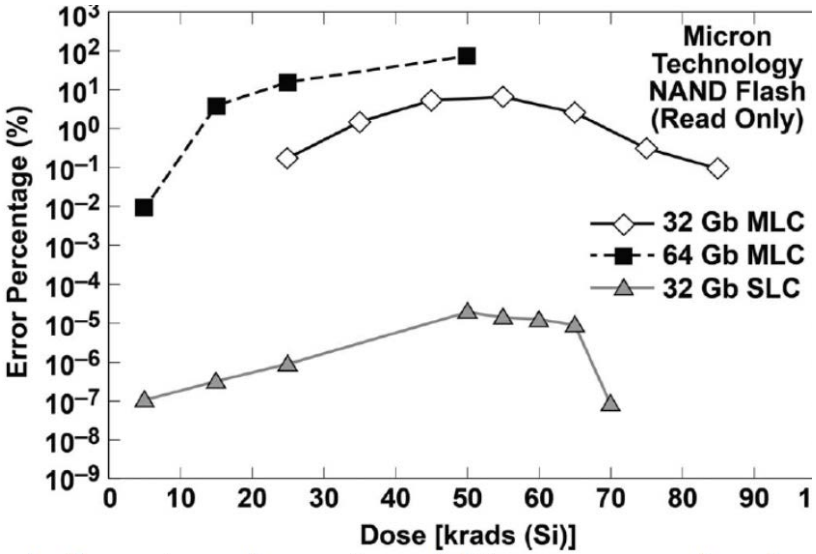


Fig. 3. Comparison of percentage of bit errors versus dose for Micron Technology 32-Gb SLC, 32-Gb MLC and 64-Gb-MLC NAND flash memories in Read Only mode

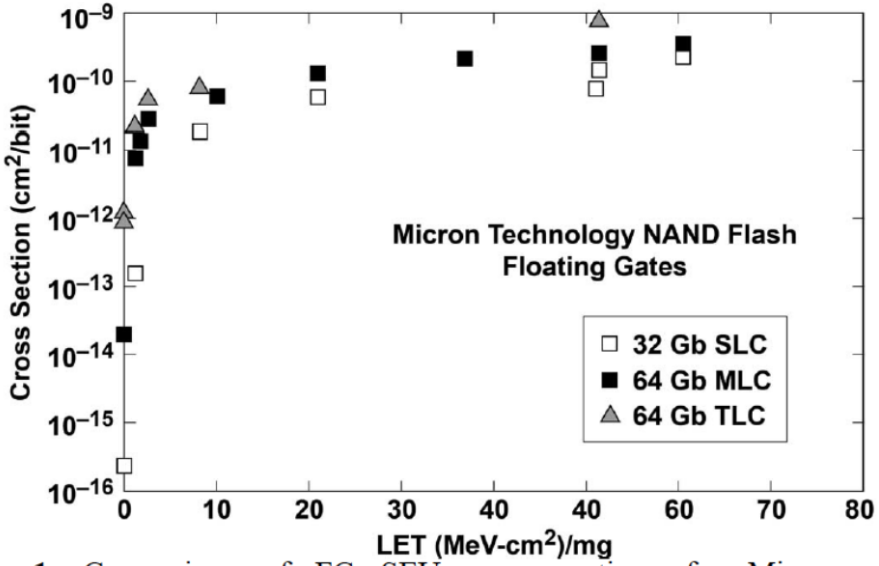
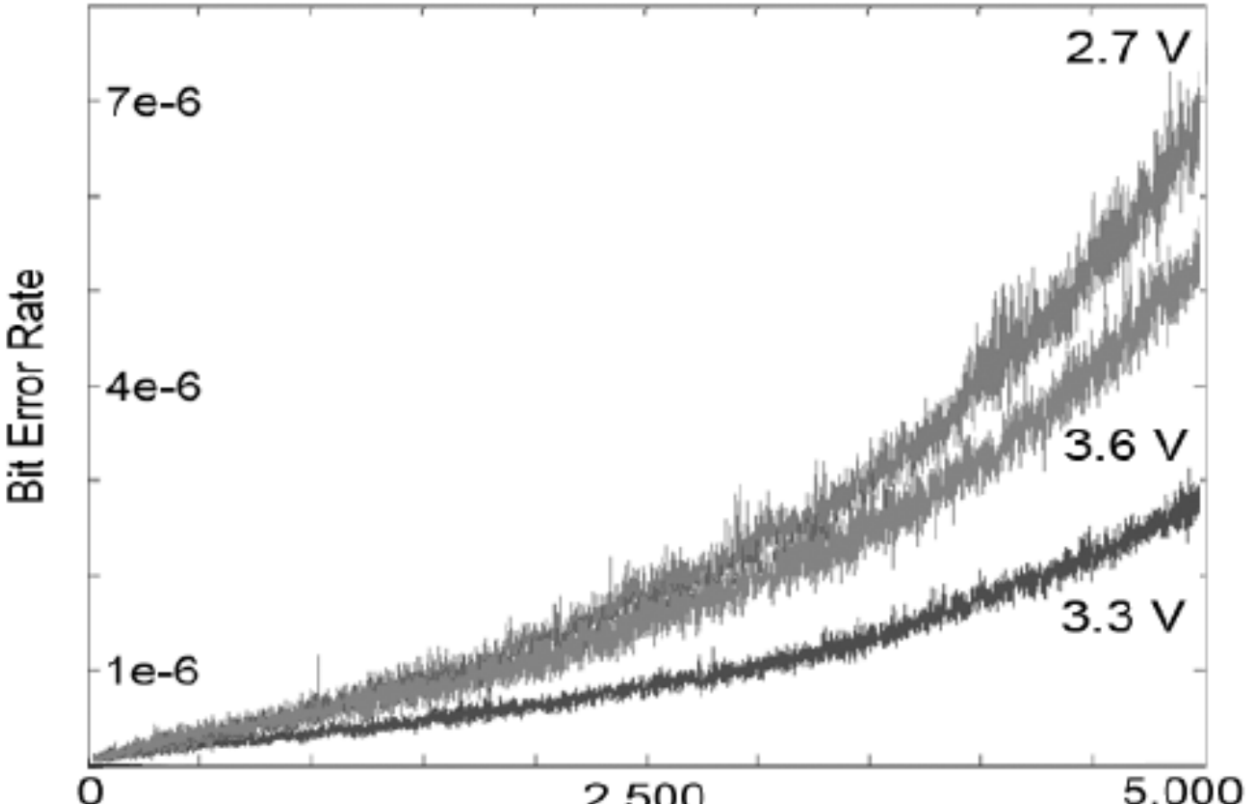


Fig. 1. Comparison of FG SEU cross sections for Micron Technology 64-Gb TLC, 64-Gb MLC and 32-Gb SLC NAND flash memories. The error bars are smaller than the size of the plotting symbols.

F. Irom et al., *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3329–3335, 2010.

- MLC NAND error rate is higher and more sensitive to TID than SLC
- Single event upset cross-section also higher for MLC and TLC NAND

NAND Reliability



J. Heidecker et al., *Integr. Reliab. Work. Final Rep.*, p. 145, 2010.

- Bit error rate for 32Gb MLC NAND as a function of endurance stress and Vcc measured for SMAP qualification show BER trend manageable when endurance managed within datasheet specification

Conclusions

- **DRAM and NAND has experienced a tremendous increase in capability in the last 10-15 years.**
- **Advanced DRAM and NAND capability can be used for space applications if limitations are understood and managed.**
  - **Radiation tolerance**
  - **Reliability**

Acknowledgments

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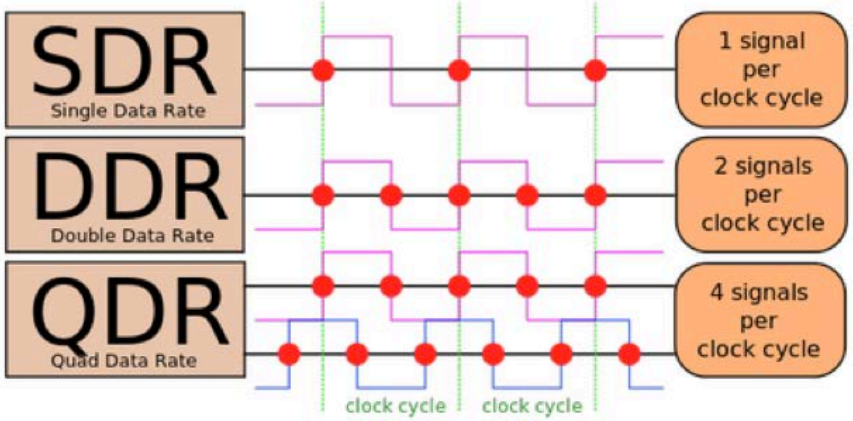
Appendix

Aerospace Memory Modules

- 3DPlus
  - Rad tolerance SRAM, SDRAM, DDR, DDR2, PROM, EEPROM, MRAM, FRAM and Flash (4Gb-128Gb)
  - Memory stacks
  - Micro-SSD- controller +2-4 SLC NAND in a package
- Maxwell
  - Rad tolerant memory in shielded package PRAM, EEPROM, SDRAM, flash
- TeleCommunication Systems, Inc.
  - Ruggeded SSD, 2.5” SATA III
  - SLC or MLC
  - Up to 8TB
  - Tested and verified to MIL-STD-810
- Seakr- 3U VpX Flash
  - http://www.seakr.com/new_site/what/MEMO/MEM/VPX.html
  - SSD with DDR2 SDRAM buffer and flash based memory
  - 92GB capacity

DRAM Data Rates



Beyond DDR->QDR

Some salient differences between DDR generations(source wiki):

Names	Memory Clock	I/O Bus Clock	Transfer Rate	Theoretical Bandwidth
DDR-200, PC-1600	100 MHz	100 MHz	0.2 GT/s	1.6 GB/s
DDR2-800, PC2-6400	200 MHz	400 MHz	0.8 GT/s	6.4 GB/s
DDR3-1600, PC3-12800	200 MHz	800 MHz	1.6 GT/s	12.8 GB/s
DDR4-3200, PC4-25600	400 MHz	1600 MHz	3.2 GT/s	25.6 GB/s

JEDEC DRAM Roadmap

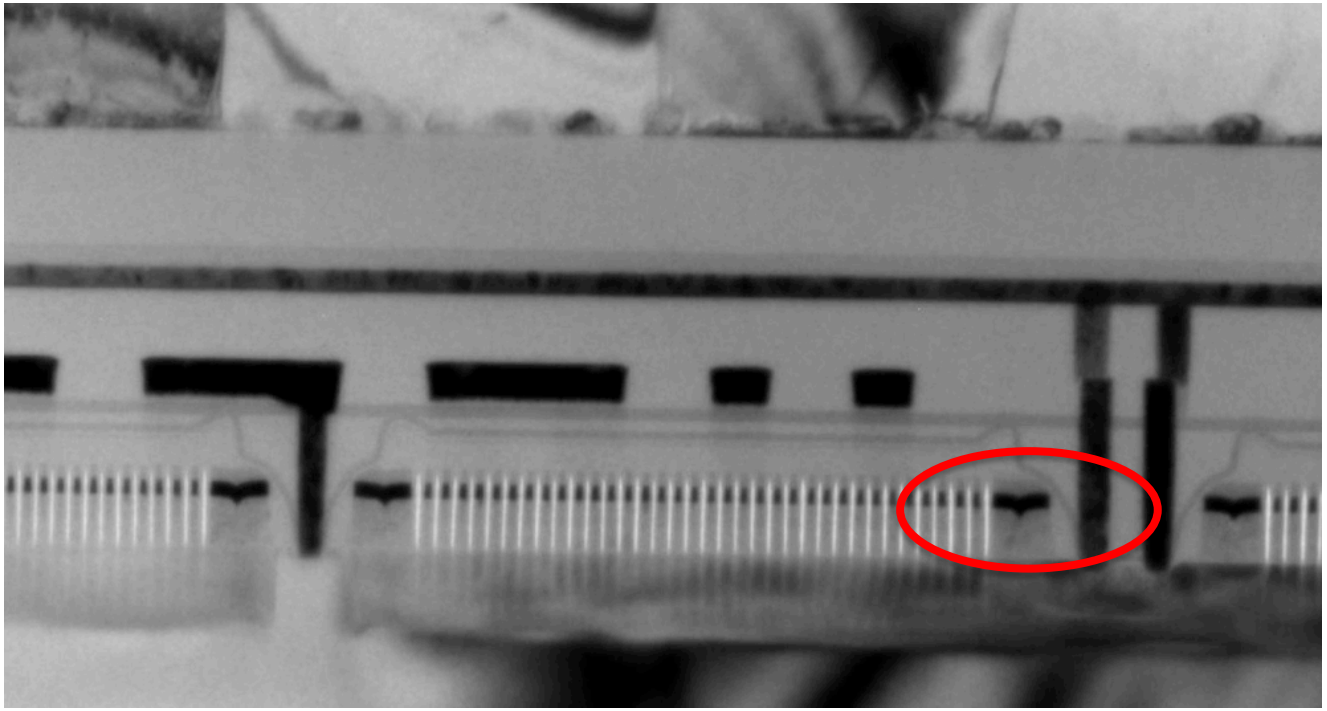
	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Process	3x nm		2x_H		2x_L		1x_H		1x_M	
DDR3	1600		1866							
DDR3L	1333		1600							
DDR4			1866	2133	2400	2667				
DDR4L						2400	2667	2667	2932	3200
Device		2Gb								
Device				4Gb						
Device							8Gb			
Device										16Gb
DIMM	8GB	16GB		32GB		64GB	64GB			128GB
3DS/TSV				DDR4_2H		DDR4_4H		DDR4_8H		

R. D. Williams, T. Sze, D. Huang, S. Pannala, and C. Fang, “Server Memory Road Map,” JEDEC report. 2011.

Note:

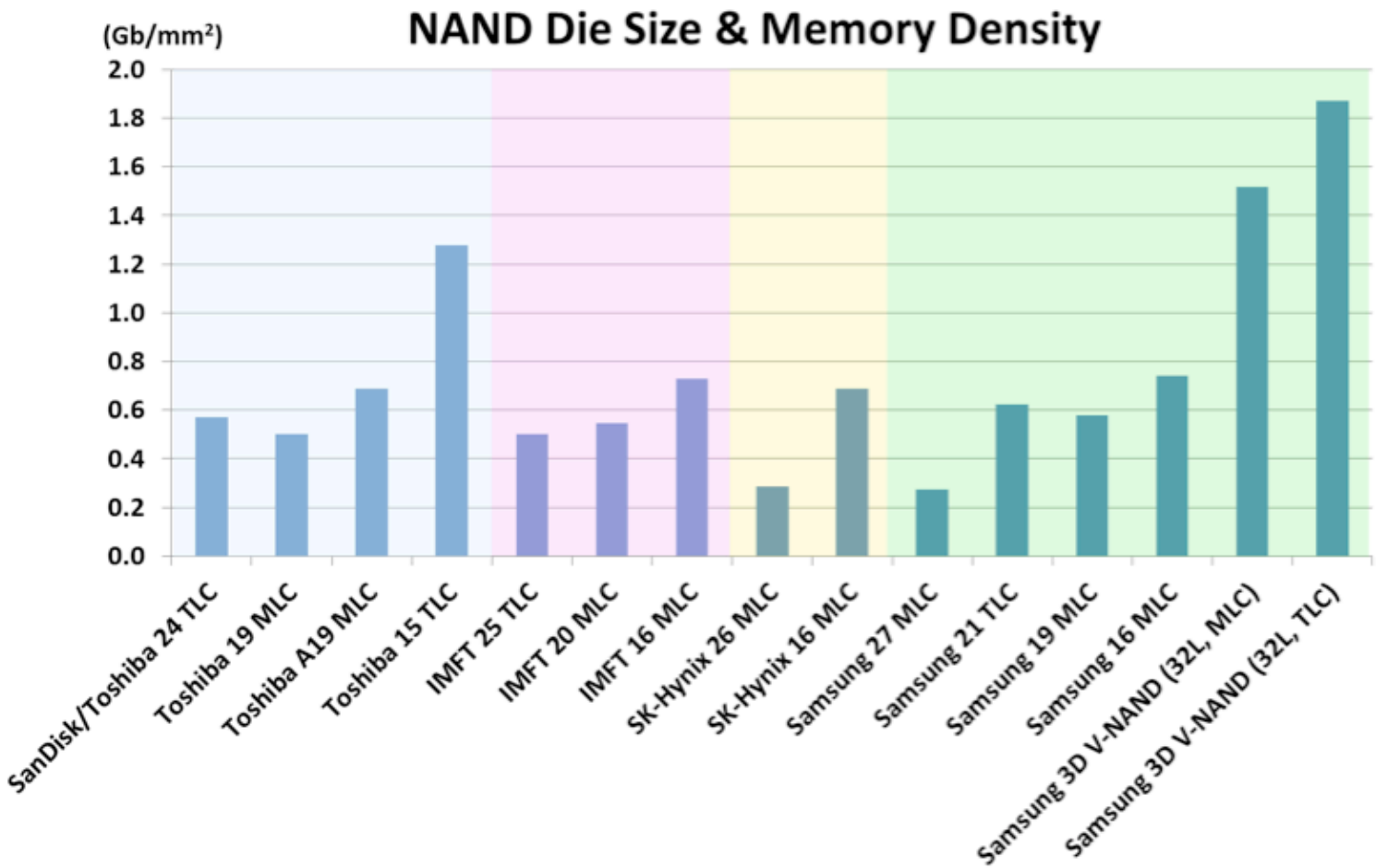
* DRAM speed: device raw speed, in Mbps.
* DIMM density: sweet spot density.
* 3x = 30-39 nm, 2xH = high 20’s nm, 1xH = high teen nm, 1xM= mid teen nm
* DDR4L: 1.0V, TBD.

State of the Art NAND



- Example 19nm NAND strings show 32 physical memory cells between each select transistor.
- Note select transistor size (~200nm) does not scale and is limited by program/erase voltages

1X Node NAND Densities



http://electroiq.com/blog/2015/08/comparison-1y-nanometer-nand-architecture-and-beyond-samsung-toshibasandisk-micron-and-sk-hynix-16nm-and-15nm-devices/