National Aeronautics and
Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

AAS GN&C Conference: Feb 5 – Feb 10, 2016

Session VI
Miniaturization of GN&C Components

Conceive, Believe and Achieve; A Path To Miniaturization, COTS Infusion, and Size Weight and Power Realization for Flight

Presented by

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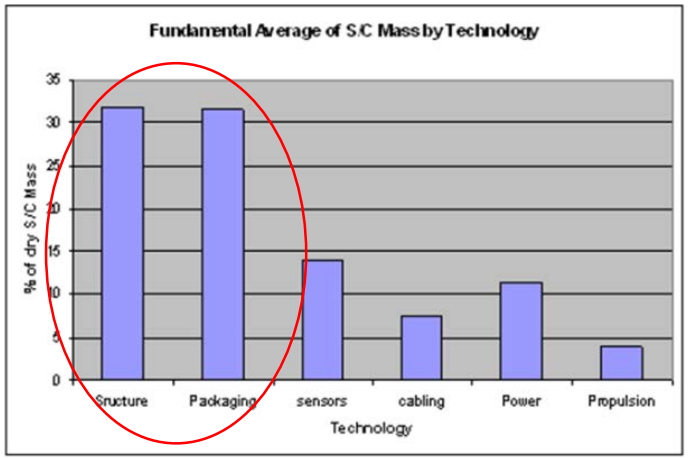
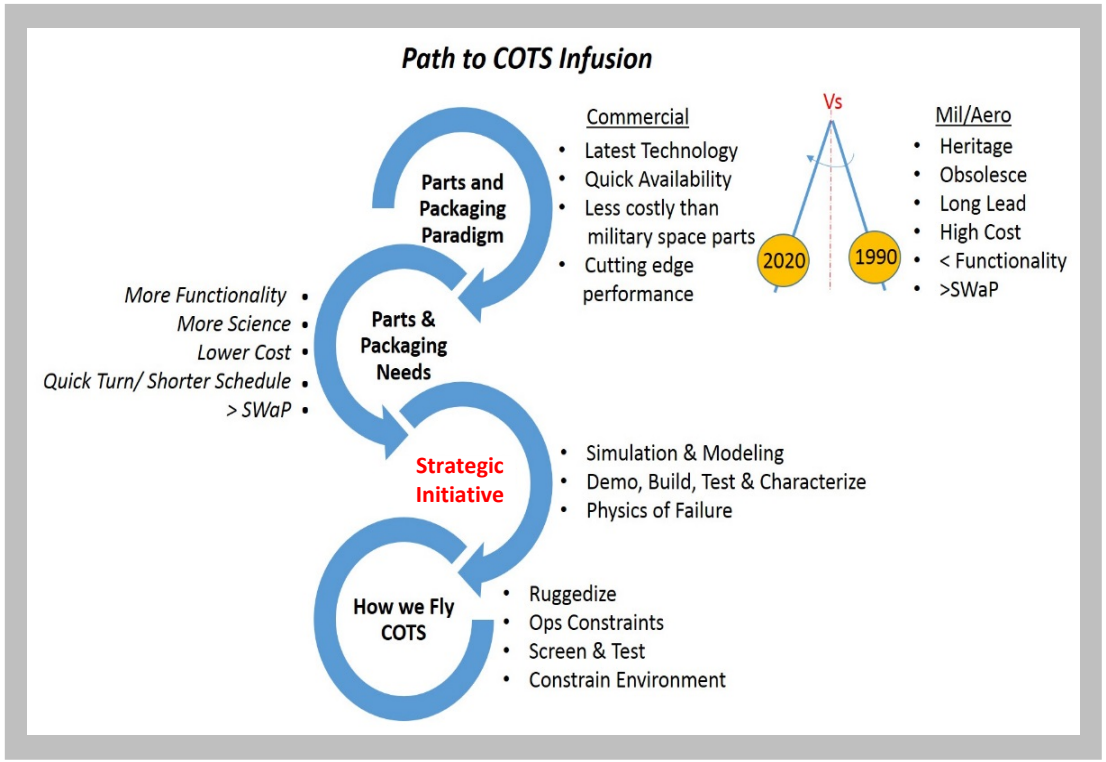
Motivation

Packaging is a major contributor to Spacecraft Mass > 30%



Since the late 1980s, studies at JPL have shown the largest contributor of total spacecraft dry mass is concentrated in two technology areas: structure and packaged electronics.

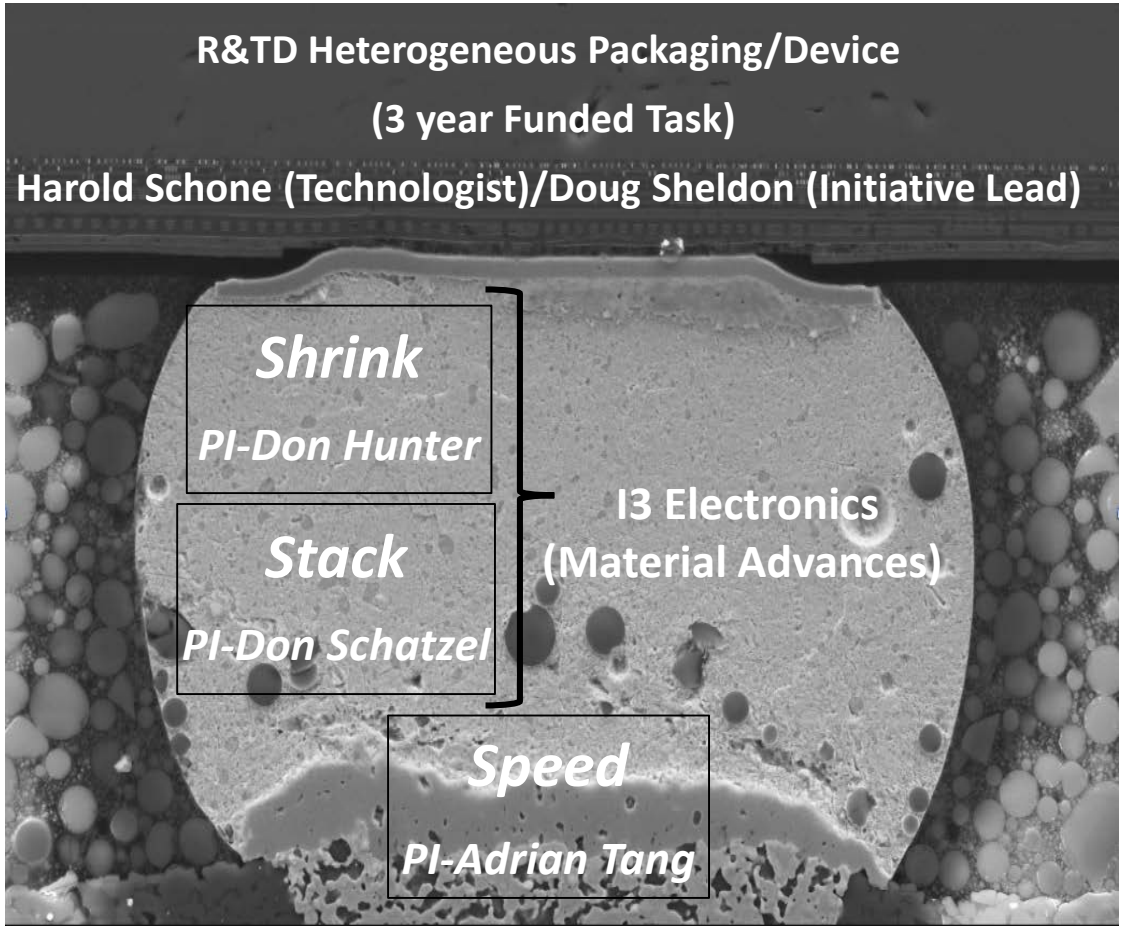


Benefits:

- **Payload costs are about $10K/lbs – incentive to miniaturize**
- **Landers/SC relies on our own power – incentive to reduce power usage is significant**
- **Interconnects i.e., (Shuttle = ~300 miles of wire and MSL = 60Kg) – incentive to reduce mass**

Initiative Objective

JPL's Office of the Chief Scientist and Chief Technologist (OCSCT) coordinates and identifies a number of strategic areas that are critical to NASA's future success



- **SHRINK GOAL: Transitioning *Commercial Off-The-Shelf (COTS) advanced yet mature Packaging Technologies into mainstream use at JPL demonstrate Size, Weight and Power (SWaP) Benefits***
- **STACK GOAL: Infuse COTS Stacked Chip Technology using a 2.5D packaging design approach with IBM developed Core EZ substrate technology for extreme Electronics Miniaturization**
- **SPEED GOAL: Perform a substrate study of highly reliable, physically flexible, and lightweight interconnects**

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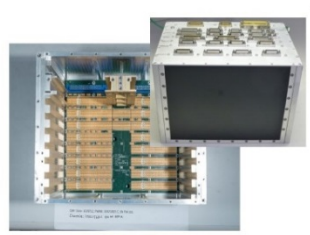
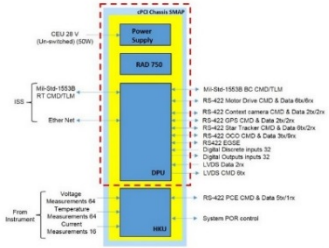
✓ Shrink

Approach: Demonstrate the reliability, performance and functionality of COTS technology



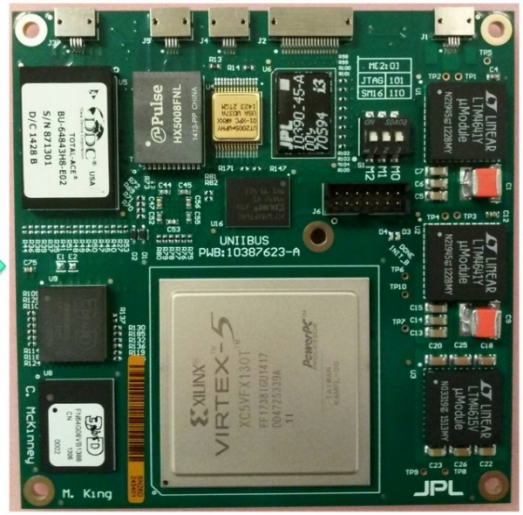
SMAP cPCI card cage

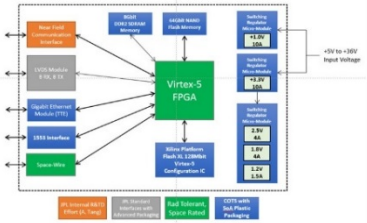


RAD-750 (3U)

SMAP cPCI Power Supply (6U)

OCO3 Digital Processing Unit (6U)





UNIIBUS (1U)

JPL's SOP circa 1990 Technology

- *8kg, 28W, 15,000 cm ^{3}*
- *6U Chassis, requires 4 PWA*
- *Labor + Material: ~$600K*

R&TD Developed UNIIBUS

- *1.2kg, 18W , 276 cm ^{3}*
- *Single 1U Assembly*
- *Labor + Material: ~$100K*

Current Snapshot, JPL Vs Industry State-of-Practice (SOP)

Benefits to NASA and JPL:

- ✓ ***Significantly reduce the contribution of electronic packaging dry spacecraft mass***
- ✓ ***Enable new types of missions not possible with JPL's traditional packaging approach***
- ✓ ***Enable more science payload capability for future missions***

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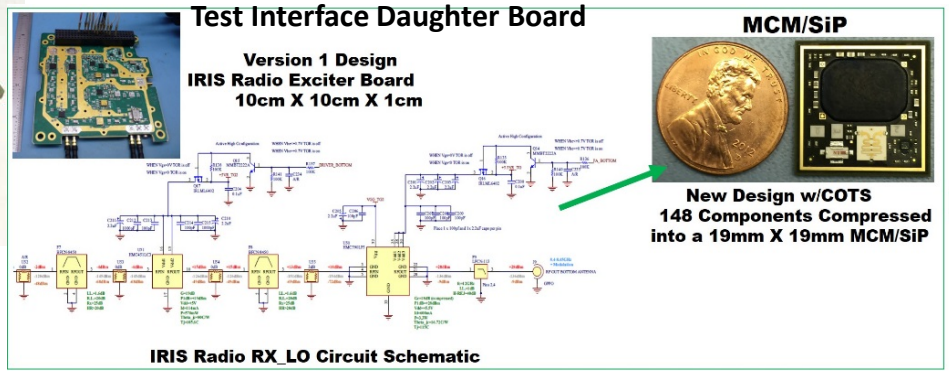
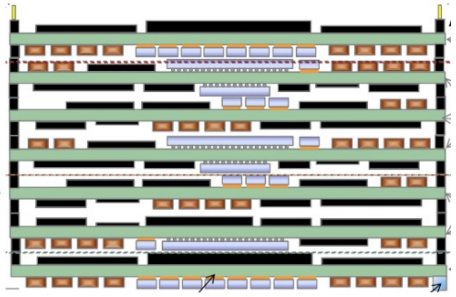
✓ Stack

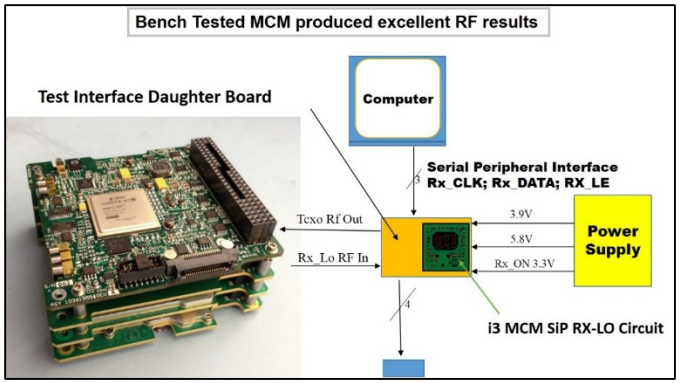
Approach: Demonstrate 2.5D stacked bare die for RF application

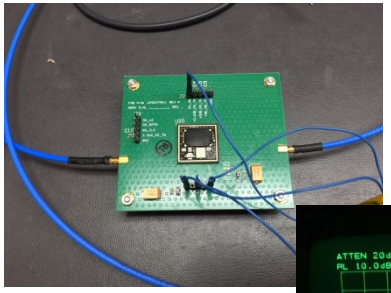
Version 1 Design
IRIS Radio 4 Board Stack
10cm X 10cm X 5cm

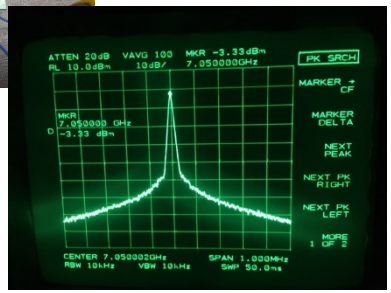




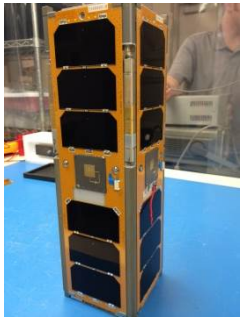
Future Design Concept
Complete IRIS Radio
MCM/SiP Stack 42mm x 42mm x 42mm







MCM Tested at 7 GHz



CubeSat Radio Applications
3U & 6U configurations

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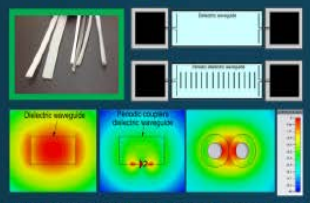
✓ Speed

Approach: Develop a gigabit, low power, low cost, EMI capable, easy to integrate WaveCable solution

Benefits to NASA and JPL:

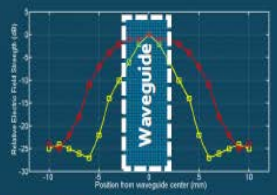
- **Developed a complete solution for Near-Field-Connects**
- **EMI study shows only 1/100K of the mm-W signal leaves waveguide**
- **PoC have shown using CMOS chips at 60, 100 and 150 Ghz operating up to Gb/s**
- **Developed CMOS NFC Rx and Tx Chips sets.**
- **Developed multiple Coupler Interface solutions:**
  - **Chip/Antenna Assembly**
  - **Socket Assembly**
  - **Improved Lens Coupler Structure**

Geometry Study Completed



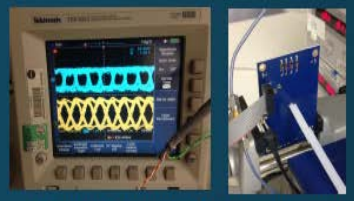
Data was collected and presented on field confinement, various substrates And geometries and which are best suited to mmW links.

EMI Study Completed



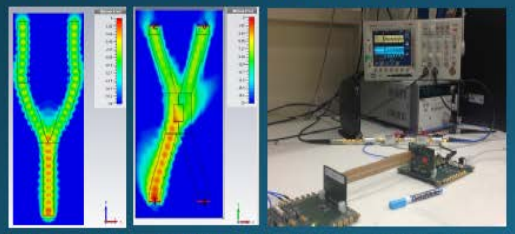
Data was collected using industry standard measurements on leakage and stray emissions showing that only 1/100,000th of the mmW signal leaves the waveguide.

P.O.C. Link Demonstrated



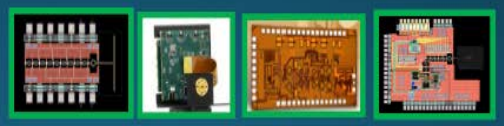
Proof-of-concept links were shown using CMOS chips at 60,100 and 150 GHz operating up to Gb/s

Spin-off technology developed:



Signal splitters, isolators and printable couplers for dielectric waveguides were also developed, based on the findings of the above studies.

Chip study Was completed



We looked at all the existing NFC mm-wave chips from Hittite, Sony, Mediatek and Vibiq, and found that we could probably do better for JPL needs by designing something ourselves.... Gen-2 done!, Gen-3 due march

✓✓ Enabling Technology

Microelectronics High Density Interconnect

CoreEZ®

- Build Up
  - Cost performance
  - **Particle filled epoxy**
  - Thin core (& coreless)
  - Laser drilled core, build up
  - 25 micron Cu trace
  - 25 micron space
  - Buried resistors, capacitors
  - Flip chip, Wire bond, SMT
  - Radiation Hard Capable

MicroFlex

- Thin, Flexible
  - Cost performance
  - Single Sided
  - Double Sided
  - **Polyimide+**
  - 50um Laser drilled vias
  - 11 micron Cu trace
  - 11 micron space
  - Flip chip, SMT

Formable/Flexible

- Thin, Flexible
  - **LCP** 4,6 Layers
  - 100um Laser vias
  - 50 micron Cu trace
  - 75 micron space
  - Flip chip, SMT

HyperBGA®

- **PTFE** Substrate
  - High Bandwidth/RF
  - Particle filled material
  - Coreless
  - 50um Laser Vias
  - Fusion Bonding
  - 25 micron Cu trace
  - 33 micron space
  - Flip chip, WB, SMT
  - Radiation Tolerant

Several options available for the miniaturization (shrink) of Microelectronics

✓Team chose to use CoreEZ® for this project based on design requirements

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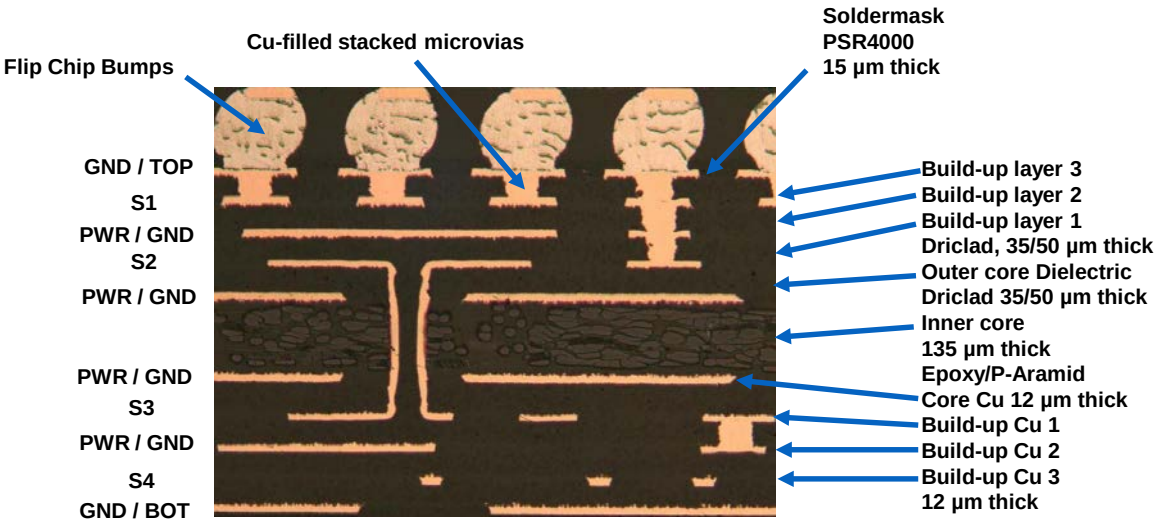
Enabling Technology

Advanced Build-up Technology:
- **Organic material set**
- **High performance dielectrics**
- **Lightweight**
- **Dense wiring**
- **Thin Layers**
- **Thin core**
- **Embedded Passives**
- **Space (radiation) compatible materials**

CoreEZ Stack-ups
- **1-4-1 = 2 Full Stripline Signal planes, 4 PWR/GND**
- **2-4-2 = 4 Dual Stripline Signal planes, 4 PWR/GND**
- **3-4-3 = 4 Full Stripline Signal planes, 6 PWR/GND**
- **4-4-4 = 4 Full Stripline Signal planes, 8 PWR/GND**

3-4-3 Stack up shown (10 copper layers)
Substrate thickness ~0.7 mm

Substrate features and advanced IC Assembly techniques enable bare die implementation



Attribute	Standard PCB	CoreEZ® Substrate	Shrink opportunity
Through via	Mechanical	Laser	
Through via dia.	200 microns	50 microns	4X
Through via capture pad diameter	400 microns	100 microns	4X
Line Width	75 microns	25 microns	3X
Space Width	75 microns	25 microns	3X
Semiconductors	Packaged	Bare die or small package	4X to 10X

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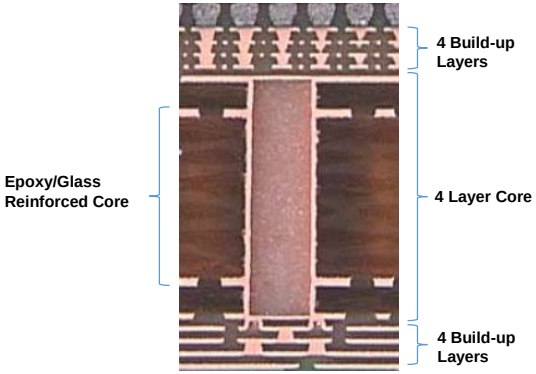
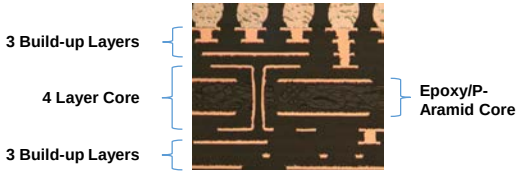
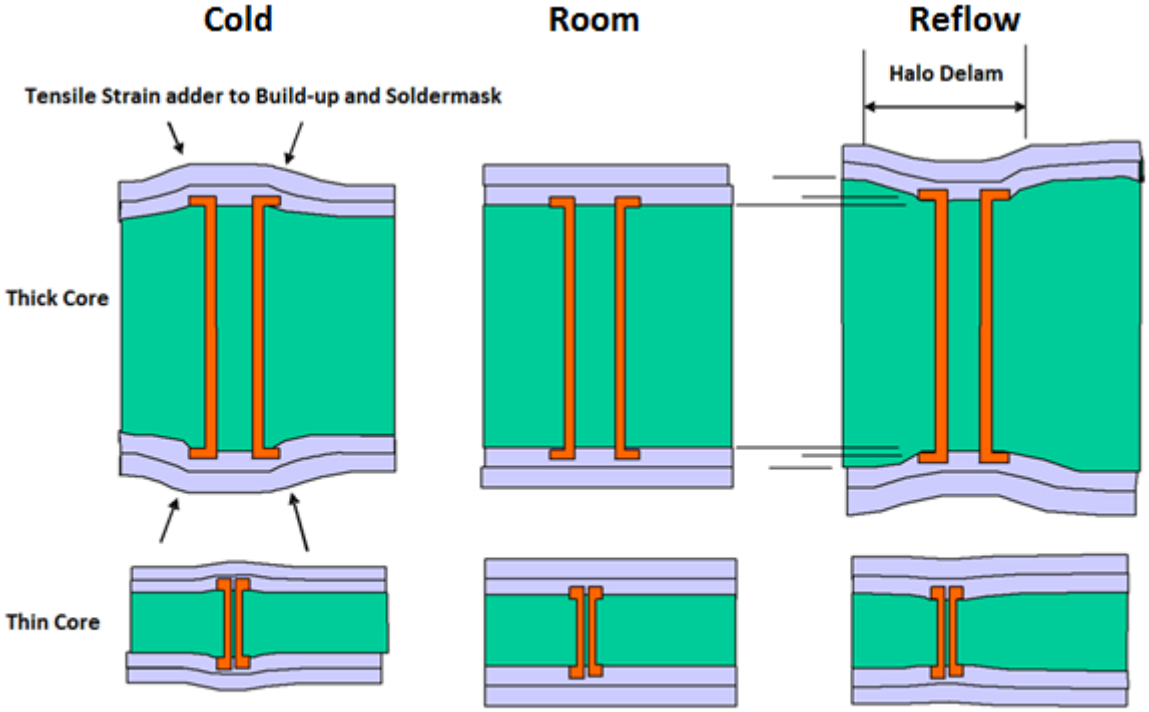
Substrate Expansion, Combined with PTH Restraint, Creates Z-expansion Stress on Soldermask and Potential Halo Delam

Standard 4-4-4 Build-up Substrate



CoreEZ™ 3-4-3 Substrate

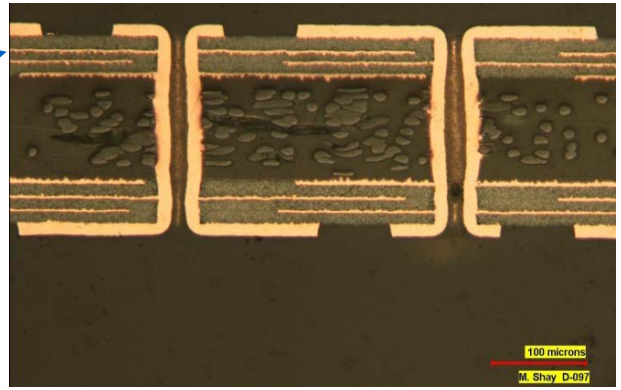




Thin Core
Much less deformation for BU layers to absorb
Results in less stress adder to BU and soldermask layers
Virtually no 'halo' delamination

Enabling Technology

Embedded Passive Components for increased size reduction



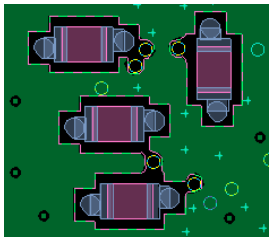
Library of pre-designed resistor elements

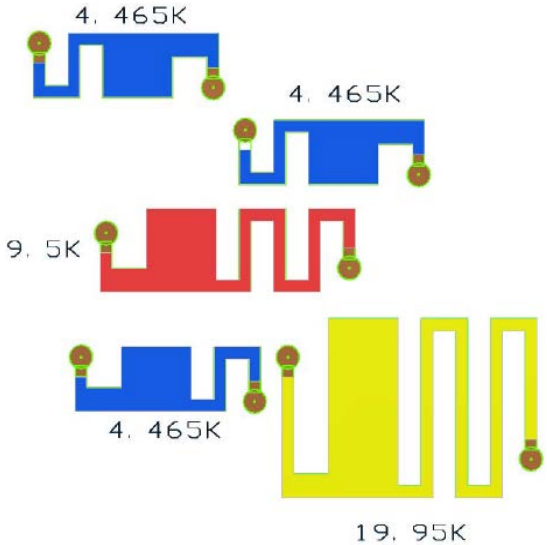
Thin film resistor materials
- Ticer TCR®
- 10 - 250 ohms per square

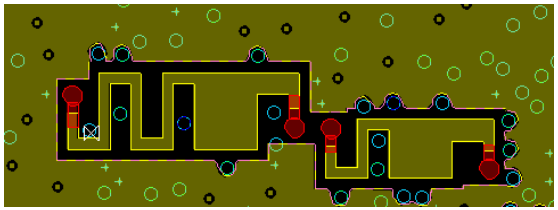
Resistor values from 5 ohm to 50 Kohm

Resistor tolerances from 1 – 20%
- Laser Trimmed for <5%

Typical resistor areas
- 0.2 – 15 mm^2







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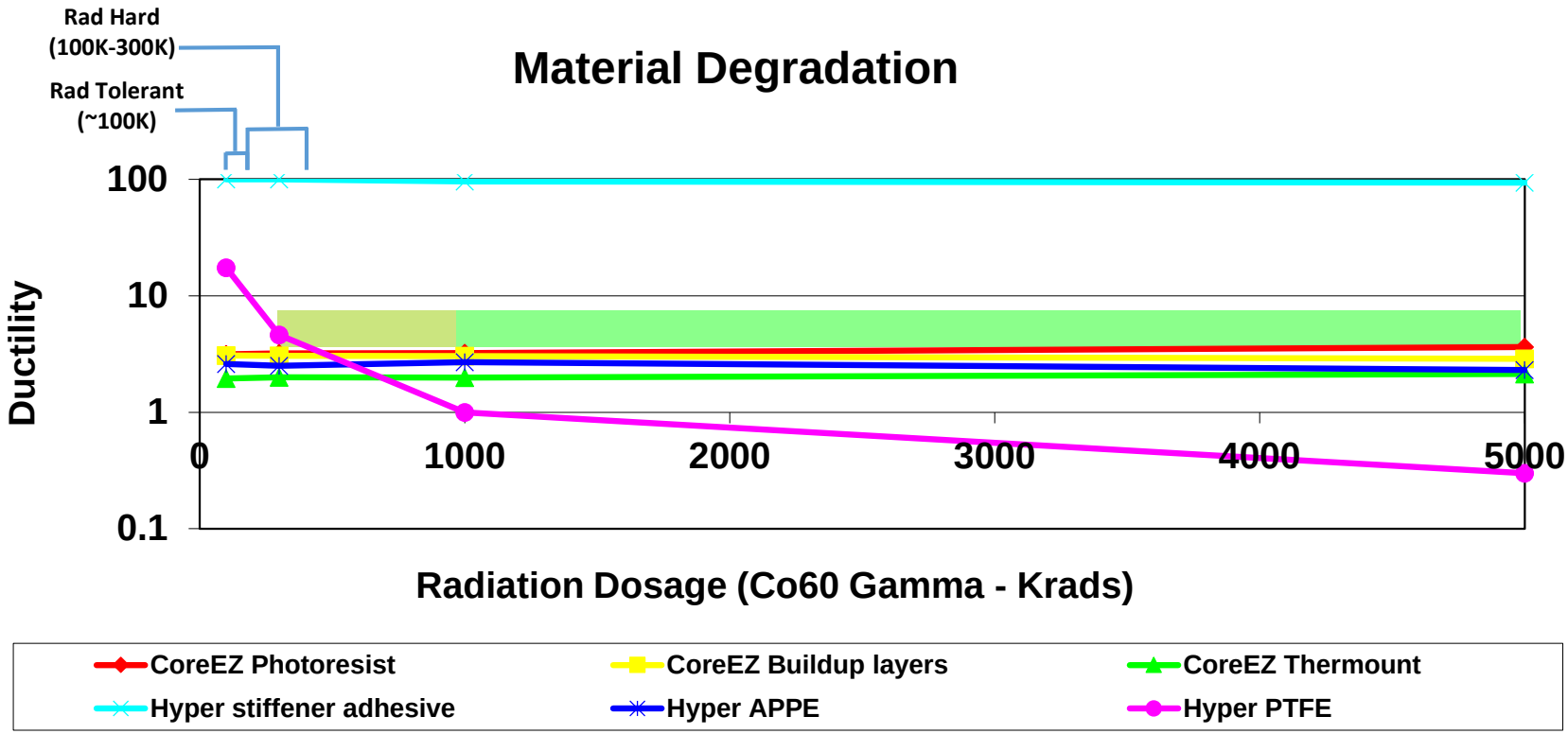


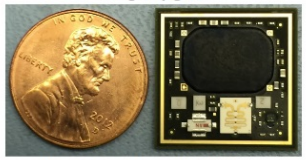
- ✓Ductility performance indicates package performance in thermal cycling
- ✓CoreEZ appears to be a good choice for Rad Hard and Strategic apps
- ✓CoreEZ Materials show no degradation with radiation level
- ✓HyperBGA appears to be best suited for Rad Tolerant applications
- ✓Hyper's PTFE degrades significantly above 300Krad exposure levels

Conclusion

COTS Technology Benefits

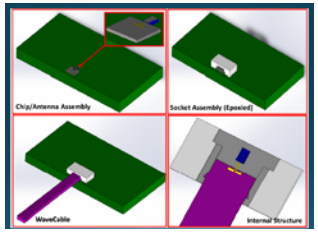
Benefits to NASA and JPL:
- ***Without any special retooling we can shrink volume and weight by 50X and power by 2X***

MCM/SiP



New Design w/COTS 148 Components Compressed into a 19mm X 19mm MCM/SiP

Benefits to NASA and JPL:
- ***New substrate technology ideal for selecting 2.5D integration***

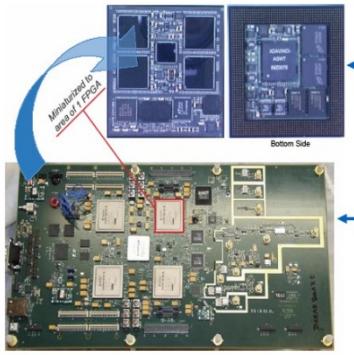


Benefits to NASA and JPL:
- ***Wave Cable increases data speed/rate***

Enabling Technology

Benefits i3 Electronics Miniaturization

- **Package Size: 55 x 55mm, 683um thick**
- **Substrate: Particle filled epoxy (CoreEZ)**
  - **X-section 3-4-3**
  - **50um vias, 30/35um Line/space**
  - **84 ft HDI wiring**
  - **>39,000 40 micron UV laser drilled vias**
- **5 Flip Chip FPGA**
- **4 Xilinx FPGA, 3264 I/O w/190um minimum pitch**
- **Discrete components: 0201 minimum size**
- **638 SMT components placed**
- **Functional final socket & Bed of Nails topside test**
- **Custom Peripheral Pin connector & Lid**



Final SiP size: 4 in²

Original PCB Size: 108 in2

27x reduction in size

BACKUP

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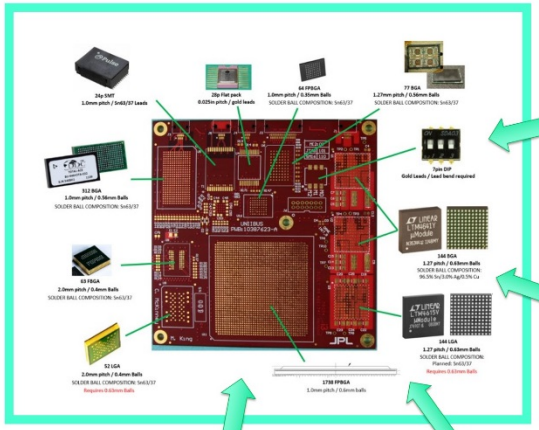
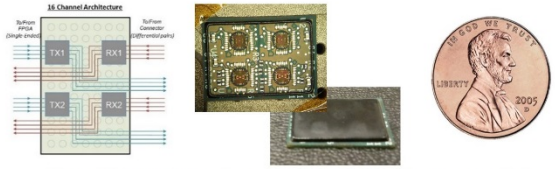
✓ Shrink - continued

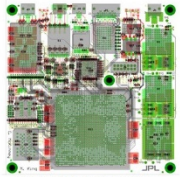
Results:

- **Validation of PWB design techniques such as Via-in-Pad. This PWB interconnect technique provides additional route area for designers when fine pitch devices are used.**
- **Fabrication techniques incorporating ENEPIG finish. This finish simplifies PWB fabrication and demonstrates mix technology solutions are viable.**
- **When COTS parts replacements are not available, SWaP solutions are still achievable. Validated with the development of the new LVDS BGA device which incorporated chip-on-board technology.**
- **Parts, Material and Processes (PMP) technical challenges can be addressed using Sherlock reliability software. Work illustrates comparison of prediction vs testing (which will be validated in year 3), ultimately saving testing cost and schedule.**





When COTS parts replacements are not available, SWaP solutions are achievable thru CoB technology – 16 channel 77 pin BGA (NPO 49525 sn# 62/077,514)

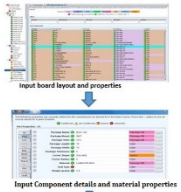


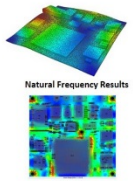
Input board layout and properties

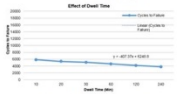
Input Component details and material properties

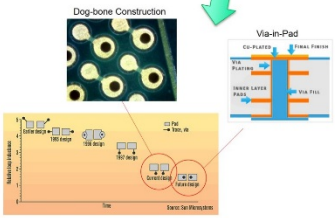
Define Life Cycle Loads
Thermal Cycling, Vibration, Shock etc

Run Analysis
(Solder joint fatigue, Displacements, Natural Freq, Strain, Harmonic and Random vib life, shock life)









Loop inductance has diminished as pad topologies have been enhanced

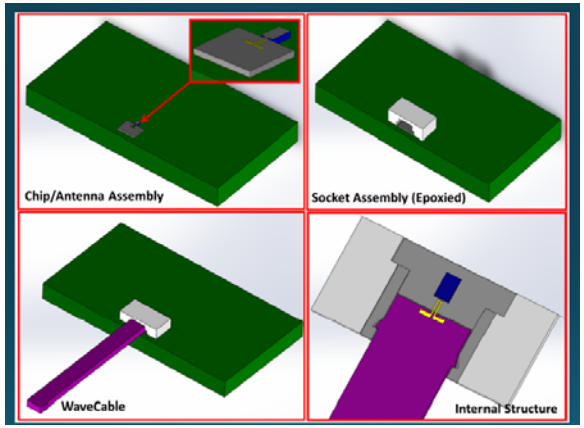
ENEPIG Reliability Conclusions

- Good Visual, Functional, X-Ray and Shear Tests
- Good Trace Durability Tests
- Versatile Finish for Wire Bonding and Sn63 Soldering

- Qualify commercial packaging technologies and materials, thru the use of Reliability Software
- Define reliability limits and generate NASA qualification data thru COTS packaging technologies.
- Understand physics of failure of commercial packaging technologies at environments relevant to NASA missions.
- Find ruggedizing solutions, ultimately extend the technology to extreme environment applications.
- Update reliability requirements, reliability test parameters, screening and test methods, and design parameters.

Snapshot Significance of Second Year Results – Take Away Points

✓ Speed Continued



Benefits to NASA and JPL:

- **Developed a complete solution for Near-Field-Connects**
- **EMI study shows only 1/100K of the mm-W signal leaves waveguide**
- **PoC have shown using CMOS chips at 60, 100 and 150 Ghz operating up to Gb/s**
- **Developed CMOS NFC Rx and Tx Chips sets.**
- **Developed multiple Coupler Interface solutions:**
  - **Chip/Antenna Assembly**
  - **Socket Assembly**
  - **Improved Lens Coupler Structure**