AAS 16-061

CONCEIVE, BELIEVE AND ACHIEVE; A PATH TO MINIATURIZATION, COTS INFUSION, AND SIZE WEIGHT AND POWER REALIZATION FOR FLIGHT

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JPL along with other aerospace agencies such as the US Air Force Space Programs [A] and a packaging technology innovator, i3 Electronics, Inc., are evaluating the use of state-of-the-art (SOA) commercial off-the-shelf (COTS) and alternative packaging technologies for future high performance and high reliability space applications. Utilization of SOA COTS technologies have resulted in large scale reduction in electronics volume, weight, power, cost and schedule with outstanding electrical performance and high reliability. We will share JPL's joint design, architectural approach, alternative substrate materials selection, associated processes, and mission assurance role in identifying reliability and qualification risks, as part of the three year Heterogeneous Packaging/Device Integration effort under the guidance and leadership of JPL's Mission Assurance Directorate [B].

INTRODUCTION

The Jet Propulsion Laboratory's (JPL) ability to meet NASA exploration and science objectives depends on the development and application of advanced technologies, as well as conducting scientific research to advance the institution's state of knowledge and chart future directions. In collaboration with program offices and other experts in science and technology fields, JPL's Office of the Chief Scientist and Chief Technologist (OCSCT) coordinates and identifies a number of strategic areas that are critical to NASA's future success, and plans and implements its investments portfolio accordingly.

This paper focuses on the accomplishments associated with the Heterogeneous Packaging/Device Strategic Initiative. Its technical objective is to demonstrate the reliability, performance and equal functionality of SOA COTS electronic technologies. Its goal is to leverage these new packaging/device technologies to solve practical JPL needs and to infuse these technologies into JPL's overall technology portfolio and capability.

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The strategic initiative structure is made up of three unique tasks:

1. "SHRINK" represents the effort to leverage SOA COTS technology to reduce size, weight and power (SWaP) [1] of an existing JPL-SOA 6U Instrument Interface electronics assembly,
2. "STACK" represents the effort to leverage 2.5D technology to reduce RF circuits for a JPL-SOA RF Radio,
3. "SPEED" represents the efforts for point to point RF link using "WaveCable/Nearfield" technology, eliminating the need for conventional dielectric cable or tube-based interconnects.

Each technology scope is based on utilizing high reliability solutions to support successful technology infusion. In addition, the SHRINK and STACK efforts leveraged the use of advanced organic substrate technologies [2] to achieve extreme electronics miniaturization. Key enablers are smaller circuiti-zed feature dimensions for lines and space widths, smaller UV laser micromachining, vias and enhanced assembly processes.

SHRINK APPROACH AND RESULTS

Transitioning Commercial Off-The-Shelf (COTS) Technologies into mainstream use at JPL demonstrates Size, Weight and Power (SWaP) Benefits

Objective

The objective of the SHRINK task was to demonstrate the reliability, performance, and functionality of SOA COTS electronic packaging by refactoring JPLs existing OCO3 Digital Processor Unit (DPU). The DPU is, part of the Central Electronic Unit (CEU), which is based on a ruggedized packaging topology in a 6U cPCI standard form factor of 260mm x 130mm into a 1U distributed form factor of 100mm x 100mm. This technology solution integrates the same functionality of the DPU and CEU functions through the use of SOA COTS electronics packaging solutions resulting in a miniature **Uni**versal **I**nstrument **Bus** (UNIIBUS). The goal of SHRINK is to demonstrate current JPL avionics architectures can adapted COTS components, yet maintain equal system performance and achieve predicted SWaP improvements. Ultimately providing an understanding of COTS limitations and margins.

Approach

Since the DPU is based on JPL heritage data bus interfaces (i.e., 1553 and RS422) the components were selected with isolated transformer applications eliminating a large number of ancillary circuitry. To refactor the low voltage digital signal (LVDS) circuitry, a new marketable 16 channel driver and receiver solution was developed. Additionally, COTS integrated point-of-load (POL) programmable buck converters were utilized to move core voltages onto the UNIIBUS to improve reliability and eliminate additional circuit card assemblies; see figure 1. Future-focused data interfaces such as Space-wire (SW), Time Trigger Ethernet (TTE) and Near-field Communications (NFC) solutions were designed to eliminate the large number of point-to-point IO's required in the original DPU design. The end result of this design effort was to create a miniature bus (a.k.a. instrument interface) that can be used with any science instrument that leverages centralized or distributed architecture applications. More details on the architecture, part selection, and reliability analysis used are provided below:

- Architecture: The approach was to provide a refactored OCO-3 DPU- based architecture that allowed for backwards compatibility that featured a Xilinx Virtex-5 based FPGA, 2GByte

SDRAM, 1553 and RS422 interfaces. The UNIIBUS solutions expanded on the Xilinx platform incorporated new bus solutions currently being evaluated at JPL, (i.e. Spacewire, Time Triggered Ethernet, near field communication) with additional 64GByte NAND flash memory. Additional improvements in performance and resource utilization were accomplished by adapting appropriate power conversion for the core voltages, allowing design flexibility by incorporating programmable buck converter solutions. The mechanical architecture focused around a 1U solution taking into consideration, dynamic, thermal and board layout design to meet IPC6012 Class 3/A standards with preferred producibility.

- Part selection: Significant size savings, both in board and circuitry complexity, were found by incorporating the COTS Xilinx V5 Configuration Chip with NOR flash to replace the RTAX 632pin device used as a programming startup for the FPGA. Programmable point of load converters were selected to handle the core voltages: +1.0V, 1.2V, 1.8V, 2.5V and 3.3V. Additional 64GBytes of NAND Flash memory from 3D plus was selected to improve storage over the current OCO-3 design. Since a multi-channel receiver/driver COTS solution was not available, JPL developed a 16-channel low-voltage digital signal (LVDS) ball-grid-array (BGA) solution that provided a 77% reduction in size. Since Spacewire, TTE, and NFC are new bus solutions, appropriate COTS SOA chip sets for both SW/TTE were selected and incorporated a test capable solution.

- Reliability Analysis: COTS components offer positive attributes such as- leveraging the latest SOA technology, part availability, and lower cost than military/space parts. Early recognized limitations of this approach appear to be lack of traceability, lack of quality level testing (some parameters not tested over temperature ranges), and radiation performance. From a printed wiring board design point of view, new part geometries, trace routing methodologies, Class 3/A producibility and manufacturing processes fall outside of standard JPL design guidelines. Since heritage design rules and reliability data for COTS applications are limited, a comprehensive assessment of circuit card design (i.e. inner layer interconnects, solder joint and empirical reliability predictions) to establish early analytical failure mechanisms and help with design attributes or identifying design short comings was required. A new analytical software tool Sherlock, an automated design software capable of providing a comprehensive assessment of early stage circuit card design along with an ability to meet quality, reliability and long-life expectations, was used for reliability predictions.

The next challenge was to develop a printed wiring board design based on SOA COTS parts selected, and maintain board design methodologies based on a Class 3/A producibility and manufacturing processes enabling JPL use of current approved suppliers. In some cases geometries fell outside of standard JPL design practices, pushing focus around commercial geometries that would fit within JPL manufacturing process. The key attributes in the UNIIBUS PWB design that enable the use of COTS are described below:

- Via-in-Pad: JPL's current SOA for high density/fine pitch devices requires the designer to use dog-bone vias. With fine pitch devices like the Xilinx V5, it is challenging to meet IPC-6012 class 3-A requirements with dog-bone vias. Via-in-Pad allows for more routing room to meet IPC-6012 class 3/A requirements and for potential improvement in signal integrity.

- Finish-Electroless Nickel, Electroless Palladium, and Immersion Gold (ENEPIG): JPL design guidelines only allows for two finish types:

- HASL (hot air solder leveling) where a PWB is typically dipped into a bath of molten solder so that all exposed copper surfaces are covered by solder and excess solder is removed by passing the PWB between hot air knives.
- ENIG (electroless nickel, immersion gold) which consists of a nickel plating covered with a thin layer of immersion gold.

Planarity can be inconsistent with HASL resulting in attach process challenges for placing fine pitch BGA or CGA devices. ENIG has good planarity characteristics, but is not allowed for CGA/BGA due to black pad concerns (black pad occurs when there is hyper-galvanic corrosion of the nickel layer during the gold plating process thereby creating a potentially latent defect).

- Electroless Nickel, Electroless Palladium, and Immersion Gold (ENEPIG) finish has good planarity characteristics. Black pad concerns are eliminated with the protection of the palladium layer over nickel. In addition, the electroless process also provides self-limiting gold plating thickness that eliminates the risk of excessive gold in solder. The key attribute of ENEPIG is the ability to use chip-on-board (CoB), wirebonding, and solder technologies on a single assembly [3].

- Manufacturing Processes: The UNIIBUS Assembly utilizes a variety of different package types; from standard flat pack (gull wing) parts to, standard land grid arrays (LGA) to fine pitch and standard pitch ball grid arrays (BGA). Planning for the manufacturing attach process was based on the ability to survive 1000 thermal cycles from -55^{0}C to +125^{0}C. We chose to use i3 Electronics to assemble the UNIIBUS units based on the ability to leverage modern techniques such as underfill for the LGA parts. The manufacturing process will be validated during thermal cycling and compare results to the Sherlock predictions.

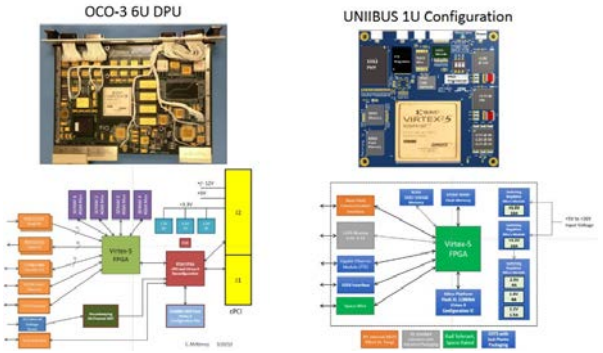


Figure 1 - JPL SOA Architecture Vs COTS

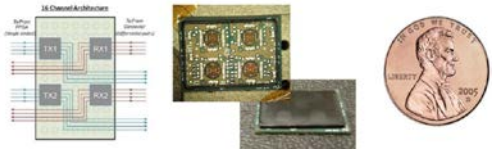


Figure 2 - COTS MCM/CoB

COTS – MCM/CoB

JPL's motivation to develop a custom integrated COTS LVDS device was based on the problem that current space qualified LVDS drivers and receivers are only available in individual 14 pin ceramic flat pack, or other similar package type, (i.e., either four driver or four receiver channels per package). Most electronic designs employed by NASA/JPL require several channels of both transmitted and received data, and thus require several pairs of driver/receiver 14 pin packages, ultimately taking up several square inches of limited PWB area. No electronic part that combines driver and receiver circuits into a single package device is available on the market.

SOA chip-on board technology was leveraged, which combines 2D manufacturing along with matched driver and receiver die to create an LVDS solution that provided a 77% improvement in density. As shown in Figure 2, the new 16 channel 77 pin BGA-LVDS device was architected with single-ended signals to an FPGA and differential pairs to an IO scheme. Power and ground were partitioned so one "quad" driver and one "quad" receiver were connected to each power/ground plane pairs for added design flexibility. The power enable/disable signals for each quad driver/receiver were pinned out allowing the user of the targeted circuit to minimize the quiescent current and channel enable/disable capability.

The LVDS substrate technology selected for the electronics package is a key enabler towards achieving SWaP reduction. High density substrates fabricated from thin particle containing organic laminates are a good alternative to standard PWBs that contain glass cloth reinforced dielectrics. Figure 3 shows a cross-section comparison of i3's silica particle filled epoxy-based CoreEZ® thin laminate compared to a standard build up PWB. The absence of glass cloth in the dielectric provides several distinct key advantages including reduction in thickness, tighter core via pitch, and improvements in assembly yields and reliability. The absence of the glass cloth also results in a smoother surface finish on the particle filled dielectric, enabling higher resolution photolithography for finer line widths and spaces, and improved electrical performance, especially for high speed applications. Laminate materials that do not contain glass cloth, unlike typical printed circuit board laminate materials, allow for the formation of smaller vias by UV laser drilling as opposed to more conventional vias formed by mechanical drilling of the glass cloth containing cores, and CO_2 laser drilling of blind vias for interconnection in the buildup layers. The smaller via size minimizes capture pad area requirements and enables a much greater via density, resulting in substrate size reduction as compared to conventional PWB technology with glass cloth reinforcement.

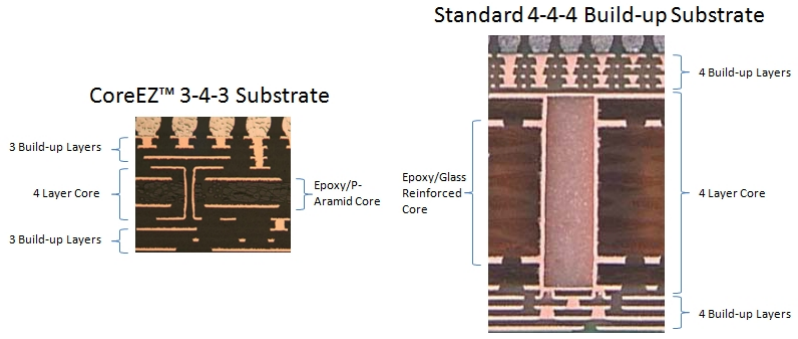


Figure 3. Comparison of standard sequential build up structure (right) with CoreEZ sequential build up (left), illustrating the impact of a denser, thinner core on overall substrate thickness.

The final delivery challenge considered two different approaches; in-house design-build (based on current JPL rules) and an i3 enabled design-fab-assembly (leveraging SOA capabilities). The in-house design approach required JPL approved PWB vendors to push the capabilities of producibility which did not meet IPC-6012 class 3/A requirements and resulted in non-functioning PWBs. Utilization of i3 Electronics SOA PWB capability allowed for fine feature geometry design and producibility which lead to the delivery of 10 functional LVDS units, see figure 2.

New Reliability Tool

Early studies [A] recognized limitations with COTS parts; lack of traceability, lack of quality level testing (some parameters are not tested over temperature ranges) and radiation performance.

Since heritage design rules and reliability data for COTS applications are limited, a comprehensive assessment of circuit card design (e.g. inner layer interconnects, solder joint and empirical reliability predictions) are needed to establish early analytical failure mechanisms and help with design attributes or identifying design short comings. This analysis was conducted on the UNIBUS board using Sherlock 4.1 software. Sherlock is virtual simulation software that has the capability to model the electronic printed wiring board (PWB) and components to predict their reliability. The software is widely used in industry for virtual simulation and life prediction analysis. Some key feature of the software is its ability to simulate printed circuit board and components. Once the component information is entered in the software, analysis can be run in minutes and a parametric analysis could be performed. The tool is useful in optimizing design parameters, life prediction of interconnects and understanding the effect of several load types such as thermal cycling, vibration and shock.

Results

The use of COTS solutions developed shows significant reduction is volume and mass over the existing OCO-3 DPU/CEU. Figure 4 shows the SWaP Comparison validating the large scale reductions predicted in electronics volume, weight, and power (SWaP) with an assembled demonstration units. Additionally, the goals were satisfied with several accomplishments;

- Validation of PWB design techniques such as Via-in-Pad. This PWB interconnect technique provided additional route area for designers when fine pitch devices were used.
- Fabrication techniques incorporating ENEPIG finish. This finish simplified PWB fabrication and demonstrated the viability mix technology solutions.
- Commercial assembly and process techniques using modern PWB design and finish techniques were validated building three UNIIBUS assemblies.
- All three UNIIBUS Assemblies where delivered to the testbed and verified 4 out of the 9 functions (at the time of writing this paper), and are on track to start thermal cycle testing in March 2016, see figure 4a.

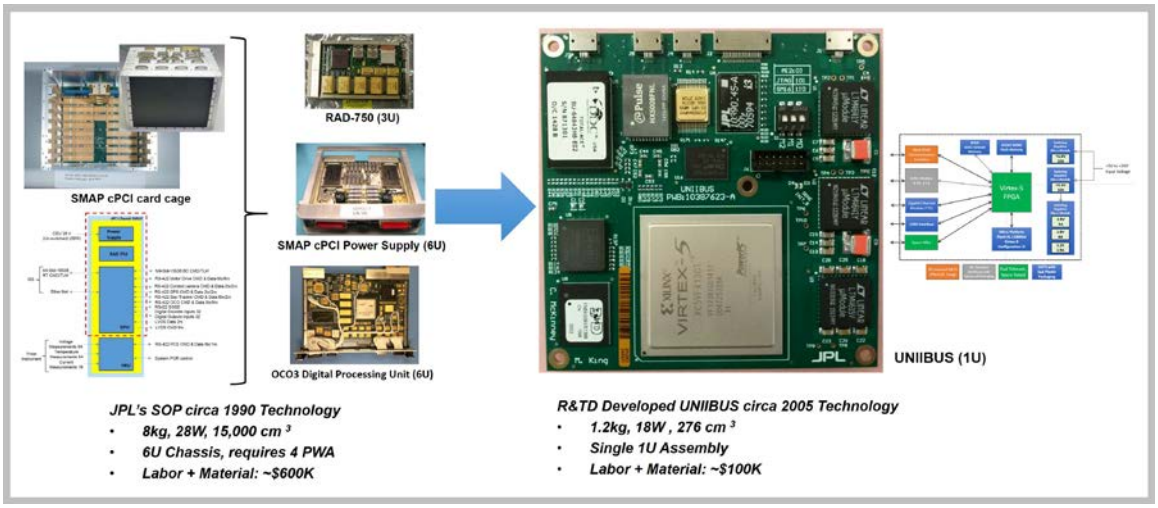
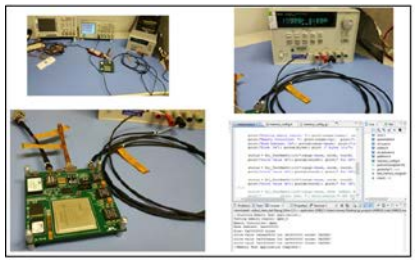


Figure 4. Current Snapshot of JPL Vs Industry State-of-Practice (SOP).



Tasks	Completion/ Date Expected	Details
Build Nanonics Cables	Done	Built x3 Ethernet, x3 Power & x1 LVDS loopback cables.
Verify POL Converters	Done	Verified 1v, 3.3v, 2.5v, 1.8v & 1.2v. ~3.8watts idle.
Verify JTAG & FPGA Functionality	Done	Virtex 5 successfully programs via JTAG.
Verify 4Gb DDR2	Done	Tested DDR2 @ 200mhz via Microblaze Memory Test Application.
Verify NAND Flash	[illegible]	Hardware interface & drivers done. Testing in progress.
Verify LVDS	[illegible]	Hardware interface & drivers done. Testing in progress.
Verify 1553	[illegible]	Hardware interface done. Drivers & testing in progress.
Verify Ethernet	[illegible]	Hardware interface done. Drivers & testing in progress.
Verify Spacewire	[illegible]	Hardware interface in progress.
Design IN-SITU Test	[illegible]	Plan to test all interfaces via commands over Ethernet to Microblaze on FPGA.
Deliver UNIBUS PWA's	[illegible]	Delivery to Don Hunter for Thermal cycling. Bootable ROM on board for IN-SITU testing via Ethernet.

Figure 4a. Testbed activity verifying UNIIBUS functions.

STACK APPROACH AND RESULTS

Multifunctional Electronics Core Substrate – Configurable Electronics Functionality with Stacked Silicon and Multi-Chip Modules

Objective

The objective of the stacked effort is accomplished by leveraging and adapting the rapidly growing field of advanced 2.5D and 3D interconnect technologies. These technologies include Through-Silicon-Via (TSV), Through-Polymer-Via (TPV), and silica resin-based interposers. A custom multifunctional core substrate scheme comprised of next generation polyimide, ceramic and/or silicon materials will be designed to integrate these new 2.5D and 3D interconnect technologies into an extremely miniaturized space qualified radio. Initial engineering studies determined that implementing a circuit redesign that utilizes custom Monolithic Microwave Integrated Circuits (MMIC) would yield the largest volume reduction. Due to very large cost of custom MMIC development, with estimates of $350-500K in development costs for each device, a decision was made to use only Commercial-Off-The-Shelf MMIC's available for approximately $3-5K.

Approach

The direction of this task was to evaluate the JPL developed IRIS radio electrical schematic complexity, the selected component packaging, and identify a path to miniaturization by selecting a portion of the schematic for miniaturization and electrical performance validation. Due to very high design and fabrication costs, silicon interposers were not chosen and the technology alternative chosen was a copper epoxy resin technology, tradename CoreEZ.

Electronic Circuit Evaluation and Integration

The baseline IRIS radio consists of a 4 slice stack that includes a Processor Board, Power Board, X Band Exciter Board, and X Band Receiver Board, less the antenna board. The primary focus is the X Band Exciter Board. The Exciter Board is a 10 layer design with 514 individual packaged surface mountable components and represents the most complex board for miniaturization of the IRIS radio. The Exciter Board RX_LO portion of the Exciter slice was selected for expanded integration. See Figure 3 that depicts the hardware physical size reduction of the of the RX_LO circuit integrated into a high density MCM package. This was accomplished by using integrated circuits in bare die format (without their respective individual component packaging). This circuit is comprised of approximately 1/3 of the Exciter IRIS radio slice.

Functional Evaluation of MCM Test Circuit Electrical Performance

The RX_LO MCM was mounted to a test board to allow simulation in a radio. Functional electrical test results are shown below:

1. Output Power (-3dBM)
2. Frequency Tuneability (Synthesizer) swept receiver
3. MCM was tuned across the necessary bandwidth (7GHz center w/200 MHz bandwidth)

4. Tested and verified functionality and programmability (programmed the PLO, PE97632)
5. Tested harmonics (>45dB rejection)
6. Verified loop stability (via phase noise and output spectrum)
7. Phase Noise (<90dBC/Hz@ 100KHz offset)

Electrical Redesign of the Exciter Board

The direction of this task to reach extreme miniaturization was consistent with integrating most of the electrical schematic from a distributed circuit into a Monolithic Microwave Integrated Circuit (MMIC) approach. The current IRIS radio distributed circuit design is a relatively small volume electrical package by current JPL standards. This includes printed circuit boards (10cm x 10cm) that are comprised of many packaged devices. The advantage of this approach is it is easily tested, tuned and reworked and the cost of hardware is relatively inexpensive. It consists of approximately 59 integrated circuits such as hybrid couplers, power amplifiers, operational amplifiers, vector modulators, inverters, voltage controlled oscillators, planar attenuators, IC drivers, switches and sensors. The challenge was to modify and redesign the electrical circuit compressing the current physical board layout dramatically. This can only be achieved with a design that contains multiple devices and functions on a silicon or gallium arsenide chip. These chip scale devices can be placed on a silicon interposer or daughter substrate that replaces a large organic substrate such as a polyimide PCB to route the large number of input/output signals necessary to integrate to the multifunctional core substrate. Hence, a new design approach that would facilitate extreme miniaturization is converting the electrical schematic to a custom MMIC design. The primary advantages are extremely small electronic packages and extreme miniaturization, the primary disadvantage is a very high development and fabrication cost. Developing a custom MMIC solution and can exceed $500,000 per MMIC device. Therefore, a decision was made to redesign the Exciter Board for the IRIS radio using Commercial-Off-The-Shelf MMIC's. The cost is manageable and 10 to 15 times less expensive than a custom 125µm MMIC. It does however require a custom signal routing solution to communicate to the multifunctional core substrate. This will be accomplished with a silicon interposer with Through-Silicon-Via (TSV), and a multi-layer stack-up or with silica particle-filled epoxy resin and copper interposer.

CoreEZ® Interposers fabricated and thermal cycled for interconnection reliability

The CoreEZ™ [4] package is an organic build-up offering that incorporates a 4-layer, 200 µm thick core made of p-aramid fiber-filled Thermount® resin surrounded by silica particle-filled epoxy resin coated copper (RCC). Formation of vias in the particle containing dielectric materials are readily accomplished with UV lasers, resulting in smaller via size, subsequently reducing capture pad area requirement and enabling a much tighter core via pitch (CVP), refer to figure 6. When CVP is nearly equivalent to die bump pitch, it enables Z-escape routing to all wiring planes which can eliminate the need for additional buildup layers. This can also relax the line width and space requirements for signal routing as all of the wiring planes are accessible, thereby improving manufacturing yield. Because the core is laser-drilled, the resulting 50 µm plated UV laser drilled through holes enable smaller pitch between core vias, and subsequently reduced substrate layer counts and tighter die pad and ball grid array (BGA) pitches.

Several different material sets have been developed and successfully implemented for fully qualified production processes compliant with industrial and military standards and compatible with Pb-free assembly where required. The selection of the material set is driven by a number of factors including the electrical performance requirements, thermal, mechanical, reliability, and form factor and system integration. The particle filled, epoxy-based CoreEZ® has a total cross-sectional thickness range of approximately 0.5 mm to 0.8 mm. This highly versatile material set

can be configured to support diverse design requirements. Original implementation was based on a p-aramid fiber core, but more recently, a thin, 25 µm liquid crystal polymer (LCP) layer can be used in lieu of the p-aramid to result in a basically coreless structure with improved electrical performance and a thinner cross-section. This technology has been successfully implemented for a wide range of applications including military and Pb-free assembly, and it is also rad hard. Risk of conductive anodic filament defects (CAF) is eliminated entirely with the omission of glass cloth.

The test vehicle for this investigation was a CoreEZ® 3-4-3 substrate, refer to cross-section figure 5. The 19 mm body size substrate was designed with a 150 um flip chip bump pitch with soldermask defined (SMD), 100 um bump pad openings. Substrate thickness was 0.731 mm, the substrate had a 1.27 mm ball grid array (BGA) pitch. The die that was assembled to this substrate was a 3.6 mm X 3.6 mm flip chip with 100um ball limiting metallurgy (BLM) pad and 80 flip chip bumps. Module assembly was performed with a standard Sn63 eutectic reflow profile using OA type water washable flux. The die were underfilled with NAMICS U8437-2 chip encapsulants, and the assembly was fitted with a 17 mm nickel-plated copper cover plate that was 0.250 mm thick and attached to the die and substrate with thermally conductive adhesive. In addition, 0.762 mm diameter Sn63 BGA balls (77 x) were attached to the back side.

Obtaining high reliability in extreme applications, as measured and proven by stress testing, has numerous facets that extend beyond the scope of this paper. However, understanding the impact of fundamental design attributes, especially as related to critical properties of substrates and devices, can be very instructive to reach this goal. One of the ubiquitous problems facing flip-chip assembly onto substrates is due to the interaction between the silicon chip and the substrate; the silicon has a low linearized CTE, taken as 3.0 ppm/^{0}C that typically differs from that of the substrate, on the order of 20 ppm/^{0}C for CoreEZ. When a flip-chip die is joined to a substrate using traditional solder reflow and underfill dispense/cure, subsequent cooling back to room temperature engenders a stress response that usually results in die warpage, stress to the die owing to this warpage, and interaction stress between the die and substrate.

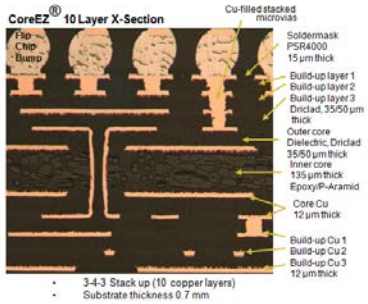


Figure 5. Photograph of 3-4-3 CoreEZ substrate with die attached. Microvias for build up can be stacked or staggered[2].

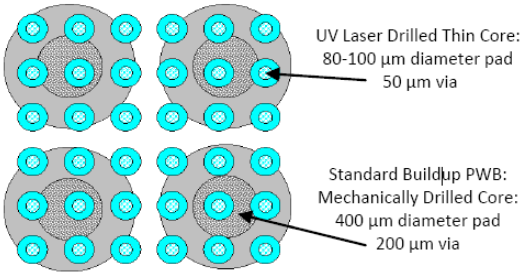


Figure 6. Core via pitch (CVP) comparison between UV laser-drilled particle-filled laminates and mechanically-drilled standard build up PWBs using dielectric core materials reinforced with glass cloth[2].

Extremely miniaturized electronics for space applications must be able to withstand multiple deep thermal excursions. This is especially true for planetary operations on the surface of Mars where electronics may have to operate between the extremes of -135°C and 85°C for thousands of cycles. The critical electrical interface between bumped silicon devices and an interposer substrate are dependent on the dice to interposer flatness, solder bump metallurgy, matched thermal

coefficients of expansion and the correct underfill. At the time of this report a single RX_LO MCM is being thermal cycled from -55°C to 100°C. It has currently been through 200 temperature cycles and will be functionally electrically tested at 250 cycles; if there are no significant output parameter changes it will be thermal cycled for an additional 250 cycle and tested again.

Results

The basic electrical performance and interconnection reliability was verified with hardware comprised of silicon chips and BT resin organic substrates. This paved the way for further integration and increased circuit complexity. The validation of RF signal performance in a Multi-Chip Module with a RF circuit is critical to establishing the direction for continued electronics miniaturization. The effort expanded from a very simple circuit to a moderately complex MCM that incorporates 148 devices in a 19mm x 19mm area. This level of packaging miniaturization has never been done before at JPL. Electrical performance testing was excellent with results depicted Figure 8. The baseline circuit was compressed from its original circuit board layout. The test results are an excellent indication of RF performance feasibility in a 2.5D MCM package. Interconnection reliability testing will be complete in the first quarter of FY16 up to 1000 thermal cycles.

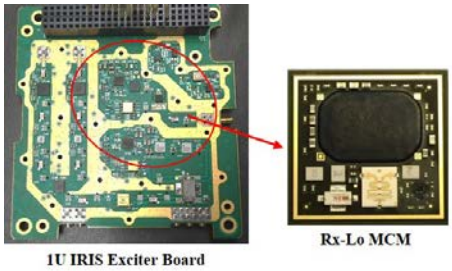


Figure 7 – Circuit area for MCM refactor

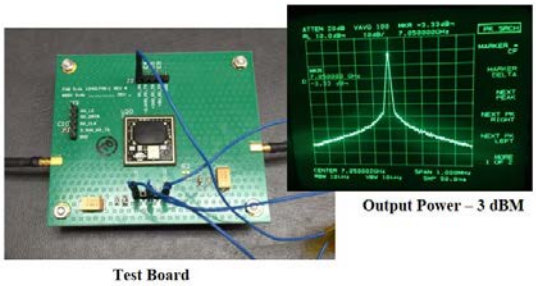


Figure 8 – MCM Electrical Testing

SPEED APPROACH AND RESULT

94 Ghz Data-Link Based on Dielectric Ribbon Interconnects

Objective

The objective of the Speed focuses on high bandwidth multi-Gb/s point to point non-free space Millimeter-wave (mm-wave) communication up to 10 meter. Dielectric ribbons allow direct coupling from a transceiver with either an on-chip probe or antenna structure placed nearby the ribbon's end. The transmission through a dielectric ribbon does not rely on an electrical contact as traditional copper interconnects allowing reduction in overall payload weight. The work discusses a prototype dielectric ribbon system for aerospace spacecraft inter-module data links which offers multi-casting capabilities, where one source can simultaneously transmit to many receiving nodes [5-7]. While the commercial market is driven by high data-rates, this prototype link is more modest, operating at data rates of 10 Mb/s which is comparable with the typical signaling interfaces found in spacecraft systems.

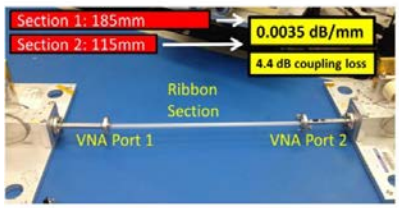
Approach

HDPE (High Density Polyethylene) was selected for the dielectric ribbon, both for its lightweight properties as well as its relatively high melting temperature. To characterize the proposed dielectric ribbon we first optimized the dimensions using CST (Computer Simulation Technology) and then fabricated several straight ribbon sections to characterize the insertion losses as well as coupling losses. Final dimensions were selected as 3mm (E-plane) x 1.5mm (H-plane). Two

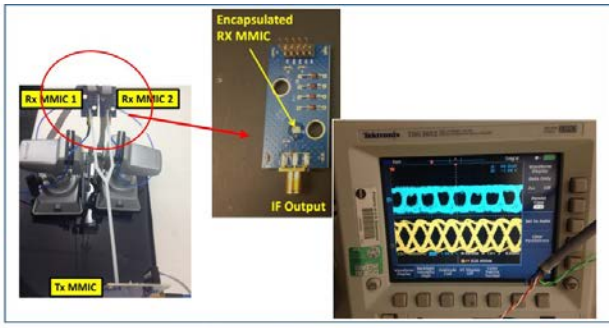
measurements of the same dielectric ribbon with two measurements different lengths (115mm and 185mm) directly coupled through open WR-10 rectangular waveguide were performed using a vector network analyzer. By de-embedding the length difference between the two measurements, the loss per unit length, and the coupling losses of the ribbon we extracted from the test sections as summarized in figure 9.

Results

The proposed dielectric ribbon was constructed with the arrangement shown in figure 10 where two receiver MMIC's are placed on the output ports of the power splitter, while the input port was excited with the Tx MMIC. The transmitter and receivers were connected to a 10BT ethernet signal source (802.3.3) between a laptop and a router in order to perform a connectivity test. Figure 6 shows the recorded eye-diagram as a streaming video is transferred across the ethernet-link formed by the dielectric ribbon operating reliably at 10 Mb/s with a bit error rate better than 10^{-12}.



HDPE Ribbon Characterization



Test Setup with Tx-Rx MMIC and HDPE Ribbon Data-link

Figure 9 – HDPE Ribbon Characterization **Figure 10 – WaveCable Electrical Testing**

CONCLUSION

Each technology scope described under SHRINK, STACK and SPEED achieved its technical objectives and goals as noted in the task results. Demonstration shows SOA COTS electronic technologies can have equal or improved performance and equal or improved functionality in regards to SWaP improvements. Future efforts planned this year, hope to show equal or improved reliability through environmental testing.

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PUBLICATIONS AND PRESENTATIONS

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[B] D. Sheldon, "DRD 5X Strategic R&TD Initiative Review – Heterogeneous Device/Packaging Integration Architecture," presented to JPL, Pasadena, CA, August 25, 2014.

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