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Determination of Outlier DDR2 Devices for Improved Space Missions

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Outline

- The problem we're trying to address
- Reliability vs. acceptance testing
- Test equipment
- Reliability test results
- Acceptance/outlier test results
- Conclusions

Problems in Flight

- On SDRAMs, but the concerns carry over to DDR/2/3
- Memory region with significant increase in bad bits
  - Not observed in ground testing (simple all 1s/0s)
  - Observed shortly after launch
- Memory bits with “stuck” behavior
  - Only a few bits observed in more than a year
  - Not observed in ground testing (again, simple 1/0)
  - Observed at different times after launch (some within a few hours)
- Memory bits with weak/stuck behavior
  - A few bits observed to not work well at 125°C – more complex patterns
  - (Commercial parts specified only to 85°C)
  - Study of behavior indicates this is probably just the point where the weakest bits start to manifest – so we now have data on this

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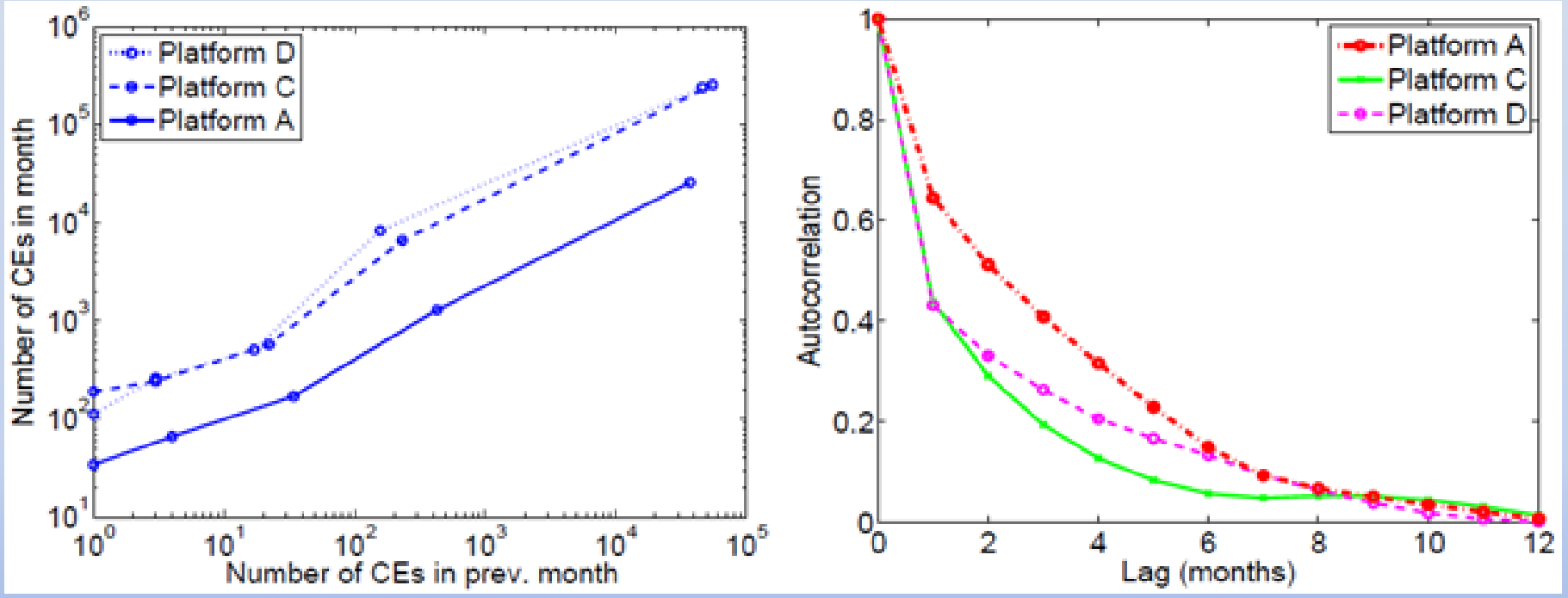
Behavior of Devices in the Field

- DDR2 devices in Google's fleet used to observe field failures of devices (isolated to DIMMs)
- Failures were bit errors that were temporary or permanent
- Once a DIMM started showing errors it was much more likely to continue showing errors



Schroeder 2009

Reliability Testing

- Provided failure mechanisms are known, prototype and final production components can be tested for known reliability issues.
- We have found it difficult if not impossible to get this data.
- Given the nature of the business, the manufacturer must ensure high reliability of their devices.
- Due to our limitations, we have not been able to identify useful reliability testing that can be performed for flight projects.

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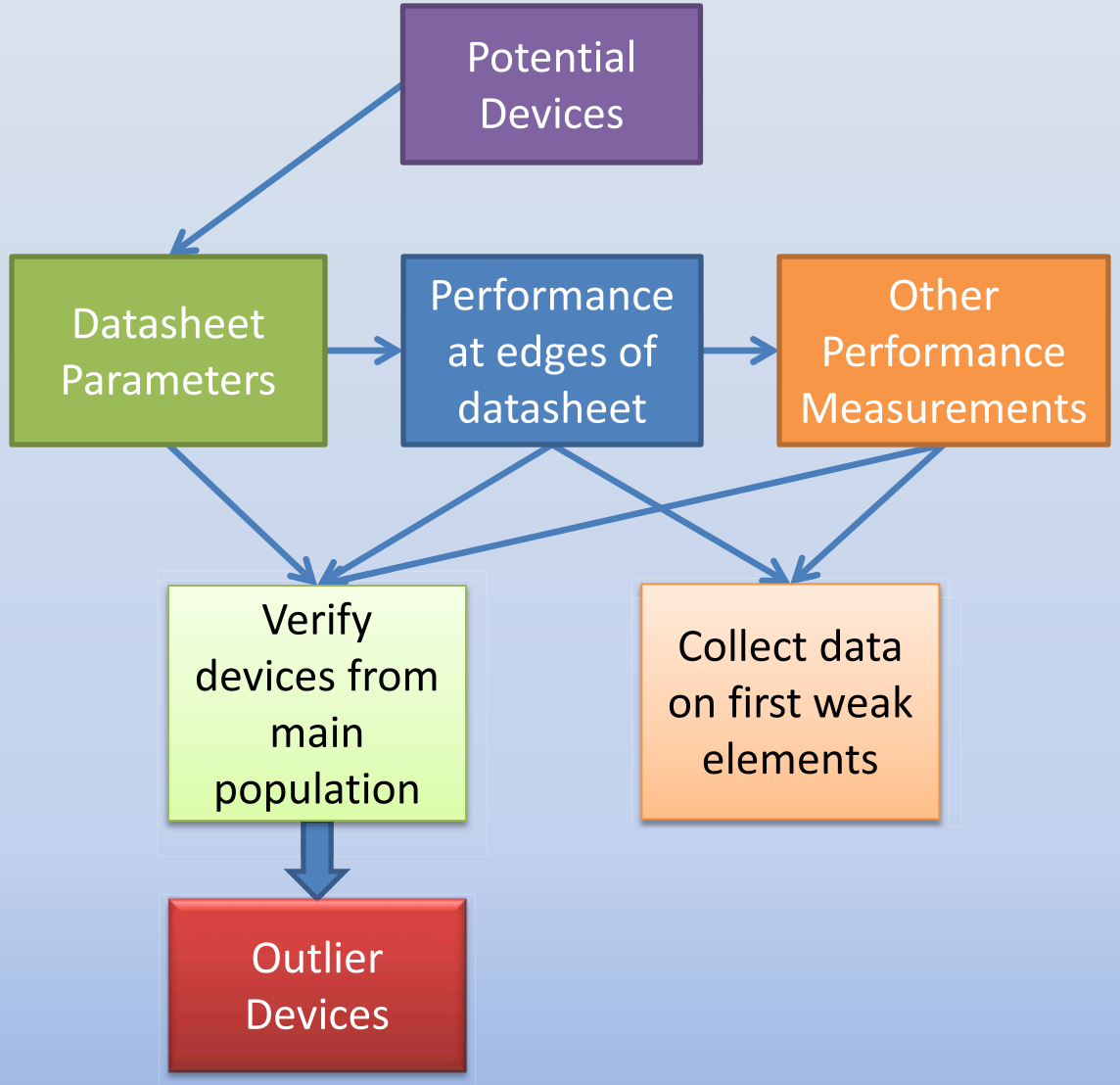
Acceptance Testing

We determined the most effective approach is to use test equipment to ensure used devices are from the main population – **not outliers.**



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Getting (*Reasonably) Good Test Parts

- Manufacturers will sell you wafers
  - You have to get them packaged yourself
  - Unclear of reliability impact
- Small order vendors will sell parts
  - about 30$ each
  - No single lot likely to be
- Testing for outliers requires 100+ parts, for life testing requires at least 5 parts per test condition (should have more)
  - Realistically, need between 100 and 300 parts
- Only viable choices for buying parts:
  - Get wafers (200+ parts) and package them, then test packaging (~50$ ea)
  - Purchase tape/reel (1000+ parts), then sample for multiple populations (~7$ ea)
  - Purchase DIMMs (8 parts at a time), and accept coupled behavior and multiple populations (~5$ ea)
- For this work, we use DIMMs, for flight projects it is probably best to use reels

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Test Equipment – Acceptance Tester

- Eureka DDR2 system
  - Enables testing of DIMMs and loose devices using an adapter
  - Can be used to quickly perform standard acceptance testing
  - Can also perform shmoo testing across various operating parameters

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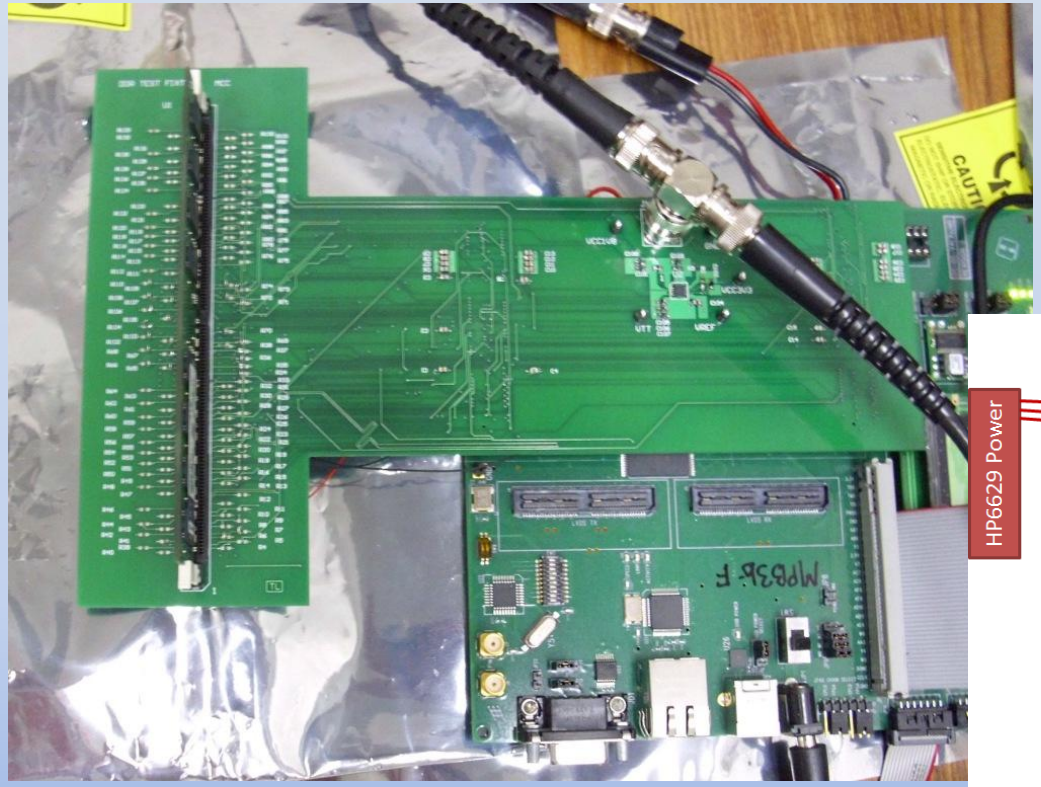
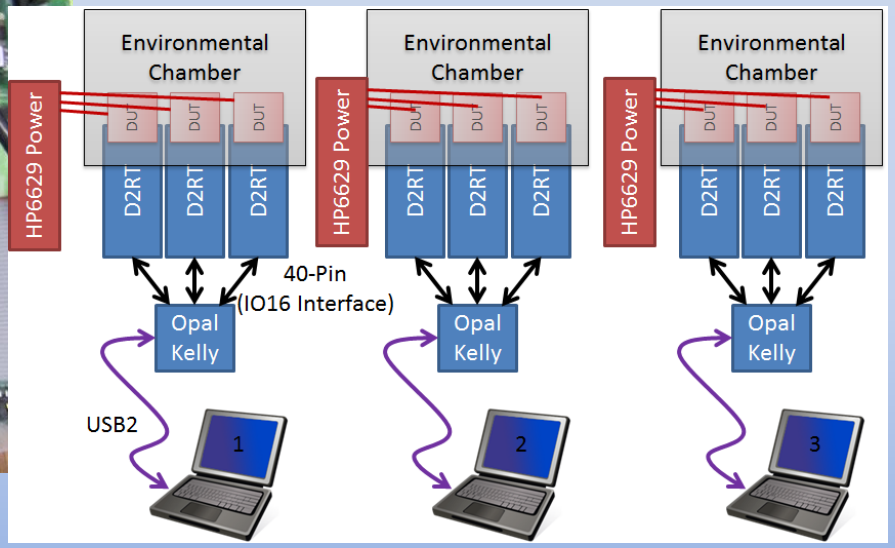
Test Equipment – Characterization Boards

- Outlier devices are about 0.1 to 1% of the population.
- Characterizing 100s of devices for >1 week each requires high volume capability.
- We developed an FPGA board that can take DUTs placed into DIMM adapters.





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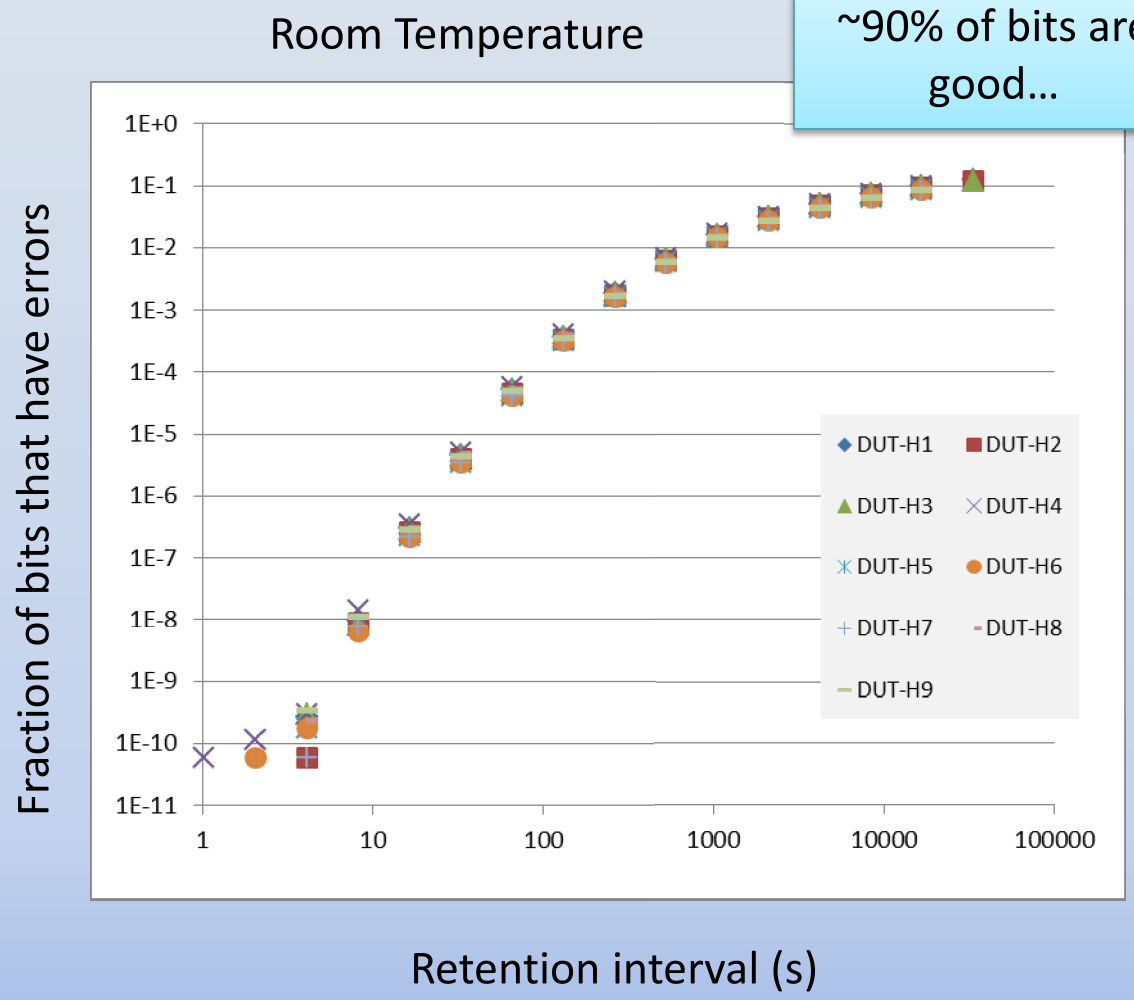
Retention Measurements

- Data is stored in the DUT
- The device is not operated for a given time – the retention time
- The data is then read out.
- The full scan runs from ms to hours.

Even at 8 hours, ~90% of bits are good…



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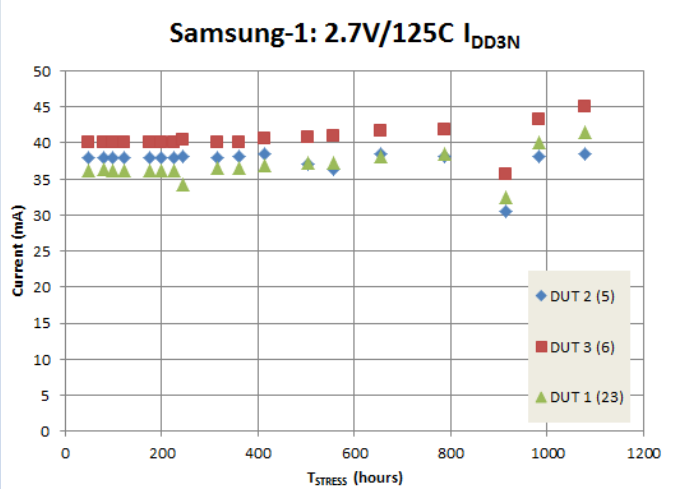
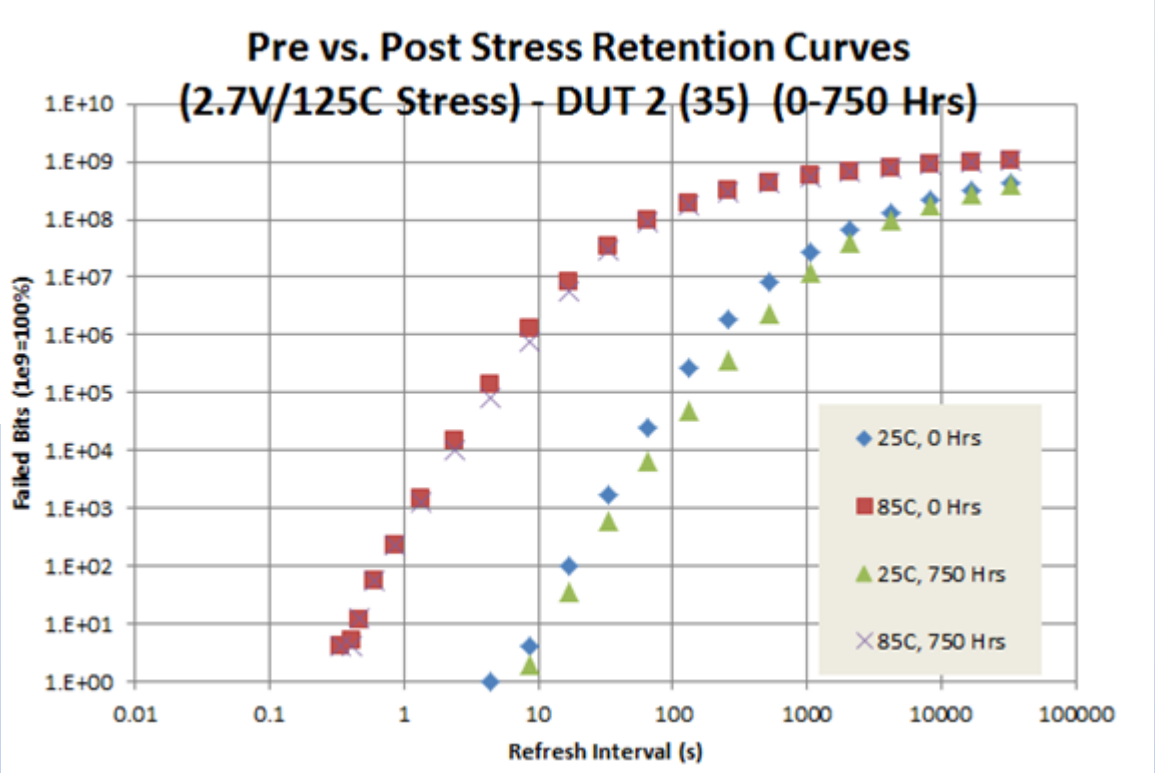
Life Testing – on individual devices





25°C = room temperature
Which was not well controlled

Note that in the 20-200s range, the life testing improved cell retention

- Goal was to perform testing against many test conditions, in order to identify the activation energy of failure modes. But testing was not targeting outlier devices.
- 1000 hour life testing resulted in some changes in operating currents
- However, the ability for cells to retain data was unaffected and we were not able to activate any failure mode that may be seen during flight

IDD Measurements

- Easiest quick verification of overall health.
- Standard readings, specified in datasheets.
- Testing can identify outliers and establish a baseline for life testing.

IDD Item	Description	Specification (mA, at 800 MT/s, CL=6) Micron	Samsung	Hynix
IDD0	Operating One Bank Active-Precharge Current	65	45	75
IDD1	Operating One Bank Active-Read-Precharge Current	75	51	85
IDD2P	Precharge Power-Down Current	7	10	10
IDD2Q	Precharge Quiet Standby Current	24	20	32
IDD2N	Precharge Standby Current	28	25	45
IDD3P	Active Power-Down Current	20	23	25
IDD3N	Active Standby Current	33	37	55
IDD4W	Operating Burst Write Current	125	72	170
IDD4R	Operating Burst Read Current	120	80	160
IDD5	Burst Refresh Current	145	105	170
IDD6	Self Refresh Current	7	10	10
IDD7	Operating Bank Interleave Read Current	210	160	230

*Note – testing here performed on DIMMs with 16 devices (8 active at a time, with others in standby)

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IDD Observations

- Typical IDD measurements for our DIMMs (Hynix shown)
- All DIMMs show essentially the same IDD behavior
- No outliers observed by this method
  - but 16-at-a-time may have obscured some

	Datasheet Spec										
	1 Part	8 Parts + stdby	H12_1	H12_2	H12_3	H12_4	H12_5	H12_6	H12_7	H12_8	H12_9
IDD0	75	680	378	376	369	375	378	375	378	375	371
IDD1	85	760	457	447	437	447	431	439	445	443	437
IDD2P	10	160	66	66	65	66	67	66	66	66	64
IDD2Q	32	336	176	175	172	202	178	175	177	173	171
IDD2N	45	440	174	172	170	172	175	172	174	170	168
IDD3P	25	280	62	64	60	64	64	62	64	62	60
IDD3N	55	520	544	541	533	535	542	533	544	539	529
IDD4W	170	1440	**533**	**425**	**517**	**414**	**541**	**531**	**521**	**519**	**400**
IDD4R	160	1360	**1310**	**1281**	**1287**	**1173**	**1308**	**1146**	**1259**	**1269**	**1322**
IDD5	170	1440	847	851	833	835	847	835	841	839	830
IDD6	10	160	37	37	37	37	37	36	37	37	35
IDD7	230	1920	427	441	429	427	439	433	431	437	421

Strange variation in IDD4 occurs in all manufacturers tested.
May be due to tester.

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Shmoo Testing

- Tested DDR2 DIMMs for voltage and frequency ranges – to identify any devices out of family.
- Very reproducible results – Samsung shown
- Interesting gap between 333 and 400 MHz

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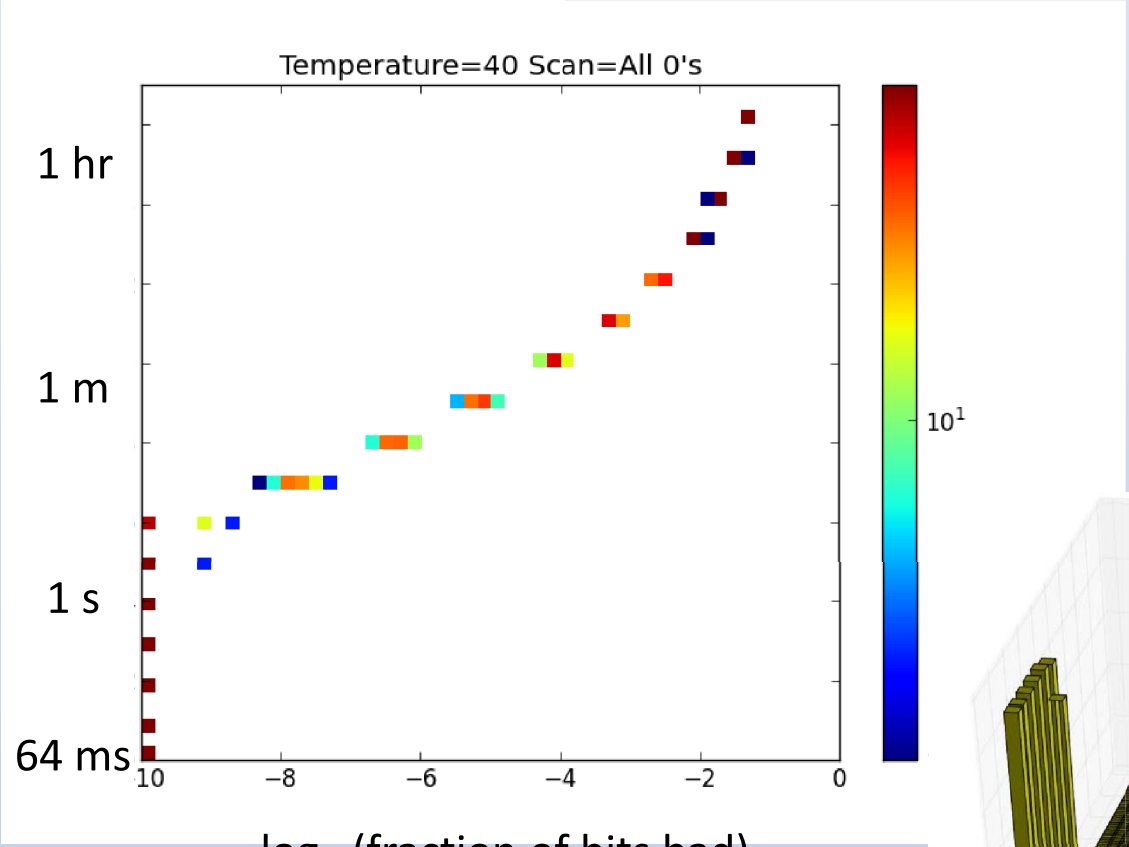
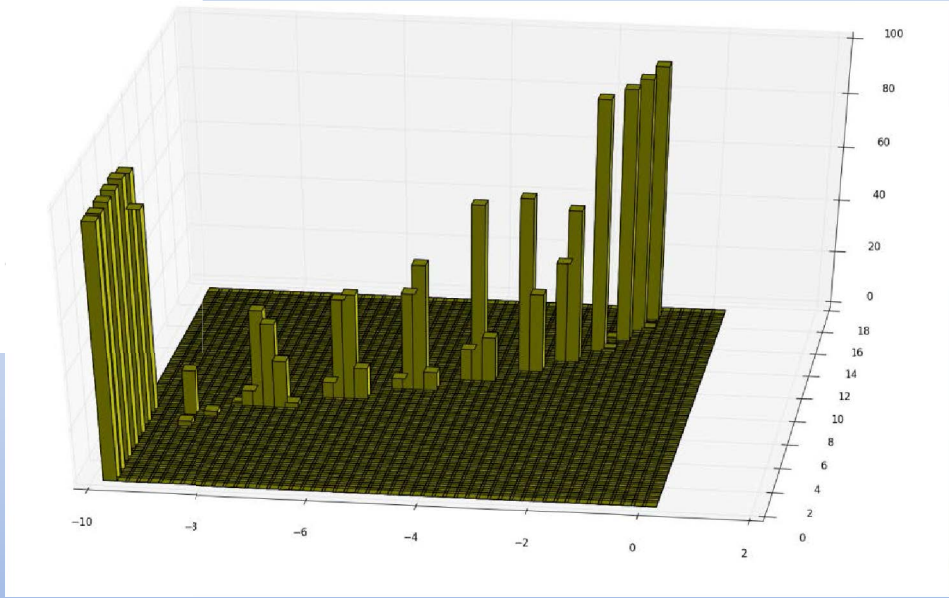
Nominal Retention Scan
- using all 0s, 40°C, on Hynix DIMMs



$\log_{10}$(fraction of bits bad)



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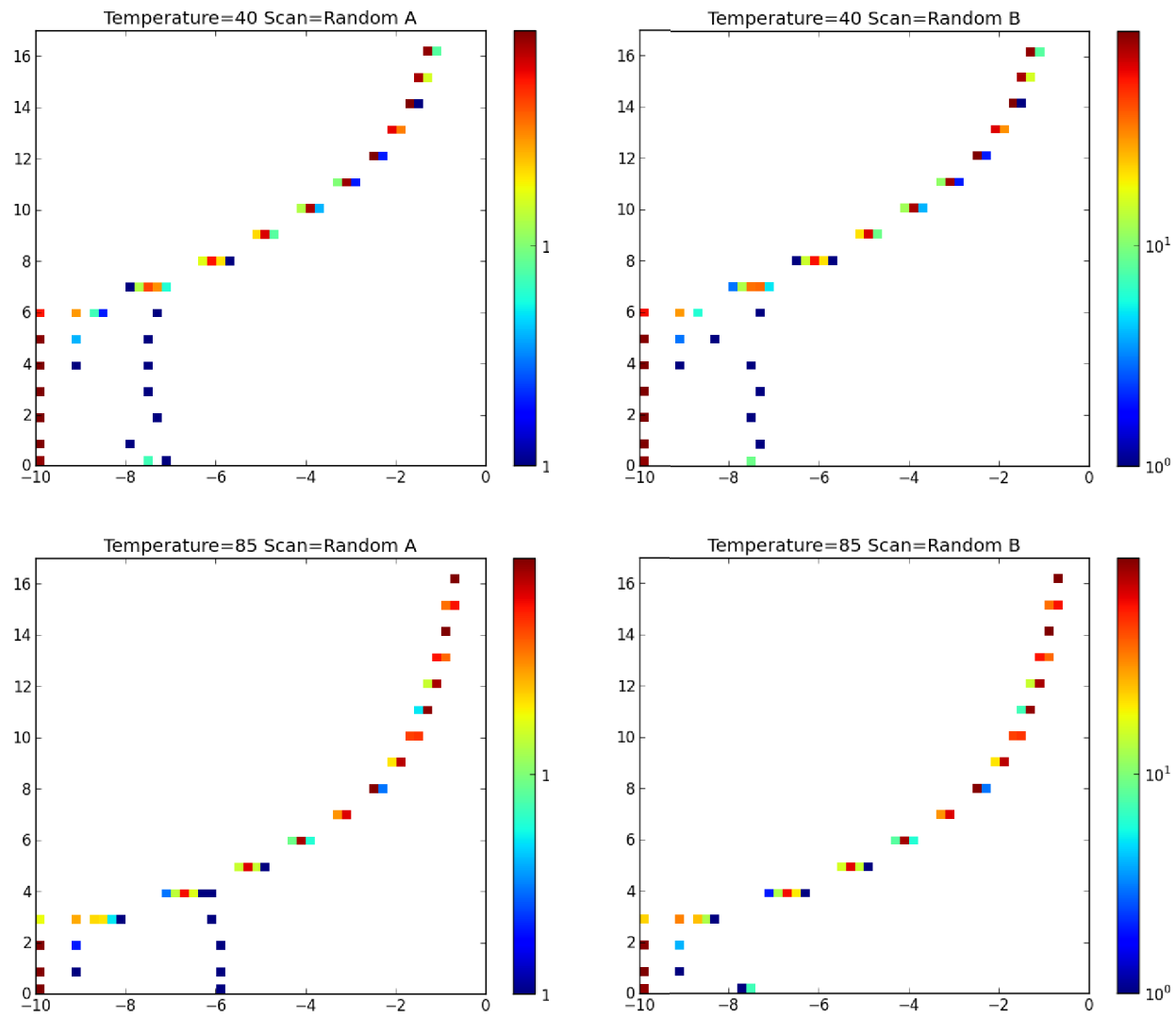
Effect of Random Patterns - shows bits with problems at 40°C

- Random patterns showed clearest sign of pattern sensitivity.
- Even one of the random patterns did not show weak bits under all conditions.
- Note that the "bad" parts join the main population as retention time increases.



Conclusions

- Rates of ~1% for DDR(2) devices with outlier behavior are expected.
- In order to explain flight anomalies it is best to have detailed performance information on devices prior to launch
  - Particularly for performance of storage bits
  - Including data retention tested with complex patterns
  - This is data we can take that the manufacturer cant due to time/cost
- Testing has shown:
  - 1000 hour life testing of limited value (not rejected but expensive and likely shows nothing)
  - All devices handled all 0s/1s and “checkerboard” patterns fine
  - Found 1 out of 144 devices with difficulty handling random patterns
- Additional recommendations
  - Be ready to identify the actual worst bits (first 100 or so) on each part
  - Although outliers can simply be discarded, it is also possible to recommend flight rules to improve operation
- Will be studying more DDR2 and DDR3 devices for NEPP