G12 Task Group No. 2010-01 Class Y: A New QML Class for Non-Hermetic Space Products

Task Group Meeting No. 8

Columbus, October 1, 2012
DRAFT

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Agenda

- Current Status (S. Agarwal)
- TG Effort at a Glance (S. Agarwal)
- Road to QML-Y Flight Parts Procurement (S. Agarwal)
- DLA-VA Class Y Status Update (M. Akbar)
- Other Comments (L. Harzstark, D. Sunderland)
- Invited Presentation – BAE
- Wrap up (S. Agarwal)

- Attachments:
  - Section Y: Task Group 10-01 Summary

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Progress Status

- DLA-VA **completed** Engineering Practice (EP) Study.

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38535 QML Space – Current Status

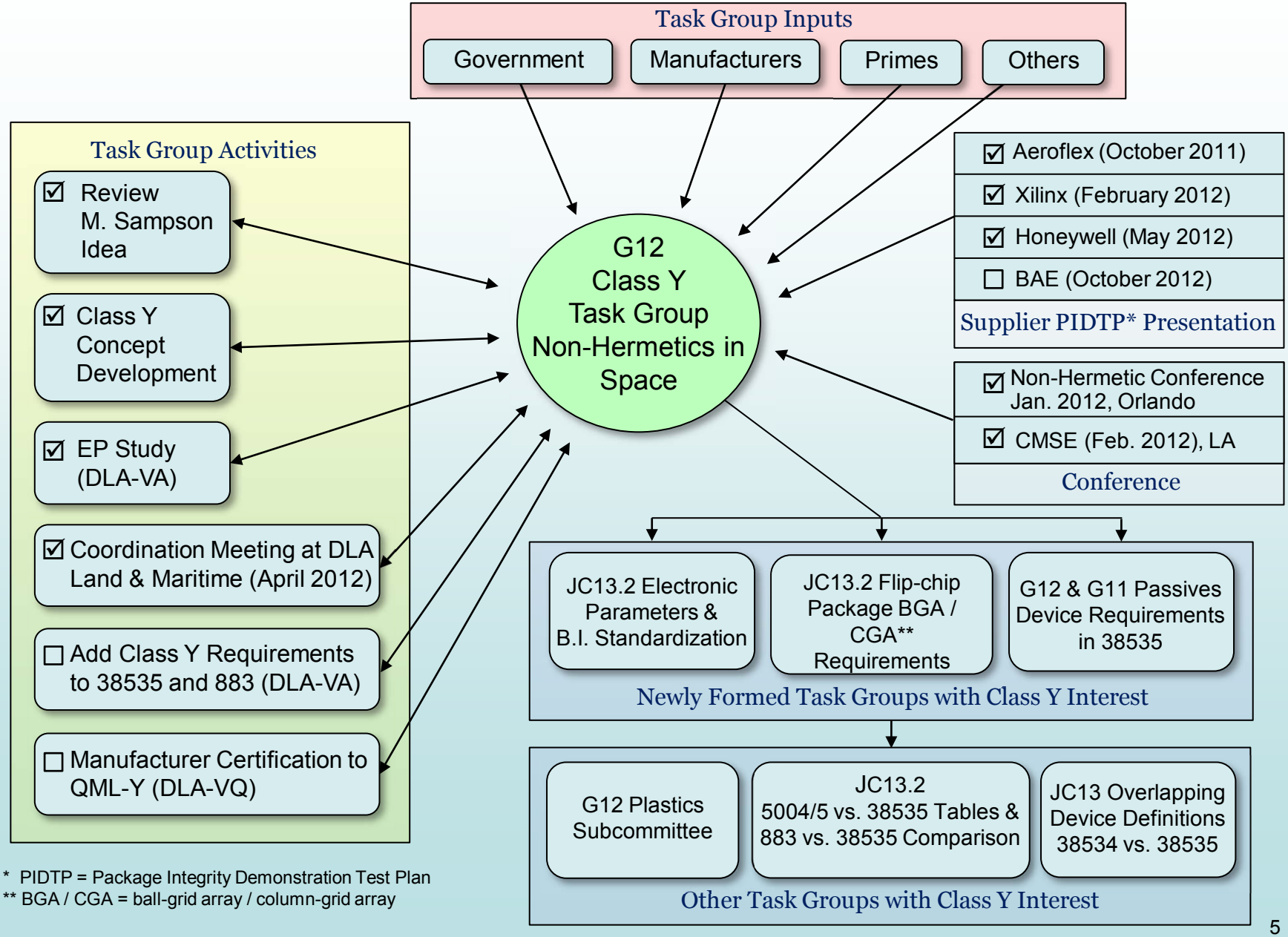
		Class V (Existing)	Class Y (In Development)	Comment
QML	Need class specific PIDTP	No	Yes	
CGA**	Offered as QML	Yes	Yes	
CGA*	CGA specific PIDTP	Yes	Yes	same for both classes
Flip-chip*	Flip-chip specific PIDTP	Yes	Yes	same for both classes
Passives*	38535 Para 3.15	applies	applies	same for both classes
Passives*	Any updates for BME	would apply	would apply	same for both classes

- **Observations**
  - * represents an issue which is common to both classes
  - ** highlights the fact that CGA devices are currently offered as QMLV.
  - Despite limited resources in working this task, a meaningful QML Y product must be delivered to the flight projects in a timely manner. While the common issues are being worked, we should be able to update MIL-PRF-38535 to include Class Y requirements. This would enable the manufacturers and DLA-VQ to gear up for Class Y audits, an activity that can start now and continue in parallel with resolution of common issues, thus saving time.

- **Recommendations**
  - DLA-VA to update 38535 with Class Y requirements and release it (keeping the requirements for common issues the same as they exist today for QMLV). DLA-VQ to begin auditing Class Y suppliers.
  - Keep working the common issues as quickly as possible. Continue to update the MIL documents as conclusions are reached on these issues.

PIDTP = Package Integrity Demonstration Test Plan
CGA = column-grid array BME = base metal electrode

Infusion of New Technology into the QML System
G12 Class Y Effort at a Glance



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

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Infusion of New Technology into the QML system Roadmap to QML-Y Flight Parts Procurement

- Major Milestones:
  - ☑ G12 approval of TG charter
  - ☑ G-12 Class Y Task Group to develop requirements
  - ☑ G12 approval for DLA-VA to commence EP study
  - ☑ DLA-VA to conduct EP study
  - ☑ DLA-VA to release “final” report
  - ☑ Coordination meeting at DLA Land and Maritime (April 2012)
  - ☐ DLA-VA to update 38535 and 883 with Class Y requirements
  - ☐ DLA-VQ to begin audit of suppliers to Class Y requirements

- After milestones completed,
  Users to procure QML-Y flight parts from certified/qualified suppliers

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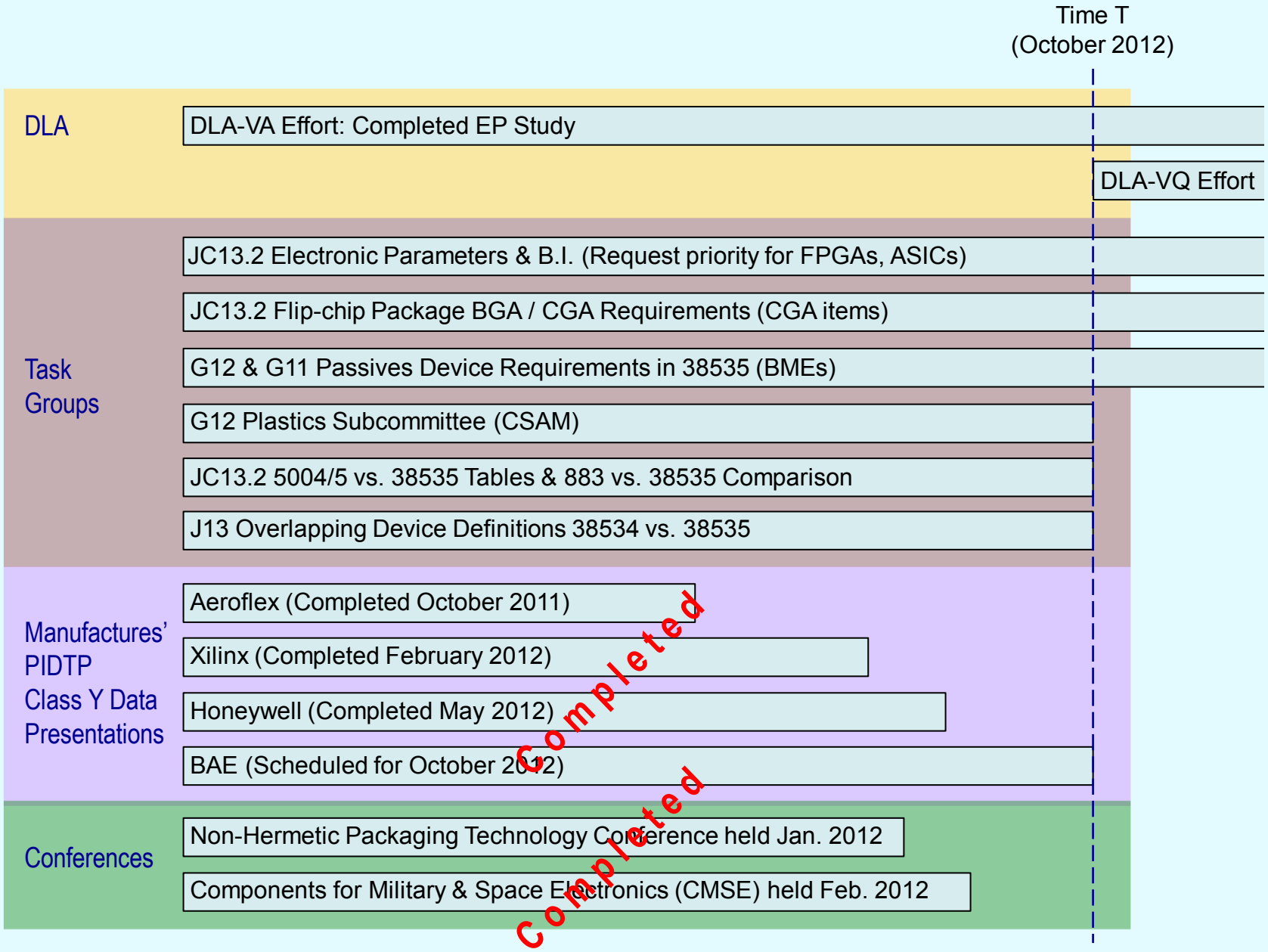
Closure of QML-Y (and related) Activities



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CLASS Y - Package Integrity Demonstration Test Plan (Class Y - PIDTP)
Data Sharing with the Space Community

- Presentations by Major Suppliers:
  - ☑ Aeroflex (Presented at the Class Y TG meeting in October 2011)
  - ☑ Xilinx (Presented at the TG meeting in February 2012)
  - ☑ Honeywell (Presented at the May 2012 TG meeting)
  - ☐ BAE (Scheduled for October 2012 TG meeting)
  - ☐ TBD

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The Team

The **Team members** are:

- Muhammad Akbar, DLA-VA
- Larry Harzstark, Aerospace
- David Sunderland, Boeing
- Shri Agarwal, NASA/JPL
- Roger Carlson, NASA/JPL

Team resources include:

- Mike Sampson, NASA/GSFC
- Mark Porter, G12
- Brent Rhoton, JC13
- Anduin Touw, G12
- Mike Adams, DLA-VQ
- Rob Heber, DLA-VA
- Tom Hess, DLA-VA
- Charles Saffle, DLA-VA

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Section Y

G12 Task Group 10-01
(Class Y)

Summary

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Current Status

DLA-VA completed EP study.

Background

Back in 2009, there was a big push to bring the Xilinx Viirtex-4 (a non-hermetic part) into the QML system as Class V device. NASA and others were not in favor as it would have created massive confusion. Mike Sampson conceived the idea of a new Class Y for non-hermetic space parts to provide QML coverage for Xilinx Virtex-4 and similar devices.

A new G-12 Task Group, TG 2010-01, was formed in early 2010 to address non-hermetic devices for space. Shri Agarwal was asked to lead the effort.

This task was challenging because it:

- Was far more involved than typical G12 tasks,
- Required development of a brand new concept,
- Used system-on-a-chip (SoC) — one of the most complicated devices,
- Needed to be simple and easily understood,
- Possessed sketchy testing and board assembly boundaries, and
- Was needed to procure a standard QML product as quickly as possible.

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Why “Class Y”?

- This effort is an attempt to bring advancements in packaging technology into the QML system.
- Advancements in packaging technology, increasing functional density and increasing operating frequency have resulted in single die SoCs with non-hermetic flip-chip construction, in high-pin-count ceramic column grid array packages
  - “Poster Child” example: Virtex-4 (V-4) FPGAs from Xilinx
  - Such products were evaluated for radiation and reliability and have drawn the attention of the space user community
- Question: How do we bring V-4 and similar microcircuits into the QML system as space products?
  - It can’t be Class V because those are hermetic devices
  - Our intent is to put V-4 like products for space users in a new category: “Class Y”.
  - In Jan 2010, G-12 opened a Task Group to develop Class Y
- What if we dropped the Class Y effort?
  - It would be a major loss for the space community and the QML program at large because the industry would be limited to ordering via Source Control Drawings (SCDs), which is counterproductive to Mission Assurance, prevents standardization, and is expensive.

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G12 Class Y Task Group Summary

- G12 Task Group formed in Jan. 2010 to develop screening/qualification requirements for non-hermetics for Space (TG2010-01).
- The TG's work so far may be summarized as follows:
  - Each of the meetings was well attended
  - As soon as the TG was formed, users were enthusiastic and eager to know when they could procure QML-Y flight parts. *See slide 8 on roadmap to procurement.*
  - A questionnaire was sent to a targeted group of users, manufacturers, and others (There are about 150 names on the Class Y distribution list). The major inputs were:
    - Class Y should cover those items that are ceramic flip-chip non-hermetic construction that passed the requirements of MIL-PRF-38535, Appendix B. The broader issue of organic-based substrates would be addressed in the next phase.
    - Some respondents asked why should space community even allow use of non-hermetic parts. (Although the feasibility of a hermetic ceramic package with under-fill flip-chip die has been demonstrated, there are concerns with sealing process, board level, etc. There are no current development programs as there is no user interest.)
    - Added the word "hermetic" to the definitions of QML-Q and QML-V classes in MIL-PRF-38535. (Done)
    - NASA does not endorse attaching the description "near hermetic" to Class Y. (How do you quantify "near-hermetic": it could be 10% or 99% hermetic, or less than half?). Both DLA-VA and DLA–VQ support the NASA position. (Status: The Non-hermetic Packaging Conference has changed the term "near hermetic" to "non-hermetic". NASA presented there.)

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G12 Class Y Task Group Summary (Contd.)

- TG meetings summary (cont'd):
  - Boeing proposed "simplified approach" was adopted:
    - Add paragraph to existing 38535 Appendix B stating differences for class Y (most remains same as Class V). One key element is for the manufacturers to submit a Package Integrity Demonstration Test Plan (PIDTP) to QA for approval. This plan must address issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, thermo-mechanical stresses, & shelf life. The PIDTP plan shall be approved by QA after consultation with the space community.
    - Separate issues related to non-hermeticity from those related to solder terminations (see below).
    - Provide markups to other affected documents.
  - 10 manufacturers so far have expressed interest in offering Class Y products (Xilinx, Actel, Intersil, Aeroflex, BAE, Honeywell, TI, e2v, 3D Plus, & Cypress).
  - Government customers and contractors have provided statements of support.
  - DLA Land and Maritime – VA (M. Akbar) was added to the team.
  - Comment from G12 management: The group may be surprised at how quickly this is moving. Usually, documents take longer than a year to get a full draft. You are far ahead of schedule. People just may not realize that Class Y is out of the conceptual stage and into the writing stage.

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G12 Class Y Task Group Summary (Contd.)

- Solder-terminated parts (could be hermetic or non-hermetic) need attention. Proposed a paragraph to add to MIL-PRF-38535, Appendix B. The JC-13.2 Task Group on solder terminations has been formed. The broad issues are: solderability, storage and shelf life, electrical testing, reworks, pull test, termination definition (tin–lead solder based?), etc. Some specific questions are:
  - What is the shelf life of the of the CGA? Specifically, how long will these parts be 100% solderable? Is this guaranteed?
  - As the columns would tend to oxidize when exposed to atmosphere, how do you store them: keep in sealed dry bags? Store in dry nitrogen?
  - Do all internal and external portions of the flip-chip package pass MIL-STD-883, Method 5011 (re. evaluation of polymeric materials)?
  - Once assembled, can the finished CGA (Like all other microcircuits, transistors, and hybrids) be functionally tested at –55ºC, 25ºC, and +125ºC? (If the solder melting point is estimated at about 180C, then it would be risky to electrically test the parts at 125ºC case temperature. Any cold brittle concerns at –55ºC?)
  - What board/assy level tests have been run for temp cycling/vibration, etc.?
  - What is the max number of allowable column reworks for space products?
  - Specify column pull test
  - Inspection of CGAs (area arrays, in general)
  - Need application notes on CGAs after column attach so that the users know what they are getting, any temperature limitations, adequacy of visual inspection, cleanliness, fluxes to avoid, etc.
  - Coordinate with IPC – what boundaries separate JEDEC work from IPC work?

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G12 Class Y Task Group Summary (Contd.)

- Clarification needed on burn-in, electricals, and delta requirements. This is a major issue for all microcircuits and would apply to Class Y products as well. For instance, statements such as, “The XXX FPGA has undergone 4000 hours of life test with parts biased in a static condition,” make one wonder why an FPGA (which is basically a digital part) was not subjected to a dynamic condition? There are other questions related to the activation energy, low temperature burn-in, etc. At the request of L. Harzstark and S. Agarwal, a JC13 Task Group has been formed to clarify/update requirements in MIL-STD-883, Method 5004.
- The screening/qual requirements for signal conditioning capacitors should be clearly stated (ref. MIL-PRF-38535, Paragraphs 3.15 and 3.15.1). What is the attached method of the BME capacitors used in many designs? During the G12, a couple companies said they use epoxy or silver–glass die attachment material to adhere the capacitor to the internal portion of the IC package. There are others who only use solder attachment. A JC13 Task Group has been formed to address these issues.
- What is a space flight part?
  - Land Grid Array, LGA, configuration (yes)
  - Column Grid Array, CGA, configuration (debatable)
- Will the set of 38535 classes, with Class Y added, cover microcircuits for the next several years? (yes, per the poll taken of major manufacturers)

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G12 Class Y Task Group Summary (Contd)

- The Team requested G12 approval for DLA - VA to conduct an Engineering Practice (EP) study using the detailed requirement input the Task Group has developed. This request was approved by G12.
- The Team's request for clear approval of the Task Group charter was also approved by G12. The charter statement reads:

  "This task group will develop requirements, including qualification and screening standards, for non-hermetic, ceramic-based microcircuits suitable for space applications. Initial effort will be focused on support for devices using flip-chip ceramic column grid array packaging, with resulting requirements to be submitted as a proposal for consideration to DLA Land and Maritime."
- So far 10 manufacturers have expressed interest in offering Class Y products (Xilinx, Actel, Intersil, Aeroflex, BAE, Honeywell, TI, e2v, 3D Plus, and Cypress).

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D. Sunderland Notes from Columbus Meeting

1. The extra time allotted for discussion in this forum was useful – 1 hour at JEDEC/TechAmerica meetings is too limited for this topic.
2. We walked through the entire EP Study report, achieving consensus on most comments that should allow an update soon after April 24 (when all comments are due).
3. Post-column electrical test remains a stumbling block. Proposed that either 1-temp post-column test or 3-temp LGA test following thermal simulation of column attach process be accepted. Also discussed sample post-column testing instead of 100% screen.
4. Various mechanical and radiation tests should have the option of being performed without balls or columns, as long as a failure mode due to balls or columns is not what is being tested.
5. All tables (screening, TCI and qualification) should have side-by-side columns for Class V and Y, differing in text and format only where hermeticity issues require it. Flip-chip and solder termination issues should apply to both columns.
6. Moisture resistance test: Consensus was that Class Y should see HAST instead of TM 1004 for V, but conditions (biased or unbiased) remain open.

D. Sunderland Notes (Contd)

7. We need a definition of PIDTP, clear indication of when one is needed, and list of what one should include. Consensus was that this should go into MIL-PRF-38535 Appendix H (Qualification), and a PIDTP would be required if any of the following technologies was used: a) non-hermetic package, b) flip-chip, or c) solder terminations. PIDTP requirements would be different for each case.

8. Use of ancillary passives not compliant with MIL-PRF-123 remains a stumbling block. Most believe that specific applications (such as power supply decoupling for low-voltage FPGAs) could be approved on the basis of: a) low stress, and b) low parametric sensitivity, and that language saying so might be useful. More generally, a lot-specific qualification program seems required, and Aerospace plans to convene a group to define what that will be. Suppliers seem resistant to creating a new military specification for BME capacitors. Limitation to only capacitors could be “at this time” to facilitate including other types in product roadmaps.

9. The exercise revealed a number of issues with MIL-PRF-38535 that have nothing to do with Class Y, flip-chip, or solder terminations. Recommendations to study the relevant passages should be made to relevant subcommittees or task groups.

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