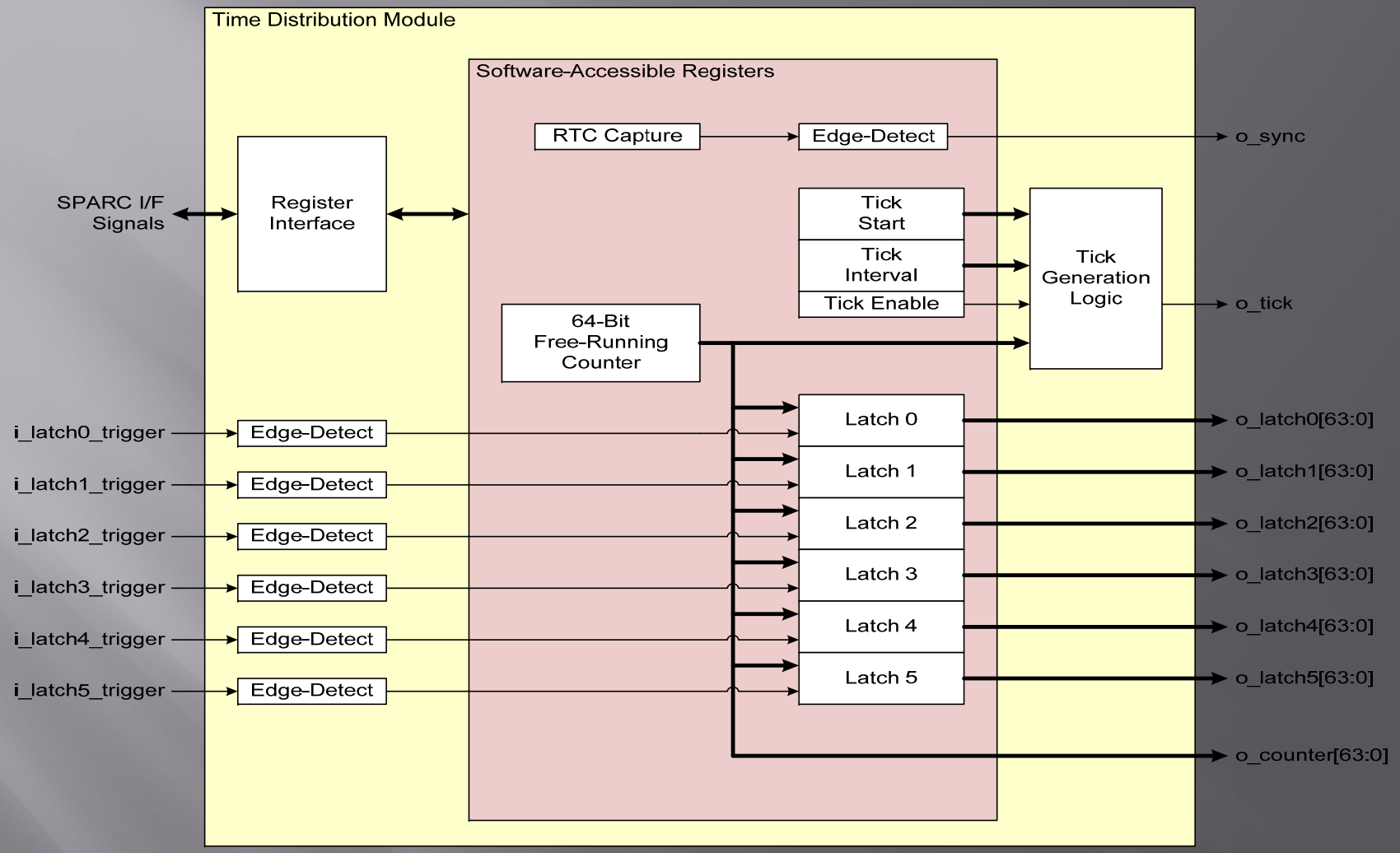
# CLOCK SYNCHRONIZATION

David Nguyen

# Goals of Experiment

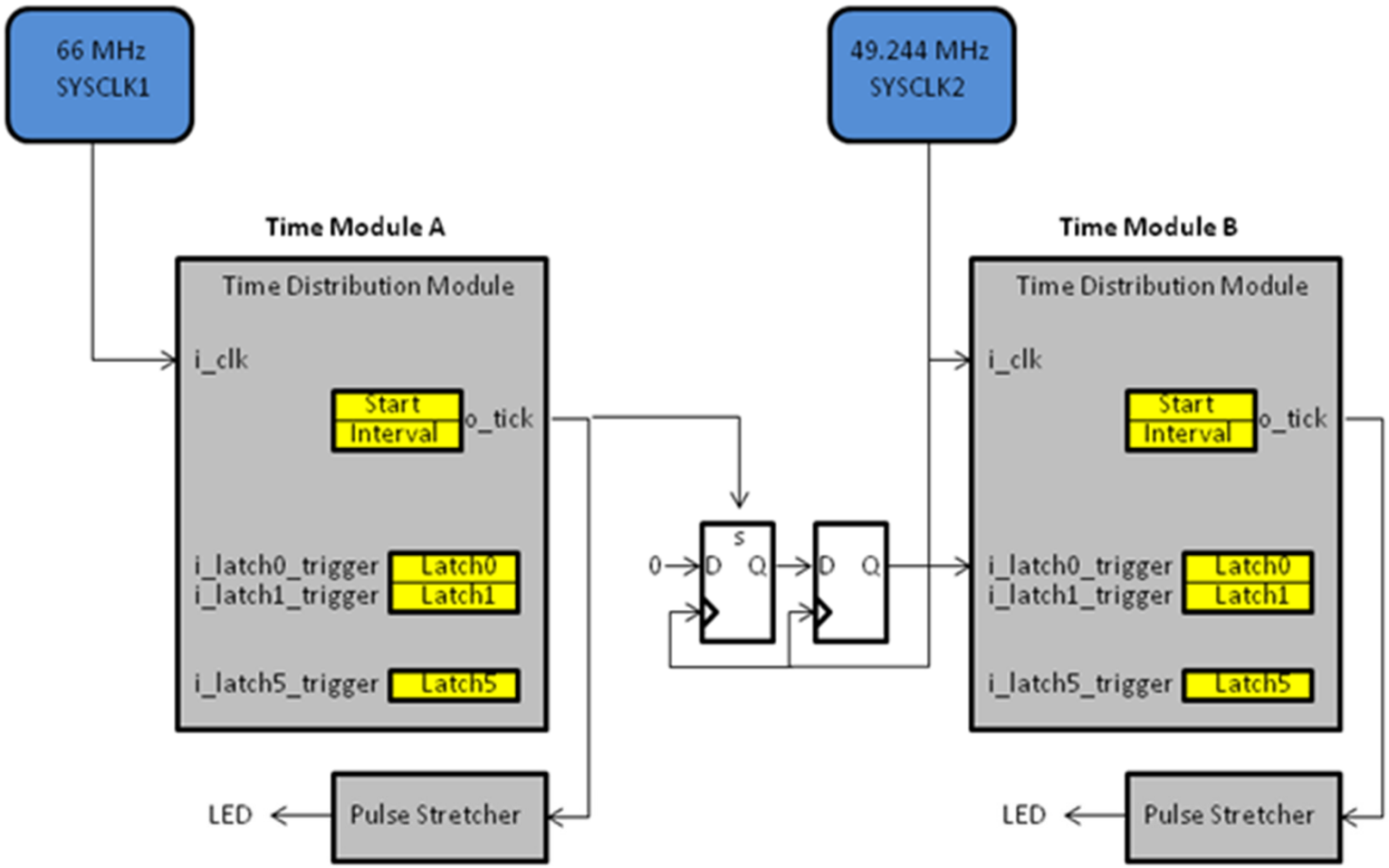
- Synchronize 1 pulse per second outputs derived from two different crystal oscillator sources
- Generate near atomic clock accuracy for other experimental needs

# Time Distribution Module Block Diagram



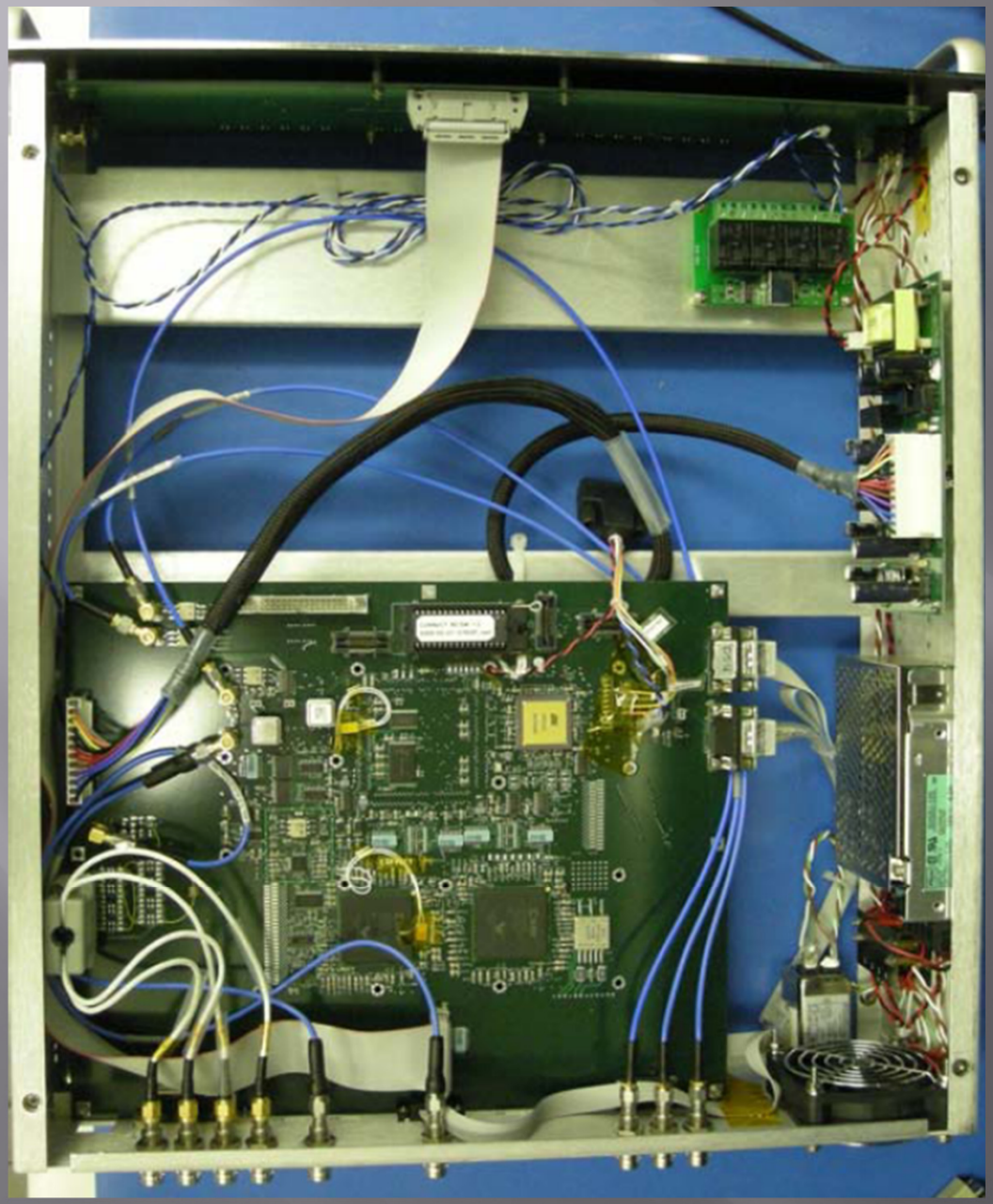

- Space Telecommunication Radio System OE for Software Defined Radio
- Verilog module
- Programmable pulse generator and counter/latch system

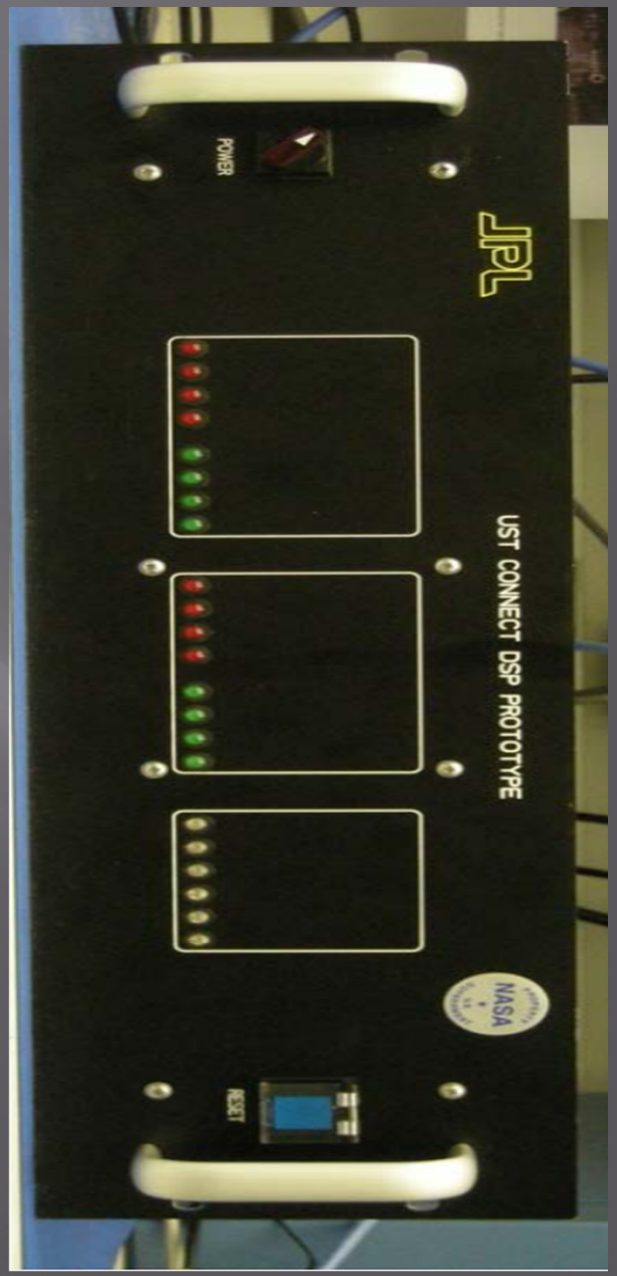
# Simplified Top Module



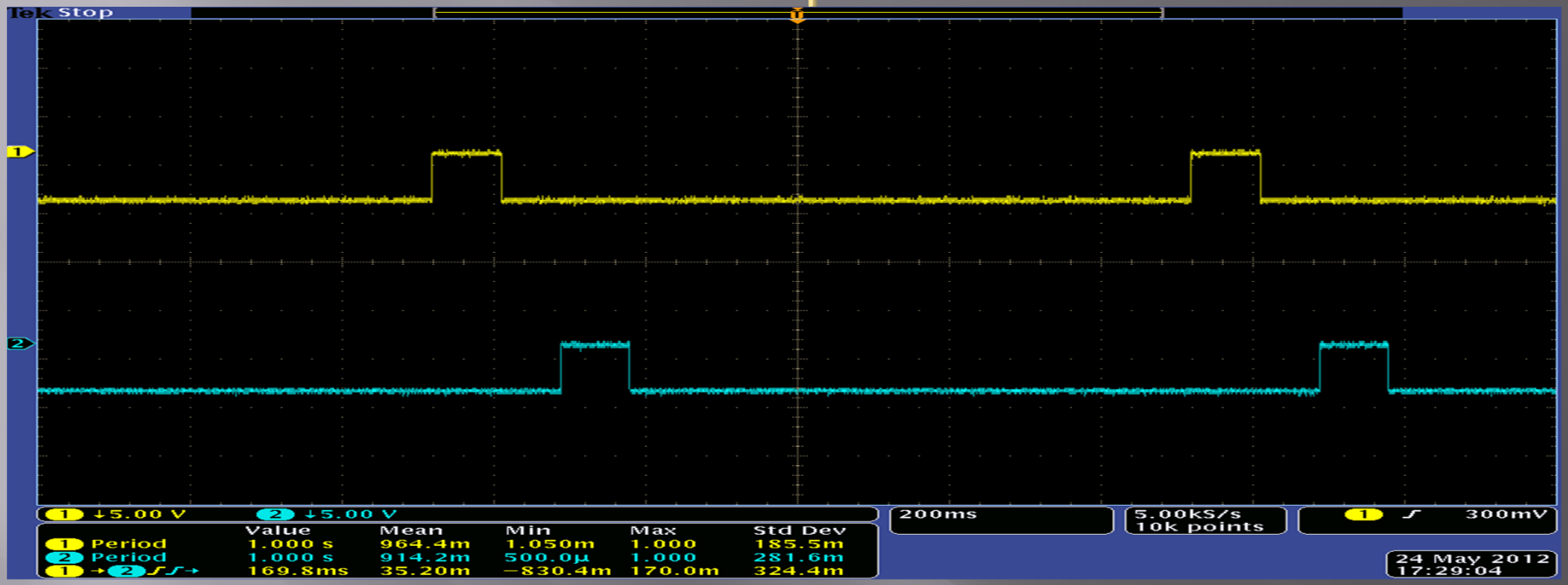

- Synplify Pro
- Xilinx (Impact)
- STRS Operating Environment <SHELL>

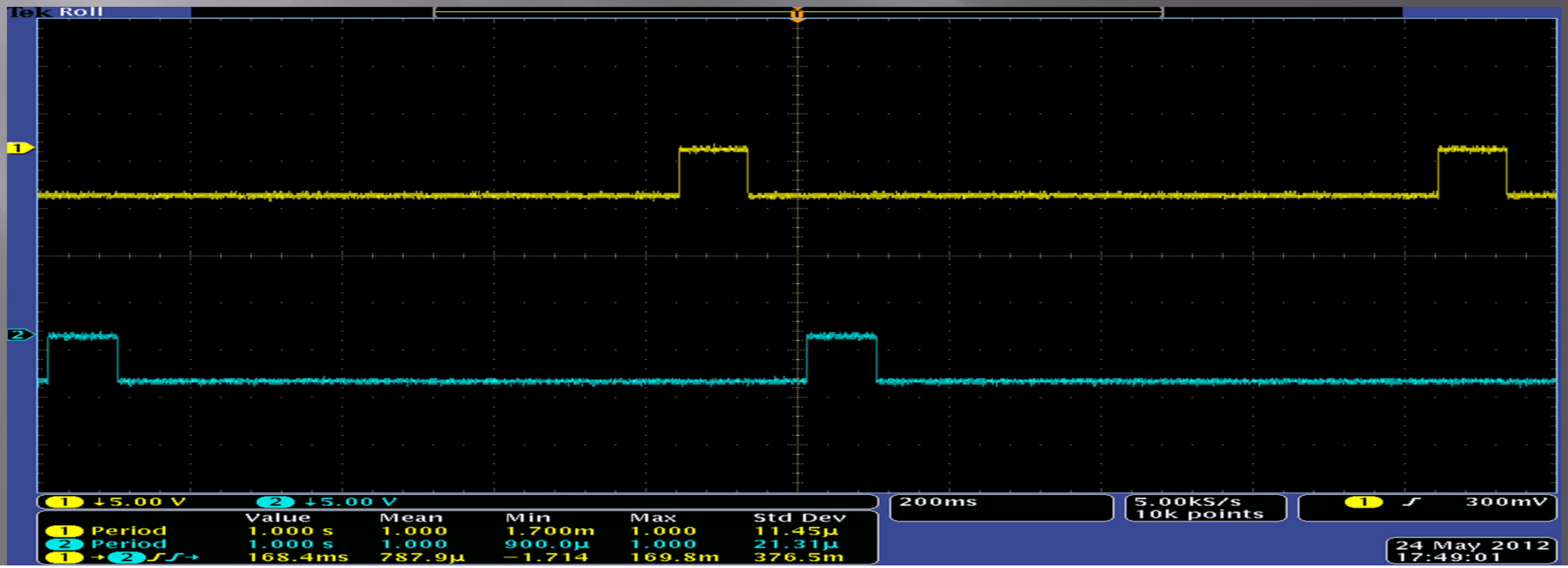
# Chassis



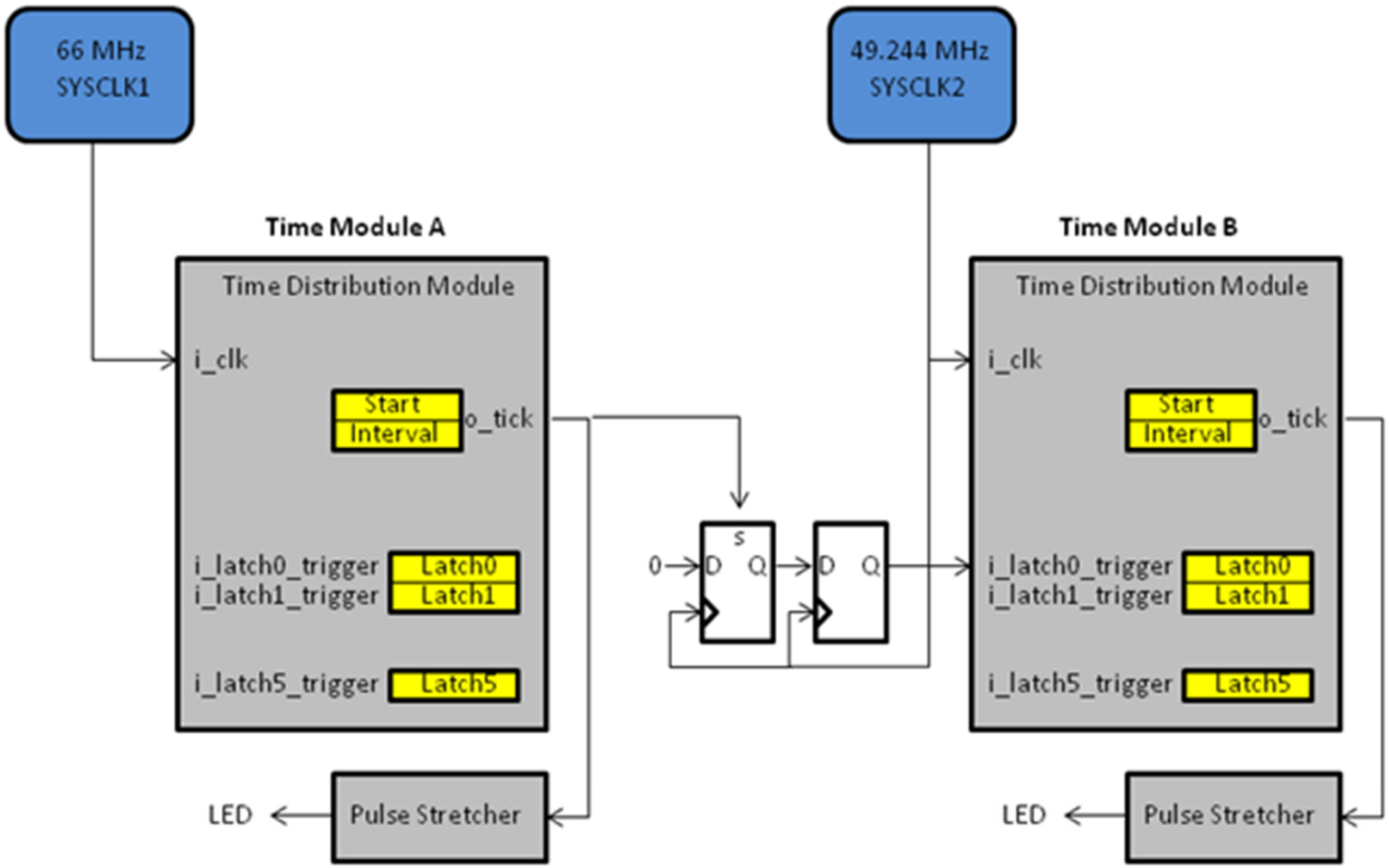


# Output


Tek Stop
1 ↓5.00 V
2 ↓5.00 V
200ms
5.00kS/s
10k points
1 300mV
Value Mean Min Max Std Dev
1 Period 1.000 s 964.4m 1.050m 1.000 185.5m
2 Period 1.000 s 914.2m 500.0µ 1.000 281.6m
1→2 169.8ms 35.20m −830.4m 170.0m 324.4m
24 May 2012
17:29:04


Tek Roll
1 ↓5.00 V
2 ↓5.00 V
200ms
5.00kS/s
10k points
1 300mV
Value Mean Min Max Std Dev
1 Period 1.000 s 1.000 1.700m 1.000 11.45µ
2 Period 1.000 s 1.000 900.0µ 1.000 21.31µ
1→2 168.4ms 787.9µ −1.714 169.8m 376.5m
24 May 2012
17:49:01

# Simplified Top Module

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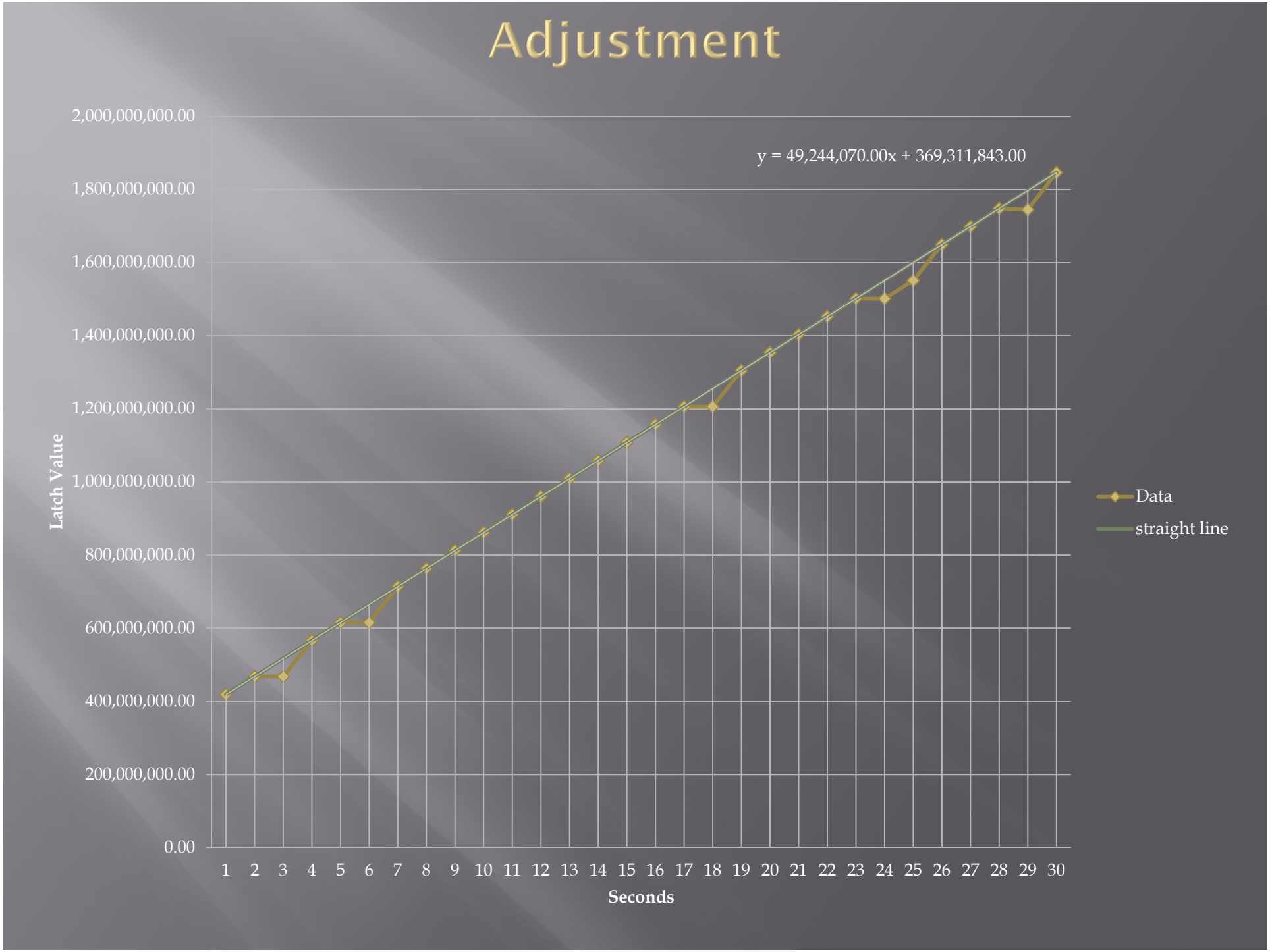
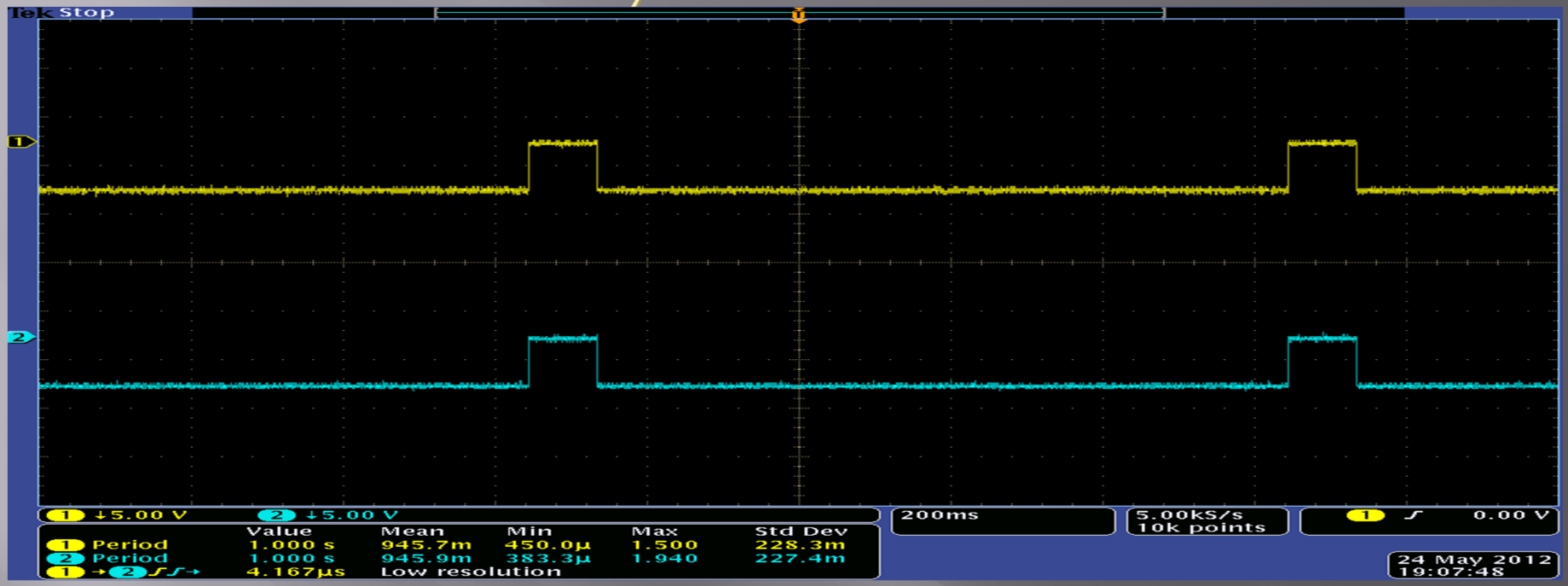
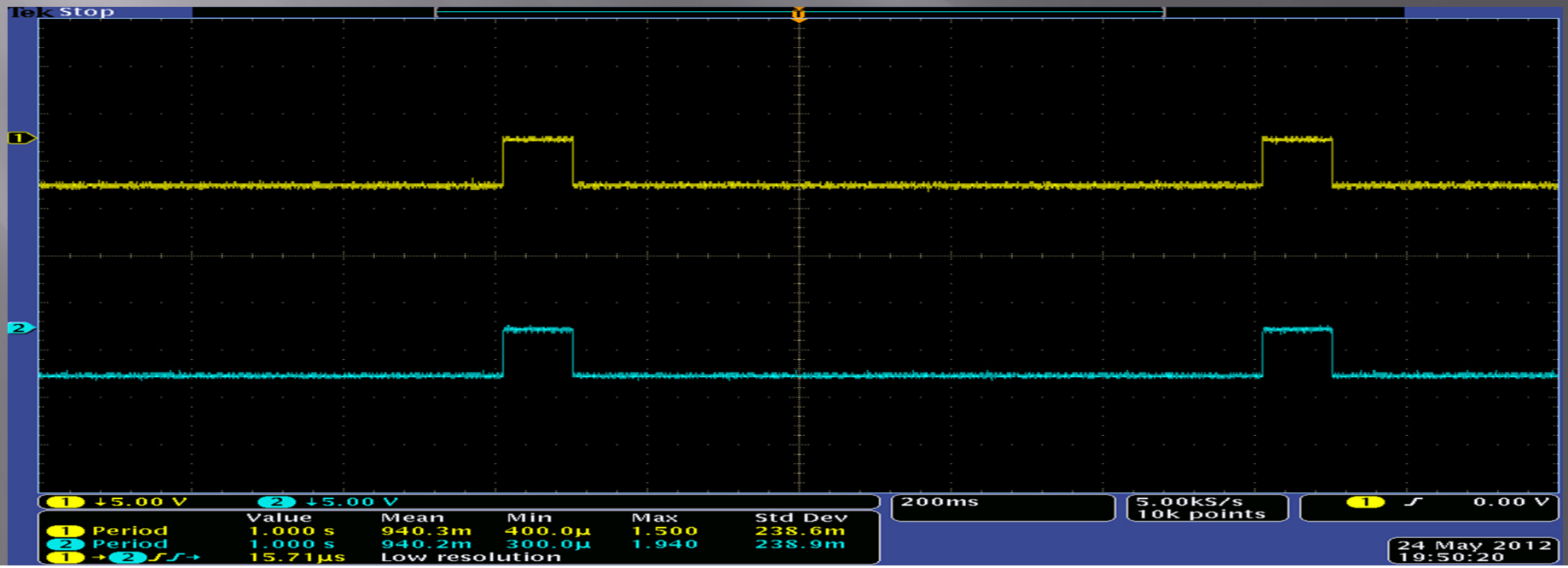

Adjustment
y = 49,244,070.00x + 369,311,843.00
2,000,000,000.00
1,800,000,000.00
1,600,000,000.00
1,400,000,000.00
1,200,000,000.00
1,000,000,000.00
800,000,000.00
600,000,000.00
400,000,000.00
200,000,000.00
0.00
Latch Value
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
Seconds
Data
straight line

# Synchronize



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