



# **Radiation Tests of Highly Scaled High Density Commercial Nonvolatile NAND Flash Memories Update 2009**

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## I. Introduction

In recent years, there has been increased interest in the possible use of high density commercial nonvolatile flash memories in space because of their high density capabilities and data retention. They are used in a wide variety of spacecraft subsystems. At one end of the spectrum, flash memories are used to store small amounts of mission critical data such as boot code or configuration files, and at the other end, they are used to construct multi-gigabyte data recorders that record mission and science data.

There are two types of basic floating gate flash memory structures: NOR and NAND configurations. In a NAND architecture, a large number of cells (typically 16 or 32) are connected in series, with a common drain connection to the bit line, and also a common source connection. In the alternative NOR architecture, there are many more source and drain connections, which allow faster access to individual cells. In flash memories, high internal voltages of 12 to 20 V are required for erase and write functions and charge pump circuits are provided internally to develop the high voltage from normal logic voltages.

Because of flash memories' complex structure, they cannot be treated as just simple memories. Thus, it becomes quite challenging to determine how they will respond in radiation environments. Flash memories have been the subject of several studies about ionizing radiation effects in recent years, regarding both total ionizing dose (TID) [1-3] and single event effects (SEE) [4-9] experiments. In both cases, the most radiation sensitive part of flash memories is the complex circuitry external to the floating gate (FG) cell array. However, the degradation of the threshold voltage,  $V_{TH}$ , of the single cell in the floating gate array after exposure to ionizing radiation is a non-negligible issue, as it may lead to the corruption of the stored code. Also, different functional failures have been detected in some commercial devices depending on the mode of operation during radiation exposure [5-6]. The functionality of flash memories begins to fail as TID accumulates during a space mission. In addition, direct strikes from galactic cosmic rays (GCR) and protons from a solar flare can upset internal circuitry associated with structures such as the charge pump, state buffers, cache, or internal microcontrollers. These upsets can result in incorrect read/write operation or even cause the device not to function until it is power cycled, reinitializing all the internal circuitry.

At present, the industry trend is to continue with feature size scaling. In advanced flash memories, one would expect the single event upset (SEU) cross section per bit to become smaller with shrinking feature sizes [2]. Also, decreasing feature size improves the possibility of an increase in the density. Furthermore, the SEU cross section for the FG arrays is becoming comparable to, if not larger, than that of the control logic. The SEU cross section can be dominated by either the FG array or the control logic, depending on the particular application [4]. Also, because of thinner oxide layers, total dose response improves [2]. However, because of the higher densities, the internal circuitry is more condensed and there is a higher chance of dynamic failure [6]. For highly scaled devices, the track structure of ions is comparable to the geometric size of critical regions within these highly scaled devices. If one or more energetic ions hit such a small critical region, the spatial average dose or charge liberation, averaged over the critical region volume, will be much larger than the spatial average would be for a larger critical region. Furthermore, a great deal of uncertainty exists in how the critical voltage condition for breakdown may be scaled with decreasing oxide thickness, and single event gate rupture (SEGR) may limit the scaling of advanced integrated circuits (ICs). In particular, this

phenomenon may be on the verge of becoming a serious problem as feature size scaling becomes comparable to ion track sizes [6].

High density commercial nonvolatile flash memories with the NAND architecture are now available from different manufacturers. This study examines SEE and TID in high density 8Gb single die NAND flash memory from Samsung and Micron Technology and reports on a new catastrophic SEE failure mode found in NAND flash memories. Both single level cell (SLC) and multi-level cell (MLC) devices were tested.

## II. Experimental Procedure

### II.A Device Descriptions

This study examines SEE effects in high density 8Gb single die NAND SLC flash memory from Samsung (K9F8G08U0M) and NAND SLC flash memory from Micron Technology (MT29F8G08AA). It also compares TID effects of Samsung 8Gb NAND SLC and MLC parts as well as Micron Technology SLC part. Table 1 summarizes the parts studied for this report.

**Table 1.** Summary of 8Gb NAND flash memories under study.

Device	Architecture	Part	Feature Size (nm)	Core Voltage (V)
Samsung	NAND (SLC)	K9F8G08U0M	51	3.3
Samsung	NAND (MLC)	K9G8G08U0A	63	3.3
Micron	NAND (SLC)	MT29F8G08AA	50	3.3

### II.B Test Facility and Procedure

#### II.B.1 SEE Measurements

Heavy ion SEE measurements were performed at three facilities—the Radiation Effects Facility located at the Cyclotron Institute Texas A&M University (TAM), the SEU Test Facility located at the Brookhaven National Laboratory (BNL), and the cyclotron facility at Jyväskylä, Finland (RADEF). The TAM and RADEF facilities use a cyclotron while BNL facility uses a twin Tandem Van De Graaff accelerator. All facilities provide a variety of ion beams over a range of energies for testing. Table 2 lists the ion beams used in the measurements for TAM facility, Table 3 for BNL facility, and Table 4 for RADEF facility. Linear Energy Transfer (LET) and range values are for normal incident ions. At TAM facility, tests used 15 MeV/amu ion beams. Beam fluence was  $1 \times 10^4$  to  $1 \times 10^7$  ions/cm<sup>2</sup>. At TAM and RADEF facilities, radiation testing was done in air with normal incident beam. Tests at BNL were done at vacuum with normal incident beam. The majority of high current spike data were taken at TAM facility. The BNL and RADEF facilities were used for SEU and single event functional interrupts (SEFI) characterization of the 8Gb Samsung and Micron Technology NAND flash memories.

**Table 2.** List of the ion beams used in the SEE measurements at TAM.

Ion	LET (MeV-cm <sup>2</sup> /mg)	Range (μm)
<sup>84</sup> Kr	27.8	134
<sup>109</sup> Ag	42.2	119
<sup>129</sup> Xe	51.5	120
<sup>141</sup> Pr	58.3	118
<sup>197</sup> Au	85.4	118

**Table 3.** List of the ion beams used in the SEE measurements at BNL.

Ion	LET (MeV-cm <sup>2</sup> /mg)	Range (μm)
<sup>19</sup> F	3.4	120
<sup>28</sup> Si	8.0	74
<sup>48</sup> Ti	19.8	40
<sup>9</sup> Br	37.3	36
<sup>107</sup> Ag	52.9	31
<sup>127</sup> I	59.7	31

**Table 4.** List of the ion beams used in the SEE measurements at RADEF.

Ion	LET (MeV-cm <sup>2</sup> /mg)	Range (μm)
<sup>20</sup> Ne	3.4	120
<sup>40</sup> Ar	8.0	74
<sup>56</sup> Fe	19.8	40
<sup>82</sup> Kr	37.3	36

### *II.B.2 TID Measurements*

Total ionizing dose (TID) measurements were taken using the JPL Cobalt-60 facility at a dose rate of 50 rads (SiO<sub>2</sub>) per second at room temperature. Also, total dose measurements were performed using a 20 keV x-ray source at the Air Force Research Laboratory (AFRL), with a dose rate of 100 rads (SiO<sub>2</sub>) per second. In all measurements, the devices under tests (DUTs) were under static bias during irradiation, but not actively exercised, because this corresponds to the actual operating condition during most of an extended space mission. The TID measurements were performed in the following two modes:

- 1. Refresh Mode (Erase/Program/Read)**
  - a. Erase, write, and read to validate sequential numbers.
  - b. Irradiate with static biased DUTs.
  - c. Read random numbers to ensure data retention.
  - d. Repeat steps **a** to **c** for each radiation increment.
  
- 2. No Refresh Mode (Read Only)**
  - a. Erase, write, and read to validate sequential numbers.
  - b. Irradiate with static biased DUTs.
  - c. Read random numbers to ensure data retention.
  - d. Repeat steps **b** to **c** for each radiation increment.

## **II.C Test Setup**

The DUTs were etched to remove the plastic packaging and expose the memory array to the ion beam. SEE and TID data were taken using a commercial memory tester called JDI. The JDI tester is capable of performing high-speed testing on memory systems. The JDI system and DUT were powered separately by an HP6629 power supply. This setup allowed for rapid detection and protection from single event latchup (SEL) events.

All the SEE tests were conducted by first loading the DUT with a random pattern and then verifying the pattern by reading it back from the device. During irradiation, the DUT was read continuously and checked for errors and logged. After irradiation, the pattern was again verified and the device's power was cycled; the pattern was erased to make the device ready for the next run.

The TID delivered to the DUT by the ion beam was monitored during the heavy ion test. When the dose reached levels where the device performance was degraded, the DUT was switched to a virgin device so as not to invalidate the fidelity of the SEE test results.

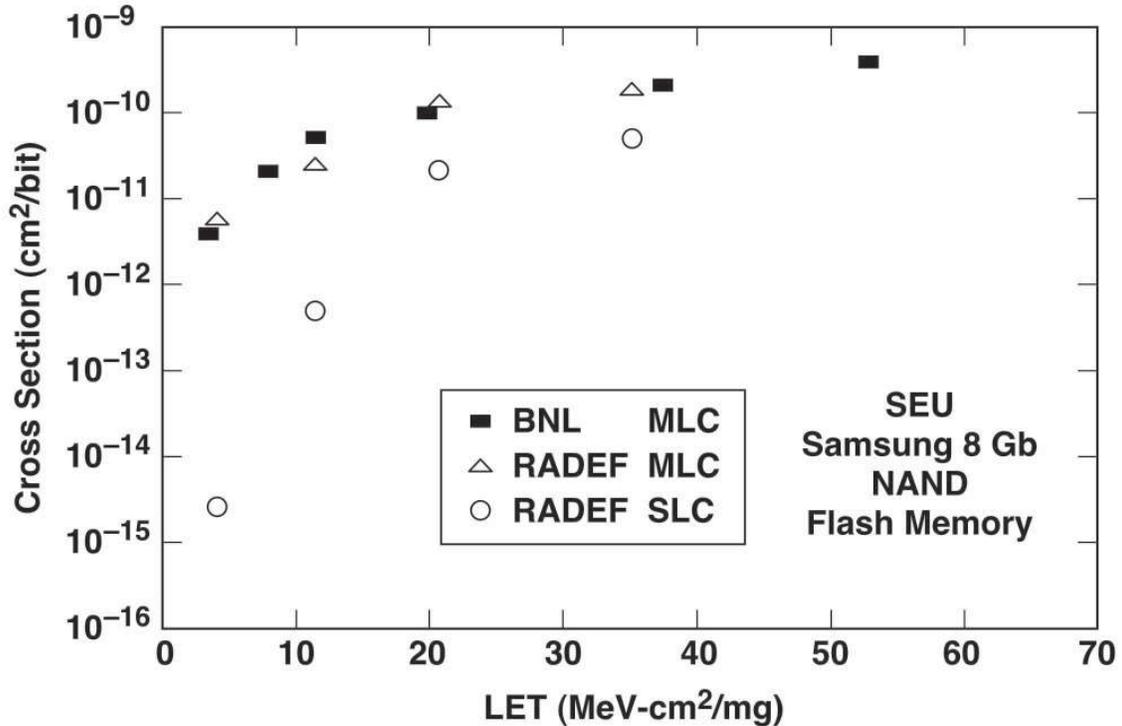
In TID measurements the DUTs were programmed all in zeros and Co-60 irradiations were performed. Also, x-ray irradiations were performed only on de-lidded Samsung MLC devices. TID measurements with Co-60 and x-ray were performed in both No Refresh mode and Refresh mode.

## **III. SEE Test Results**

Three types of radiation-induced events were observed during measurements: SEU, SEFI, and high current spikes, which in some cases caused catastrophic device failure that manifested itself as a loss in ability to erase and write to the DUT.

### **III.A SEUs**

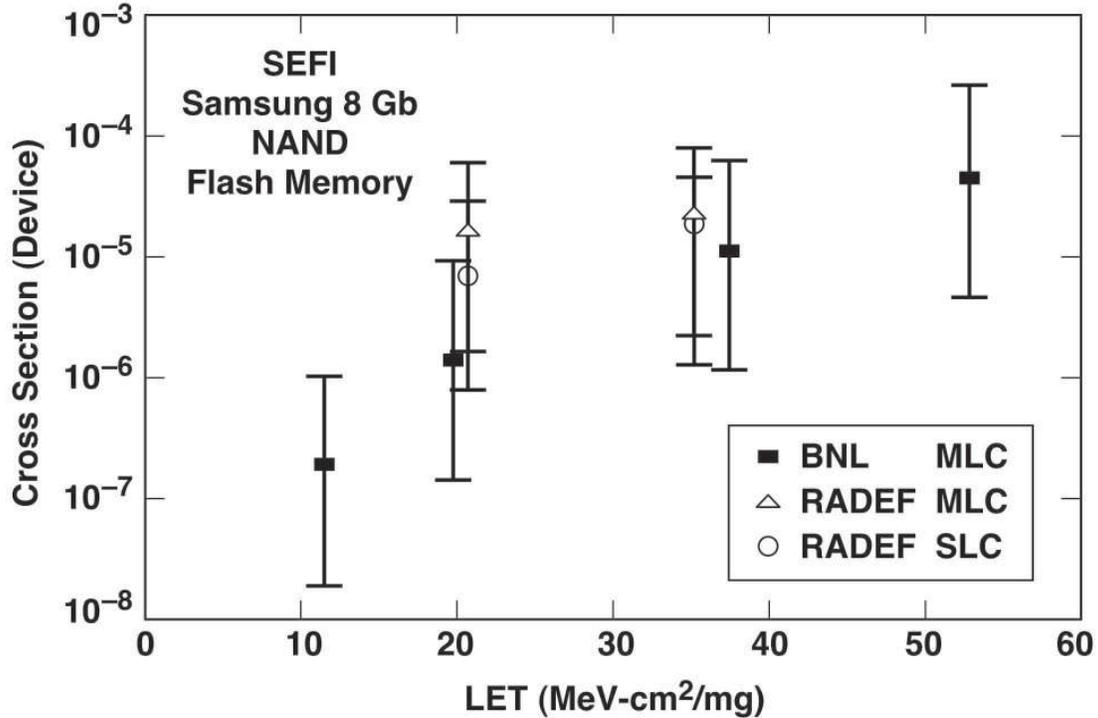
SEUs were observed for all DUTs; however, the commercial high density devices appear to be much less susceptible to SEUs than typical flash devices tested recently [1,7–9]. Figure 1 compares the SEU cross sections for the Samsung 8Gb MLC and SLC NAND flash memory. The error bars are  $\sim 2$  sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols. For comparison, this report displays results of measurements for MLC devices at both BNL and RADEF facilities. The two measurements show excellent agreement. It is not surprising that the SLC devices are less sensitive to SEUs than MLC devices. This can be attributed to the fact that the voltage threshold  $V_{TH}$  changes are smaller in a MLC device. The SEU cross section per bit for MLC and SLC devices at large LET are on the order of  $5 \times 10^{-10}$  and  $5 \times 10^{-11}$  cm<sup>2</sup>/bit, respectively. The GCR rate in interplanetary space during solar min condition for MLC devices is approximately  $1.0 \times 10^{-9}$  events per bit per year (worst case). The rate from solar flare is approximately  $2.0 \times 10^{-6}$  per bit per flare (worst case) [10]. These low upset rates can be easily handled by the most rudimentary error detection and correction systems.



**Figure 1.** SEU cross section for Samsung 8Gb MLC and SLC NAND flash memories. Measurements were performed at BNL and RADEF.

### III.B SEFIs

Figure 2 shows the SEFI cross section for Samsung 8Gb MLC and SLC NAND flash memory. The error bars are  $\sim 2$  sigma and result from Poisson statistics. For comparison, this report displays results measurements for MLC devices at both BNL and RADEF facilities. The agreement is within the statistical error bars. The SEFI LET threshold is below 12 MeV-cm<sup>2</sup>/mg for the MLC parts. The GCR rate in interplanetary space during solar min condition for MLC devices is approximately  $2.0 \times 10^{-4}$  events per device per year (worst case). The rate from solar flare is approximately 0.35 per device per flare (worst case) [10]. It is unclear how much beam was delivered to the device before the SEFI occurred, thereby complicating the analysis of SEFIs. In addition, the signature, recovery mechanism, and consequence to the device operation varied greatly, depending upon exactly how the device functionality was altered. Typical SEFI events resulted in a large number of errors while trying to read the device. We defined the SEFI cross section as the number of times the device would experience SEFI divided by the total fluence to which the device had been exposed, including runs with no observed SEFI. This was done for each LET. Some events will self-recover once the device is re-read; other SEFIs require a power cycle and the part to be re-initialized to return to normal operations.

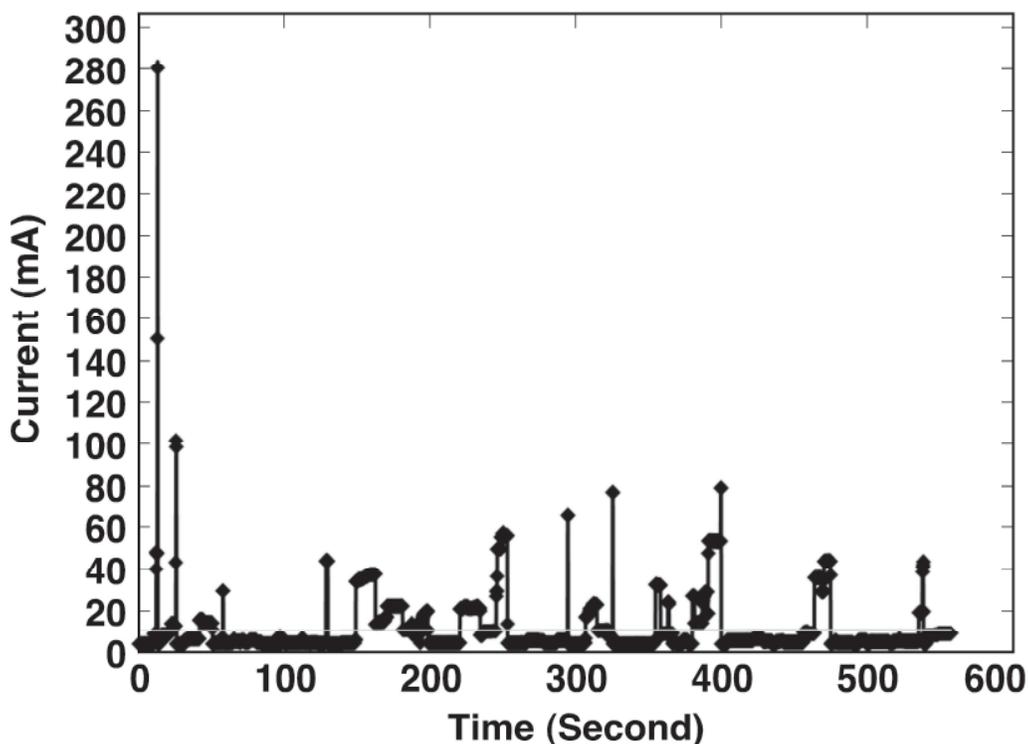


**Figure 2.** SEFI cross section for Samsung 8Gb MLC and SLC NAND flash memories. Measurements were performed at BNL and RADEF.

### III.C High Current Phenomenon

The most surprising and troublesome observation in the measurements was the occurrence of relatively high current spikes during high LET testing of high density NAND flashes. This phenomenon was destructive (the loss of ability to erase and write to the device) for all the NAND flashes under study except for the Micron Technology 8Gb flashes. This phenomenon even happened when the DUT was a virgin device and the dose delivered in that run was relatively low—approximately a couple of krads (SiO<sub>2</sub>)—confirming that the phenomena is not a consequence of accumulated TID, but due to single ions striking a sensitive area of the device. Subsequently, the effect was permanent and devices did not recover even after a high temperature anneal (some devices were still nonfunctional after being kept at 150°C for two hours).

Figure 3 shows typical current spectra versus time for 8Gb Samsung NAND flash memories in static mode at LET 85 MeV-cm<sup>2</sup>/mg, after 10<sup>7</sup> <sup>197</sup>Au ions per cm<sup>2</sup>. The operating current for this device is approximately 0.3 mA (the maximum operating current for these devices is 3 mA), but during irradiation, the current spikes were as high as 280 mA. The high current spike should not be mistaken with a typical latchup event, because a latchup is defined to be a self-sustaining state. Although radiation causes the current to spike, it cannot stay in high current mode, and the measurements show that they last for approximately 400 ms or less. In TAM and BNL studies, the high currents started at an LET around 27 MeV-cm<sup>2</sup>/mg; however, high current spikes lead to a catastrophic failure (loss of ability to erase and write to the device) at higher LET around 40 MeV-cm<sup>2</sup>/mg for 8Gb Samsung NAND flash memories. Even though the spikes themselves are transient, they produce permanent damage.



**Figure 3.** Current spectrum for 8Gb Samsung NAND flash. Data were taken with  $^{197}\text{Au}$  ion at LET  $85.4 \text{ MeV}\cdot\text{cm}^2/\text{mg}$  at TAM.

The high current spike phenomenon was observed even in static mode under bias at TAM. However, no damage occurred when parts were irradiated without bias. We masked the charge pump region and internal circuitry with a thick material during exposure in order to investigate if the charge pump or the internal circuitry was the source of the high current spikes. The material was thick enough to attenuate the beam. At TAM, BNL, and RADEF, no high current spikes were observed, indicating that the high current spikes were caused by energetic ions hitting one or both of these regions. In another shielding arrangement, the FG array was masked and the charge pump region exposed. High current spikes were observed.

This means that the charge pump does play a crucial role in this phenomenon, even if it is not the sole origin. This is typically the first structure to also fail in TID testing. In this case, a single or a few particles deposit enough energy local to the volume associated with the charge pump to produce degradation. Figure 4 shows a thermal image of a damaged device with power on, with damage in the charge pump region.

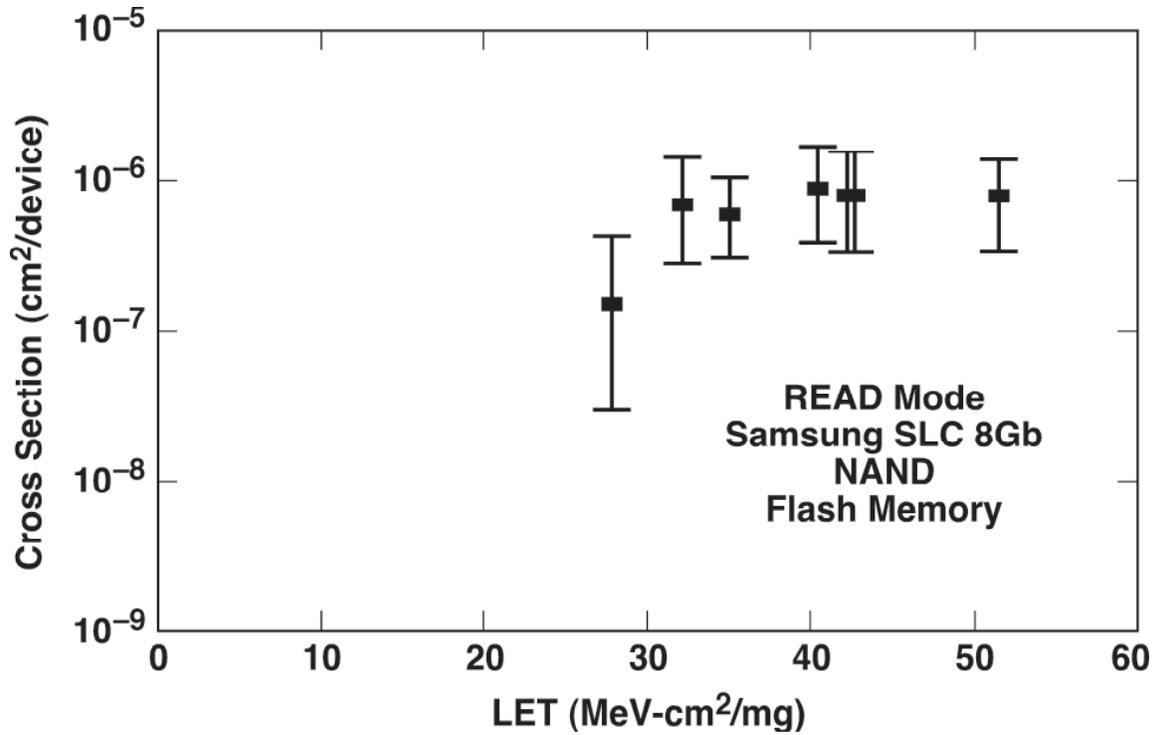


**Figure 4.** Thermal picture of the charge pump region of the 8Gb SLC Samsung flash memory. The damaged area is clearly visible.

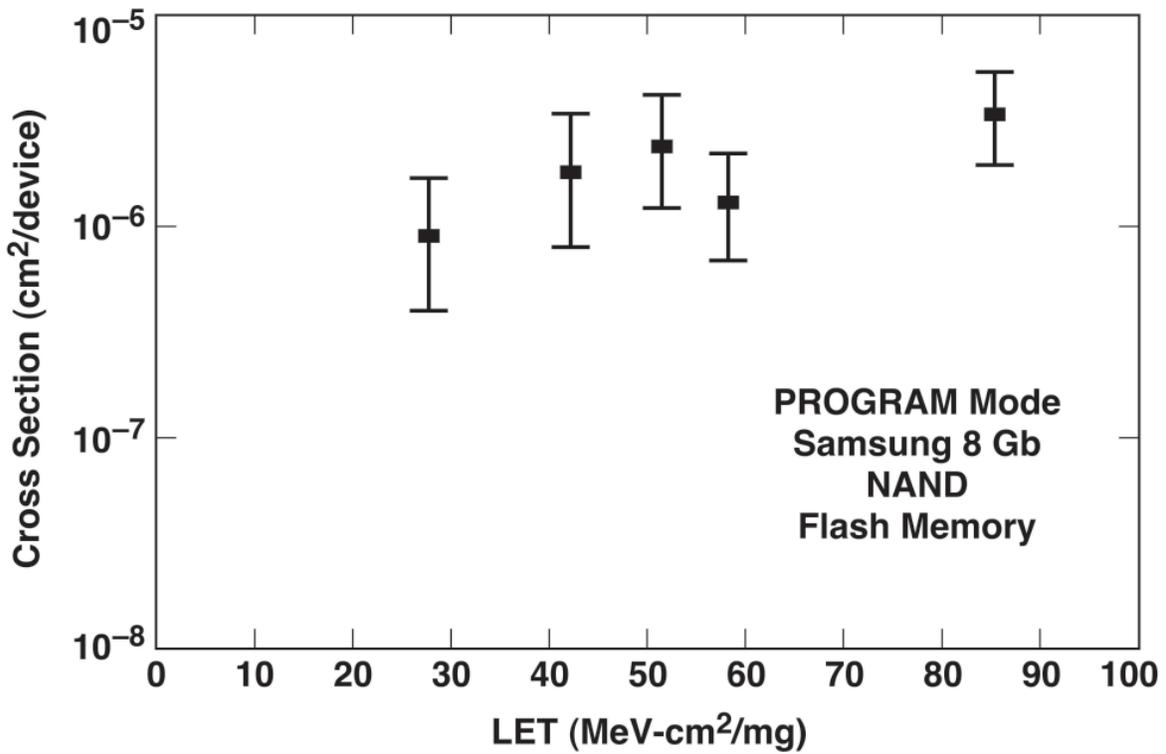
In order to investigate this phenomenon, we developed an ad hoc setup at TAM. The beam was stopped within 100 ms as soon as the supply current exceeded 20 mA and power was cycled on the DUT. This allowed isolation of individual current spikes during damage assessments. At TAM, catastrophic failure happened typically after the first spike.

At TAM, we performed measurements in two different modes: READ and PROGRAM mode. Figures 5 and 6 display the cross section data for high current spike for 8Gb Samsung NAND flash in READ and PROGRAM mode, respectively. The high current spike phenomenon was destructive for all the Samsung NAND flash memories (SLC and MLC) in READ and PROGRAM mode. The LET threshold is below  $27 \text{ MeV cm}^2/\text{mg}$ . The cross section is higher in PROGRAM mode. The high current spikes were not destructive for Micron Technology NAND flash memories in READ mode, although the limited measurements for Micron Technology 8Gb SLC NAND flash memory in PROGRAM mode at LET  $77.3 \text{ MeV-cm}^2/\text{mg}$  resulted in destructive high current spikes. We have not studied high current phenomena for any other Micron Technology NAND flash memories except the limited measurements of 8Gb SLC NAND flash memory.

For Micron technology SLC NAND flash memory, we performed the measurements in an extreme environment to test the destructiveness of the high current spikes in READ mode. A test was performed on the Micron Technology NAND flashes at LET  $85.4 \text{ MeV-cm}^2/\text{mg}$  at elevated temperature of  $80^\circ\text{C}$  and the supply voltage was increased to 3.6 V. After irradiating the part with  $5 \times 10^7 \text{ }^{197}\text{Au}$  ions per  $\text{cm}^2$ , although the device was functional, half of the blocks were not writable or erasable. The bad blocks recovered gradually after annealing. All blocks were writable or erasable after 48 hours.



**Figure 5.** Cross section for high current spikes for the 8Gb SLC Samsung NAND flash in READ mode. Measurements were performed at TAM.



**Figure 6.** Cross section for high current spikes for the 8Gb SLC Samsung NAND flash in PROGRAM mode. Measurements were performed at TAM.

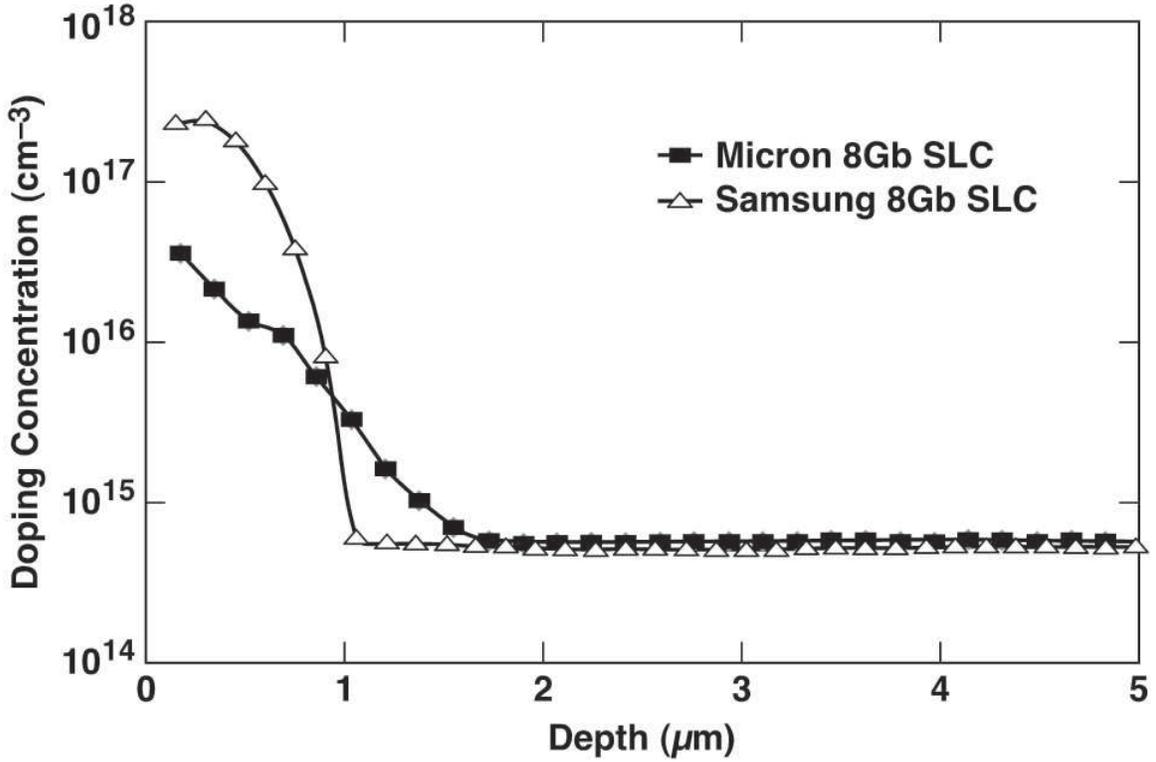
Table 5 shows the threshold for high current events in READ mode for all the NAND flash memories studied in this work and previous work [6]. The table also shows the feature size of the device and doping level of the n-well transistors used in the charge pump circuitry for each device. The doping concentration levels were measured by performing spreading resistance analysis (SRA). Data did not show any clear difference between SLC and MLC parts, perhaps they use the same charge pump.

It is interesting to note that the doping concentration level for Samsung and Hynix parts, which showed destructive high currents [6], is higher compared to Micron Technology parts and ST Micro 8Gb part. Figure 7 compares the doping level concentration for Samsung 8Gb SLC NAND flash memory with Micron Technology 8Gb SLC NAND flash memory. The lower doping concentration level of Micron Technology NAND flash memories results in wider depletion regions and consequently a higher critical voltage condition for breakdown [8]. This might suggest that the destructiveness of high current phenomena for Samsung and Hynix flash memories in READ and PROGRAM is the direct result of low breakdown voltage resulting from high doping level concentration. In the new generation of NAND flash memories, the charge pump generates 19–20 V to perform program and erase. The lower doping concentration of the Micron Technology and ST Micro 8Gb might not be low enough to prevent the destructiveness of the high current spikes in PROGRAM mode.

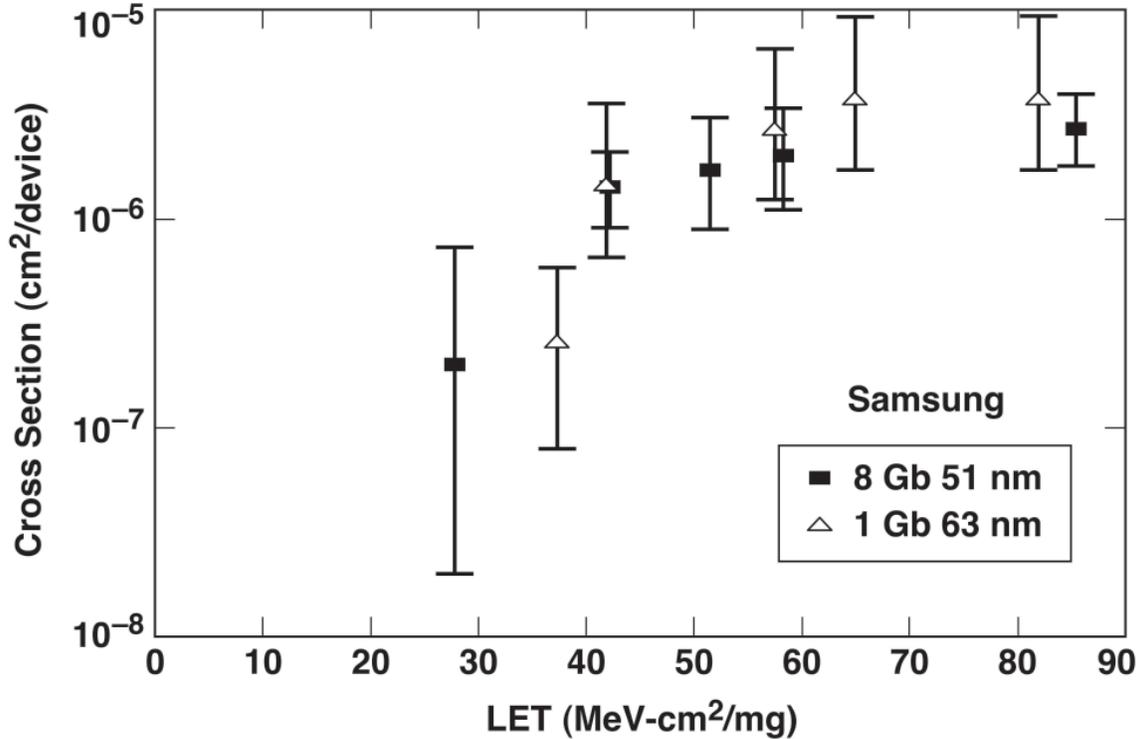
The Samsung 1 Gb NAND flash memory is built on 63 nm processes (feature size) while the Samsung 8Gb is built on 51 nm processes. Figure 8 compares the high current cross section in READ mode for Samsung 1 and 8Gb NAND flash memories. The LET threshold for current spikes is lower for the part with smaller feature size (51 nm, 8Gb), while the high-LET cross section is the same. Furthermore, Table 5 shows that the LET threshold for high current spikes gets smaller with smaller feature size. This might indicate that as the feature size scaling continues, the nature of the destructive high current phenomenon and its effects might become significant and alarming.

**Table 5.** Summary of LET threshold for high current phenomena for parts studied in READ mode.

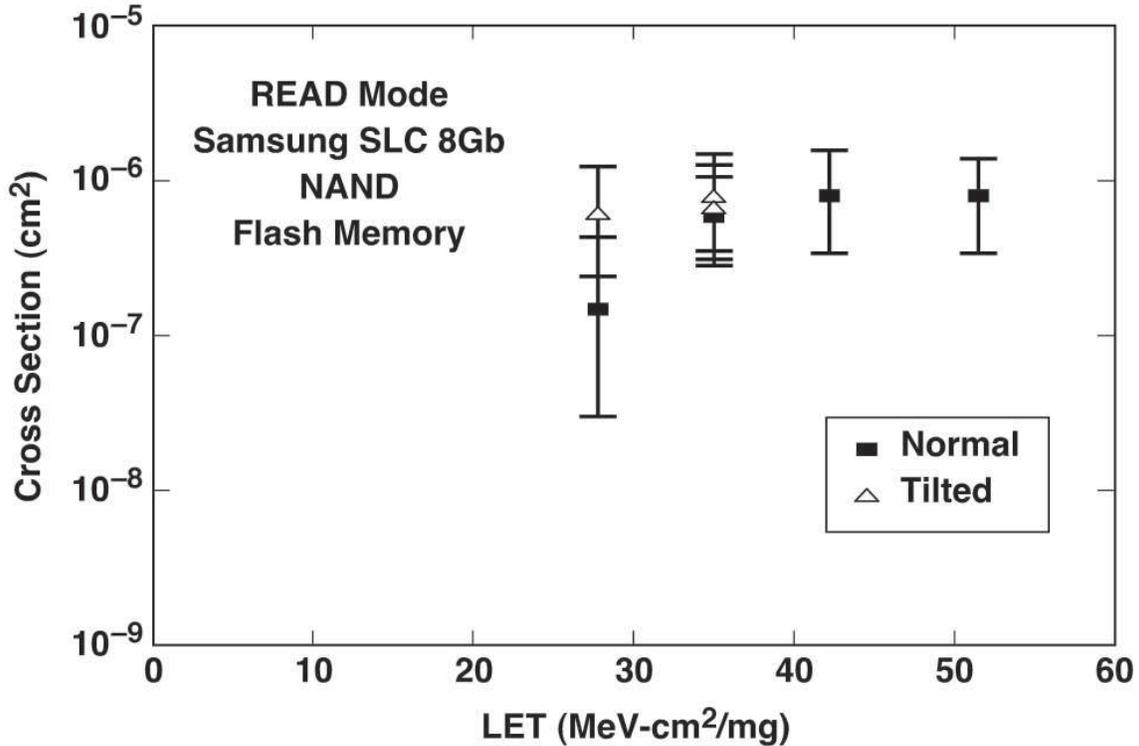
Device	Part	Feature Size (nm)	Doping $\text{cm}^{-3}$	LET Threshold (MeV-cm <sup>2</sup> /mg)	Mode
Micron 2Gb	MT29F2G08AA	90	-	LET <sub>th</sub> < 55	Non destructive
Micron 4Gb	MT29F4G08AA	72	$7.7 \times 10^{15}$	LET <sub>th</sub> < 55	Non destructive
Micron 8Gb	MT29F8G08AA	50	$3.6 \times 10^{16}$	LET <sub>th</sub> < 27	Non destructive
ST Micro 8Gb	NAND08G-BXC	63	$5.1 \times 10^{16}$	LET <sub>th</sub> < 37	Non destructive
Hynix 4Gb	HY27UF084G2M	90	$2.7 \times 10^{17}$	LET <sub>th</sub> < 55	Destructive
Samsung 1Gb	K9F1G08U0M	63	$9.8 \times 10^{16}$	LET <sub>th</sub> < 37	Destructive
Samsung 2Gb	K9F2G08U0M	63	-	LET <sub>th</sub> < 37	Destructive
Samsung 4Gb	K9F4G08U0A	63	$1.1 \times 10^{17}$	LET <sub>th</sub> < 37	Destructive
Samsung 8Gb	K9F8G08U0M	51	$2.3 \times 10^{17}$	LET <sub>th</sub> < 27	Destructive



**Figure 7.** Comparison of doping concentration level of Samsung 8Gb and Micron Technology SLC NAND flash memories.



**Figure 8.** Comparison of the high current spike cross section for the 1 and 8Gb Samsung NAND flash in READ mode.



**Figure 9.** Comparison of the high current spike cross section in READ mode for normal and tilted beam.

We also performed some limited measurements to study the angular dependence of this phenomenon. Figure 9 compares high current spike cross section in READ mode for Samsung 8Gb SLC flash memory for normal and tilted beams. The cross section in this plot is the count number divided by fluence when fluence is measured in a plane perpendicular to the beam, instead of the device plane. The LET is actual LET instead of effective LET. This plotting format places all points on a common curve when device susceptibility is isotropic. In contrast, the more traditional plotting format (with fluence measured in device plane, and LET being effective LET, which is actual LET divided by the cosine of the tilt angle) places all points on a common curve when device susceptibility satisfies the cosine law. The plot in Figure 9 shows better conformity to a common curve than the more traditional plotting format, suggesting that device susceptibility might be nearly isotropic. However, it should be noted that our limited angular measurements only covered small angles, 30°. It is possible that at larger tilts, the effect shows some angular dependence. Future studies will investigate angular dependence at a larger angle.

#### IV. TID Test Results

We performed TID measurements in two modes, Refresh mode (Erase/Program/Read) and No Refresh mode (Read only). The measurements were performed on Samsung 8Gb MLC and SLC parts as well as on Micron Technology 8Gb SLC parts. The sample size for these measurements was three.

##### IV.A Refresh Mode (Erase/Program/Read)

The first TID measurements were performed on Samsung and Micron Technology parts with Co-60 in Refresh mode. The DUTs were programmed all in zeros. The Samsung 8Gb SLC failed to

erase after 250 krad ( $\text{SiO}_2$ ), compared to the Micron Technology 8Gb SLC after 35 krad ( $\text{SiO}_2$ ). The Samsung 8Gb MLC still can be erased after 600 krad ( $\text{SiO}_2$ ).

#### IV.B No Refresh Mode (Read only)

In the second TID measurements, the DUTs were programmed all in zeros and Co-60 irradiations were performed in No Refresh mode. Also, x-ray irradiations were performed only on three de-lidded MLC devices up to 350 krad ( $\text{SiO}_2$ ) in No Refresh mode.

Figure 10 shows the buildup of read errors during TID exposure of the DUTs programmed to all zeros prior to irradiation. These errors are caused when the  $V_{\text{TH}}$  of a programmed (zero) floating gate changes enough to shift from the programmed to the erased cell (one) distribution, and being read as an erased cell in READ mode. As a result, the first cells to flip are those programmed at the lowest  $V_{\text{TH}}$ . While variations in  $V_{\text{TH}}$  occur below TID threshold, they may be too small to be detectable in READ mode [11]. For Samsung 8Gb MLC devices with all cells programmed in the zero state, the error number increases monotonically and saturates around 100 krad ( $\text{SiO}_2$ ) to half of the number of bits. After 100 krad ( $\text{SiO}_2$ ), almost half of the bits are read as a one. The charge pump was verified to be functional up to the level of 600 krad ( $\text{SiO}_2$ ) to which the DUTs were irradiated. For Samsung 8Gb SLC devices, the error number is negligible up to 200 krad ( $\text{SiO}_2$ ) and increases monotonically and saturates around 500 krad ( $\text{SiO}_2$ ) to all of the number of bits exposed to radiation; in addition, the charge pump is still functional. For Micron Technology 8Gb SLC devices, the error number is negligible up to 100 krad ( $\text{SiO}_2$ ) and increases monotonically to 250 krad ( $\text{SiO}_2$ ). The charge pump is not functional after 250 krad ( $\text{SiO}_2$ ).

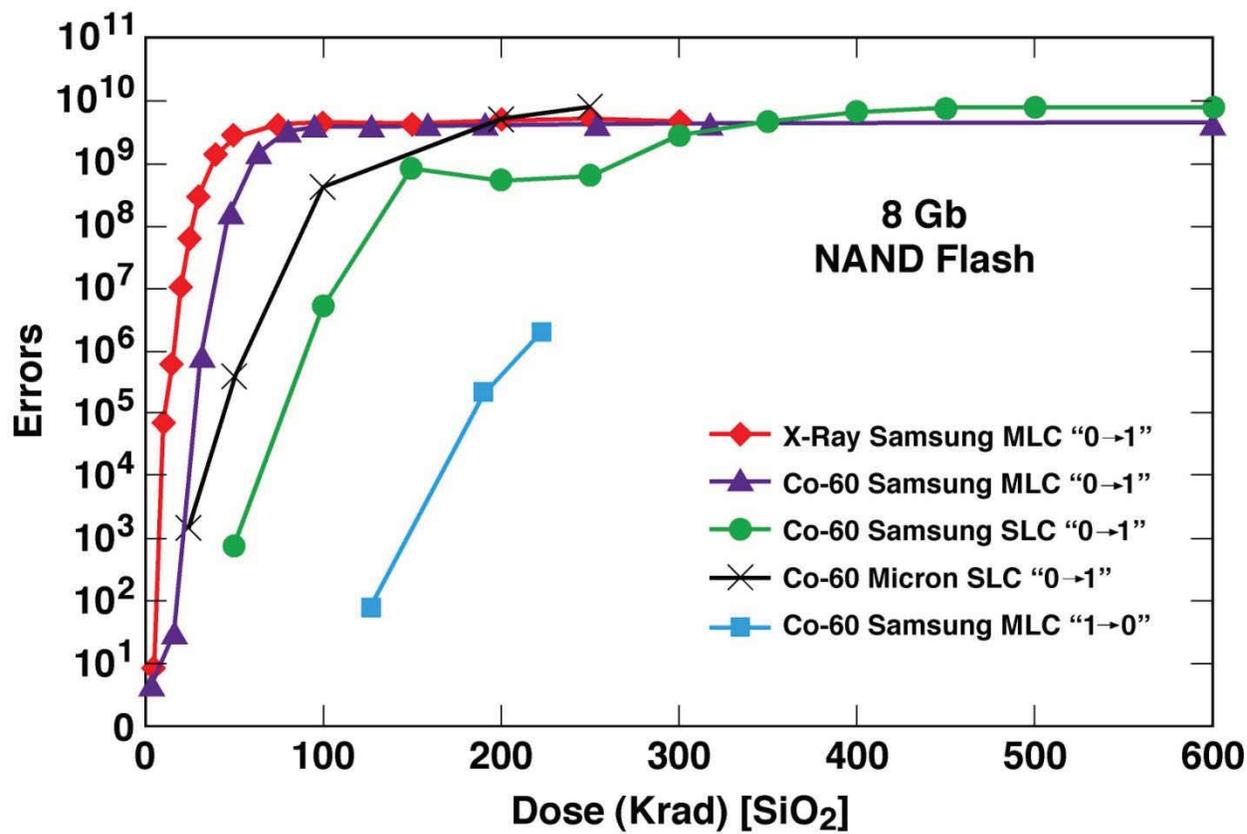
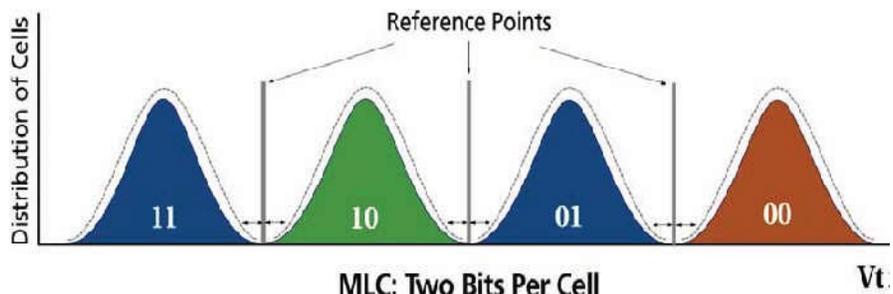


Figure 10. Comparison of TID measurements of MLC and SLC devices with Co-60 and x-ray.

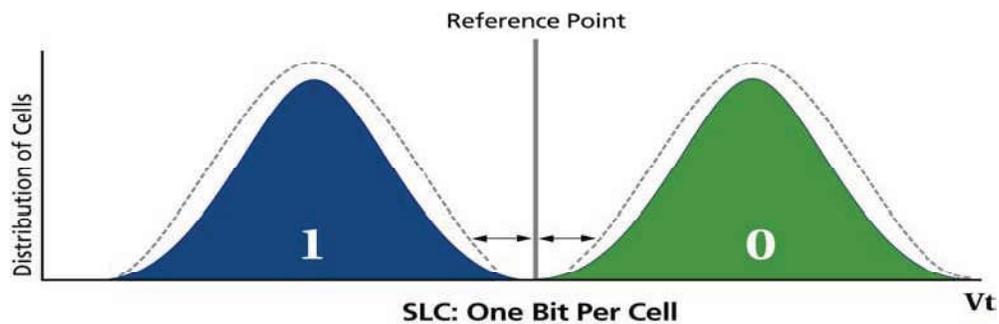
Also, the Samsung 8Gb MLCs that have been programmed to all ones prior to irradiation did not show errors in an excessive way. There were a few errors attributed to errors from circuitry and buffer regions and not from cells.

The Samsung MLC part shows more sensitivity to x-ray irradiation than Co-60. It has been shown that floating gates are more sensitive to x-ray than to  $\gamma$ -rays (Co-60 irradiation), likely due to dose enhancement effects [12]. In the case of Co-60 irradiation, we observed read errors starting around 50 krad (SiO<sub>2</sub>). For x-ray irradiation, the threshold was around 10 krad (SiO<sub>2</sub>).

Figures 11 and 12 compare threshold voltage distribution and illustrate the comparative differences between MLC and SLC NAND flash cells, respectively. SLC NAND stores two binary states (either a binary 1 or a binary 0) in a single cell, whereas MLC NAND can store four states: 00, 01, 10, and 11. To recognize the four states (11, 10, 01, and 00), special circuitry must be added to allow the amount of charge stored in the floating gate to be controlled within narrow limits during the writing, and also to detect the different amounts of charge during reading. The programming circuits must deliver precise amounts of electrons to the floating gate, and the sense amps must distinguish between the four small threshold voltage regimes. There is considerably more design margin with SLC, which leads to greater radiation robustness, reliability, and endurance compared to MLC. Before irradiation, the  $V_{TH}$  distribution almost resembles the expected Gaussian shape. However, after irradiation, the threshold voltage of all floating gates programmed in the zero state uniformly moves toward lower  $V_{TH}$ . On the other hand, the threshold voltage of all floating gates programmed in the one state uniformly moves toward higher  $V_{TH}$  [13].



**Figure 11.** Multi-level flash cells. The x-axis represents cell threshold voltage.



**Figure 12.** Single-level flash cells. The x-axis represents cell threshold voltage.

Not surprisingly, Figure 10 shows that at saturation only about half of the bits are read as a one for Samsung MLC devices. This might be contributed to a reduction in the voltage generated from the dedicated read charge pump circuitry. If the voltage generated by the read charge pump is lower than the designed value, all the cells belonging to the same string of 32 floating gates will be read as zero regardless of their actual status.

## V. Discussion

Interpretation of radiation tests in the new generation of flash memories is difficult because of the very involved architecture and internal circuitry. Heavy ion tests in earlier studies found no fundamental cell upsets; however, apparent upsets in the most complicated devices were attributed to buffer and register upsets [1,5,6]. The radiation tests in the present study were more limited in scope and concentrated on determining whether the same general types of functional errors occurred in newer high density flash memories as well as investigating the possibility of destructive failures. SEU in the newer high density devices appears to be similar to that in the older technology. The SEU LET threshold of commercial high density flash memories has changed very little with scaling. However, the saturation cross-section per device per bit has steadily decreased with smaller feature size. Functional failures caused by cell upset in the very complex control and state registers used in flash memory architecture continue to occur. It is likely that page/block SEFI type of errors arise due to upsets in configuration registers in the memory array rather than upsets of the individual bits.

The results presented above for the high current spikes and destructive behavior observed in this study is not adequate to clearly identify the exact cause and mechanism of the phenomenon. Taking into account an increasing oxide breakdown field with decreasing oxide thickness, advanced technologies should become less susceptible to SEGR at a given electric field as gate oxide thickness decreases [14], if voltages are scaled to produce the same electric field. There is, however, a great deal of uncertainty in how the voltage may be scaled with decreasing oxide thickness. Furthermore, work by Johnston [15] raised the concern that SEGR may limit the scaling of advanced ICs. In the last few years, pioneering work has uncovered a variety of new radiation-induced effects in thin gate oxides, including radiation-induced leakage current in gamma and electron irradiated oxides [16], SEGR [15], and radiation soft breakdown (RSB) [14,17–18] in oxides exposed to high LET heavy ion irradiation. However, very few advanced ICs with thin oxides have been subjected to gate rupture experiments, and most of the conclusions about scaling are based on experiments with capacitors. Although capacitors provide insight into some aspects of the phenomena, they can not necessarily be extended directly to circuits because of the difference in geometry and doping levels [14]. The dielectric gate ruptures (SEDR) due to heavy ions have only recently been observed in high density digital circuits that have ultra thin oxides (less than 7 nm). Permanent damage attributed to catastrophic gate breakdown from heavy ions was first reported in [19] for 4 Mb dynamic random access memory (DRAMs). Recently, SEGR was reported in linear devices [20]. It was concluded that SEGR thresholds depend strongly on ion energy but are independent of oxide defects, bias polarity, doping concentration, and ionizing dose.

Considering these effects, SEGR or SEDR cannot be excluded. The oxides in the charge pump circuitry are typically thin enough to experience damage from a single event strike. The charge pump is biased even during the READ operation, but at a reduced voltage from the write/erase

operation. Latent damage has been seen to recover, or exhibit a reduction in leakage current, after irradiation in several cases [14–18]. This is especially true for charge pumps with the read voltage applied as the electric field may not be sufficient to induce complete oxide failure, but initial leakage current will be significant. It is noted, however, that the charge collection mechanism a charge pump would experience might not be typical of SEGR, but the initial damage mechanism in the charge pump oxide would be similar.

This high current phenomenon might be attributed to the doping level in the NAND flash memory. It has been shown that the critical voltage condition for breakdown is somewhat lower for higher doping concentrations than for low doping [15]. The SRA measurements indicate that the Samsung and Hynix NAND flash memories might have a higher doping level and, consequently, a lower critical voltage condition.

The observed phenomenon in advanced flash memories might be indicative of standard flash memory response coming in future generations. This is likely a result of the scaling down of feature size, oxide thickness, possible higher electric fields and the number of electrons trapped on the FG. As flash cell sizes are decreased, the nature of this phenomenon and its effects might become significant.

## **VI. Conclusion**

We tested the advanced commercial high density NAND flash memories from Samsung, Hynix, ST Micro, and Micron Technology with heavy ions. The general conclusion is that the SEU per bit and SEFI cross sections in this study are smaller than the older generation of flash memories. We also investigated the TID response of 8Gb Samsung and Micron Technology NAND flash memories with x-ray and  $\gamma$ -ray irradiation. There is an improvement in the charge pump TID response compared to the older generation of flash memories. Our TID results showed that the threshold voltage shift in irradiated devices depends on the radiation source. Dose enhancement phenomena were observed after x-ray irradiation.

Another observation is a new high current phenomenon in the high density NAND flash memories. This high current phenomenon is destructive for all parts under study except the Micron Technology and ST Micro 8Gb NAND flash memories during READ mode. Our limited measurements for Micron Technology and ST Micro 8Gb NAND flash memories during PROGRAM mode at high LETs resulted in destructive high currents.

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