National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/OSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

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A Look at Failure: Junction Failure

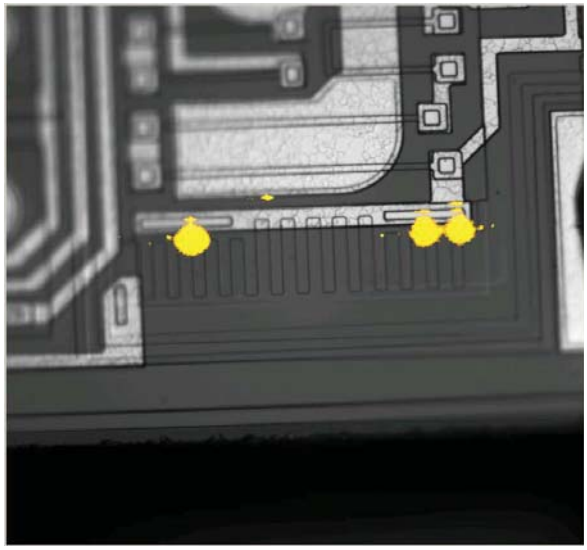

Photo Emission Microscope reveals junction failures. JPL's Failure Analysis Lab.

GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Counterfeit	**F8-A-10-03** Unauthorized Distribution/Sale of Defective Microcircuit **AHA-A-10-01** Unauthorized Distribution/Sale of Defective Microcircuit **IE1-A-10-01** Semiconductor Device, Diode **AN4-A-10-01** 32K X 8 Non-volatile SRAM
Misc.	**FN4-P-10-01A** SMA Male to SMA Female "Micro" Attenuator **T9-A-10-01** Software Implementation Error, Triple Mode Redundancy

Multi-Level-Cell Flash for Space

Multi-Level-Cell (MLC) Flash is the next step in the evolution of NAND Flash technology. By storing multiple bits within a single memory cell, MLC achieves higher densities than single-level-cell (SLC) technology. Unfortunately, this comes at a price in terms of reliability. Because MLC technology uses tighter voltage margins when charging the floating gate in order to store multiple bits, it is more susceptible to weak-program errors, read disturb errors, errors due to total ionizing dose (TID) irradiation, and has a much lower endurance specification (about 1000x worse). Also, because threshold voltage margins are smaller in MLC, data retention performance is also decreased. These errors are typically soft errors, which come and go with program/erase cycles.

Hard failures occur when many program/erase cycles degrade the gate oxide beyond being able to successfully program or erase the cell. This happens with a few thousand program/erase cycles in MLC, and a few million cycles in SLC. Manufacturers typically define a conservative endurance spec of 5,000 cycles (MLC) or 100,000 (SLC).

Soft bit errors due to the phenomenon mentioned above are common in virgin devices right out of the box. Bit error rates also increase the more the device is used; program and erase operations are destructive to the memory cell and over time will exacerbate the effects of soft program and read disturb errors. Manufacturers typically require 1-bit ECC per 512-bytes for SLC and 4-bit ECC or greater per 512 bytes for MLC. Contact Jason Heidecker 818-393-7567.

JC-13.4 Radiation Hardness: Assurance & Characterization Meeting Synopsis

Leif Scheick, JPL radiation specialist, attended the JC-13.4 agenda in San Antonio, TX on Jan. 12, 2010. Four documents were reviewed. A draft of MIL-STD Test Method 1080 presented by Jeff Titus of the Naval Research Warfare Center was reviewed and comments were advanced to the author to be reviewed later.

This test method addressed testing of power MOSFET devices for Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB). A revised JEDEC alpha counting standard was also reviewed and re-tuned for final editing.

The purpose of this document is to specify the recommended method for measuring alpha emissivity in materials utilized in the manufacturing of semiconductors. This is a growing concern for terrestrial applications of VLSI device due to soft error rate.

Also reviewed was NASA's recent proton test guideline which specifies when proton testing for Single Event Effects is viable based on previous heavy ion testing. Finally, a JC-13.5 version of MIL-PRF-38534 appendix G was reviewed. This document is a performance specification for hybrid microcircuits. Only JEDEC members voted on the recourse of the document and it was advanced to a full committee vote. Contact Leif Scheick 818-354-3272.

Task Group Update: G-12 TG10-01 38535 Class Y (e.g., V-4 FPGA and similar parts)

Space-level requirements are being developed for Class Y non-hermetic devices. Recent survey results regarding these requirements are being collected and will be discussed at the next meeting in May. If you would like to be on the email list for surveys and updates, please contact Shri Agarwal 818-354-5598.

Industry Acquisition News

Microsemi Corporation has recently acquired White Electronic Designs Corporation headquartered in Phoenix, AZ. White Electronic delivers sophisticated multi-chip semiconductor packages, high-efficiency memory devices, and build-to-print electromechanical assemblies for defense and aerospace applications.

NASA parts specialists recently supported DSCC Audits of: STMicroelectronics; Avago Technologies; KCA Electronics; Trio-Tech; ACM-Coast; AVX Corp; Sensitron Semiconductor; Aeroflex Circuit Technology; ISE Labs; Presidio Components; International Rectifier; Semicoa Semiconductor; Raytheon Corp.

Upcoming Meetings

- JEDEC JC-13 Meeting, Nashville, TN. May 17-21, 2010 http://www.jedec.org/events-meetings/view_event/130
- NASA Electronic Parts and Packaging (NEPP) Electronic Technology Workshop, GSFC, June 22-24, 2010 http://nepp.nasa.gov/

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