

Flight Qualified Micro Sun Sensor for Mars Applications

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Abstract- A flight qualified micro sun sensor is being developed and flight qualified for future Mars missions. The micro sun sensor, which is basically a small pinhole camera, consists of a small mask with pinholes, placed on top of an image detector. Images of the sun are formed on the image detector when the sun illuminates the mask. Image processing is performed in the sun sensor that outputs sun centroids.

I. INTRODUCTION

Most NASA missions that have landed on the surface of Mars included one or more sun sensors. The sun sensors have been used to determine the heading of a rover or to establish 3-axis attitude information to point a high gain antenna toward earth. At the Jet Propulsion Laboratory, California Institute of Technology a novel Micro Sun Sensor (MSS) is being developed and flight qualified for future Mars missions [1-7].

The MSS is a miniaturized pinhole camera. The focal plane is an Active Pixel Sensor (APS) camera on a chip and the optics is a small piece of silicon wafer. APS chips have the advantage over traditional CCD chips that they are based on regular CMOS technology. This means that additional circuitry such as A/D converter, timing, and communication can be integrated on the focal plane itself. Furthermore an APS is inherently more tolerant to high-energy radiation damage than a CCD resulting in longer lifetime for APS. The APS chip that the MSS is based on has all camera functions integrated on the chip itself.

The optics of the miniaturized camera is a piece of silicon wafer with an evaporated layer of chrome and an additional gold layer on one side with a number of small pinholes in the gold layer. The silicon wafer is mounted on a spacer ~1000 microns from the focal plane making the system into a pinhole camera. The Sun is so bright that it will penetrate the silicon wafer through the apertures and the rays will form an image. This is basically the same principle as in a sundial. This is sketched in Fig. 1.

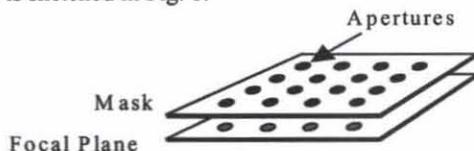


Figure 1. The MSS Concept

The MSS performs centroid calculations of the individual images and only outputs the centroid positions and the brightness to minimize the dataflow from the sensor. The MSS processing is implemented in a single FPGA to minimize mass and power consumption. The amount of logic that can be fitted in a single radiation tolerant FPGA is limited (~32,000 gates). Also, the lack of memory requires that all processing be done on the fly. The many design choices driven by the desire to simplify the complexity will be described in this paper.

All components used in the MSS have undergone qualification testing. This testing will be described and the results will be presented in this paper. Most components have been subjected to 1500 temperature cycles from -150 deg C to 25 deg C, to ensure survivability one Martian year on the surface of Mars.

II. MEMS MASK AND SPACER

A. Mask

The optics of the miniaturized camera is essentially a piece of silicon wafer with an evaporated layer of chrome and an additional gold layer with small pinholes. Fig. 2 shows a sketch of the mask (left) with a close up scanning electron microscope (SEM) image of the micro-fabricated mask pinholes (right).

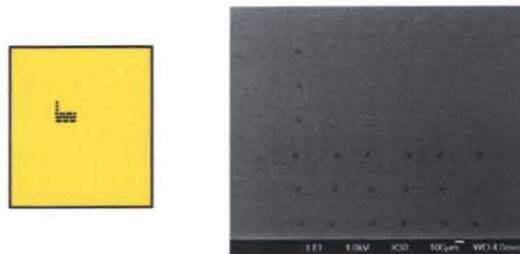


Figure 2. Sketch of the mask and close up SEM image of the pinholes

To fabricate a mask with 21 accurately aligned 50 μm diameter pinholes, MEMS micro-fabrication techniques are required. Fig. 3 shows the micro-fabrication steps. The substrate is 500 μm thick double-sided polished silicon wafer. First, Cr/Au (57nm/200nm) are deposited in an electron-beam evaporator as shown in Fig. 3 (b). Here, Cr layer works as an

adhesion promotion layer and Au works as a light absorber. Second, 1.4 μm thick AZ 5214 photoresist (PR) is spin coated on Au surface. And ultra-violet (UV) light is exposed on the photoresist through the pinhole pattern as shown in Fig. 3 (c). Since PR is a UV light sensitive polymer, it changes its state to etch-able in a developer when it is exposed to UV light. Thus, unexposed PR remains on the substrate as shown in Fig. 3. (d). The diameter of the PR is 50 μm for the pinhole. Next, the wafer is dipped into Au wet-etchant (a mixture of KI:I:DI solution). This solution etches the Au metal where it is exposed by the photoresist openings but leaves the Cr intact, as shown in Fig. 3 (e). Finally, the photoresist is stripped in acetone solution and the wafer diced.

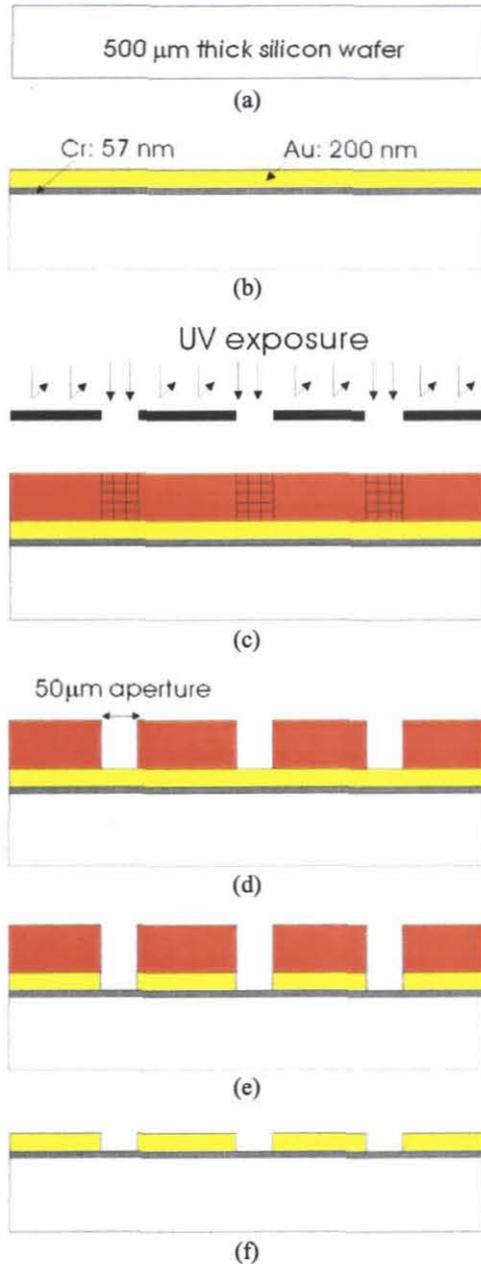


Figure 3. Micro-fabrication process steps for a MEMS pinhole mask

B. Spacer

The silicon mask cannot be mounted on the focal plane itself because of the high refractive index of silicon and reliability/vibration concerns. The objective of the spacer is therefore to separate the pinhole mask from the focal plane with a gap of $\sim 1\text{mm}$.

To fabricate a spacer, MEMS micro-fabrication techniques are also used to match the CTE of the MEMS mask. The starting wafer is 1.5 mm thick. The wafer has been etched through using Deep Reactive Ion Etching (DRIE) and the spacer is coated with gold as it is opaque to sunlight. Fig. 4 shows a photograph of the micro-fabricated spacer.

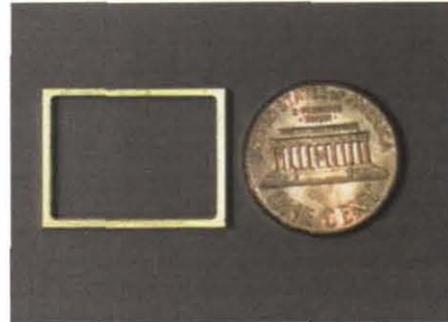


Figure 4. Photograph of spacer

III. APS DETECTOR

The Versatile Integrated Digital Imager (VIDI) 512 is a complete CMOS imaging system on a chip. The VIDI contains a 512 x 512 imaging array, 512 A/D converters (one for each column), D/A converters that control the internal reference voltages, currents, and a digital control block. The imager configuration is programmed through the serial input port. The configuration determines the pixel timing and ADC signals that are generated internally. After the imager is configured, a single command through the serial input port will cause image data to be taken. The images are output in parallel (one pixel at a time). The imager can be programmed to perform an internal column voltage offset correction to minimize column fixed pattern noise. A summary of the VIDI specifications is given in Table I.

TABLE I
SUMMARY OF MEASURED PARAMETER VALUES FOR VIDI

Characteristics	Values
Technology	CMOS, 0.5 μm
Outputs	Analog & Digital
Format	512 x 512
Pixel Size	12 μm x 12 μm
Responsivity	4 $\mu\text{V}/\text{photon}$
Quantum efficiency	3% (@ 1050 nm)
Dark Current	300 pA/cm ²
Noise	40 e ⁻
ADC resolution	10 bits (9.3 bits effective)
Power	10 mW @ 30 FPS

IV. PROCESSING ELECTRONICS

It was decided to implement the processing in a single FPGA to minimize mass and power consumption. A high-level block diagram is shown in Fig. 5.

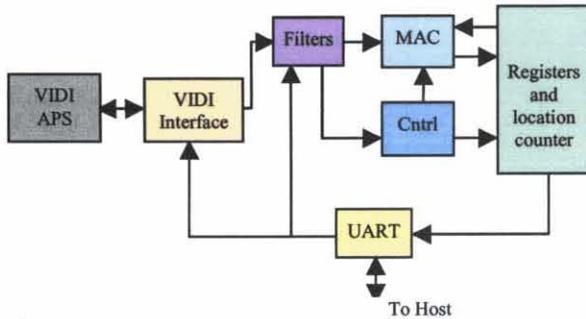


Figure 5. Block diagram of MSS Electronics

The small size of the Micro Sun sensor led to the selection of the Actel RT54SX32S FPGA, which is a radiation tolerant part. This small FPGA has only 32,000 gates to implement this design and decisions were made to reduce logic size and complexity. The lack of available memory in the device forced real-time computation of the centroid coordinates as data streams from the VIDI chip.

In response to an image command from the MSS FPGA, the VIDI chip outputs a 512x512 grid of pixels starting from location (0,0) and ending at location (511,511). The MSS FPGA tracks the current output pixel location for its algorithm. In an effort to reduce data-path and register widths, the 10 bit data output from the VIDI is reduced to 8 bits upon entering the FPGA (simulations have shown that this will not reduce the accuracy noticeably). The bit selection is controlled by an MSS environment variable that may be set by the host (spacecraft computer) prior to an operation.

The initial step of the MSS FPGA algorithm is to find the first bright pixel of the uppermost aperture. Once the reference window is found, the starting location of the four centroiding windows (each 32x32 pixels) is determined by adding a fixed offset to that location (-16, +96). It is imperative for the algorithm that any isolated bright pixels be removed from consideration before checking against the reference windows threshold. A hot pixel is considered to be any single pixel or two concurrent pixels that are at least a software set threshold greater than their row-wise neighbors. Any pixel deemed a hot pixel is replaced with the last pixel determined not to be a hot pixel. Fig. 6 sketches an example of the reference window (marked with a '+') and the location of the four centroiding windows. Notice, also, that certain isolated bright pixels have been ignored, due to the hot pixel filter.

Following the hot pixel filter is an offset filter to screen out offset pixels. For each pixel, a software set threshold is subtracted from the pixel value. If the value of the pixel is less than the threshold, the value of that pixel is added to a sum, and the number of pixels count is incremented by one. The sum and number of pixels count are relayed to the host

together with the centroiding data to help determine the correct settings for the MSS FPGA and the VIDI chip.

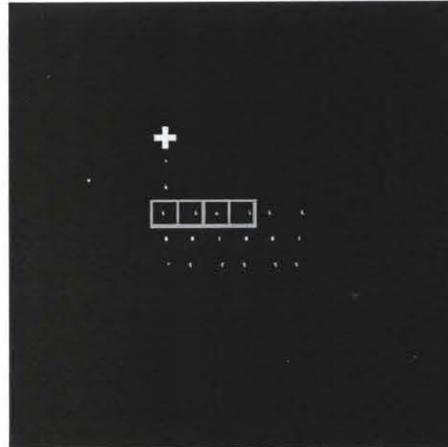


Figure 6. Selection of reference window and centroiding windows

Now that a pixel has been filtered for hot pixels and offset, the new value is compared to the reference window threshold to determine if it is the first bright pixel. Once the reference window is identified and the centroiding windows locations determined, the MSS FPGA then waits until the VIDI output reaches that point.

For each pixel in the four centroiding windows, the product of the x location counter and the pixel value are added to the current window's x moment register, the product of the y location counter and the pixel value are added to the current window's y moment register and the pixel value is added to the current window's energy sum register. To save space in the FPGA, these operations share a single booth-2 encoded multiplier and adder. The same adder is also used for calculating number of pixels over threshold count and the centroid window locations. Each multiply-accumulate operation takes 5 clock cycles in addition to 4 stages of pipelining. The moment registers are each 21 bits wide, of which the upper 20 bits are returned to the host at the end of the VIDI output. Adding the extra bit to the register reduces the chance of an overflow, but the extra bit cannot be returned to the host as the UART only sends 5 bits of data per byte returned. If any register does overflow, an error flag is set and the host must decrease the integration time of the VIDI chip or the noise threshold of the MSS FPGA.

The mask is designed to cope with a situation where one of more of the apertures are blocked (e.g. Mars dust). Fig. 7 is a sketch of a case where 3 apertures have been disabled including the reference aperture. Also, the whole aperture pattern has moved to a new location due to a different sun angle. The new reference window is marked with a '+'. Note that a different set of centroiding windows have been selected, because they are now the correct offset from the reference window.

In this case the FPGA will still output 4 centroids, the third of which will have a value close to 0 because of the

aperture blockage. The host can still identify the selected centroids, because the distance between the apertures on each of the rows is unique – this is the reason that the apertures appear a little skewed in Fig. 2.

Finally, note that each row actually has 6 apertures. This is to allow the host to select, at run time, whether to use the left 4 apertures or the right 4 apertures on a row. This allows the host to use 6 apertures over 2 exposures for greater accuracy.

The 'pseudo' code for the FPGA image processing is shown in Fig. 8.

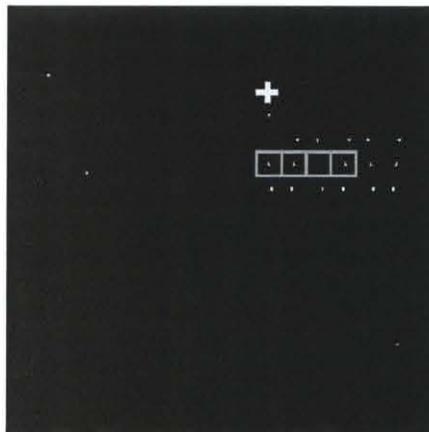


Figure 7. Sketch of blocked apertures and new reference window

```

% go though image (avoid edges)
for y=1:16:512-16,
    for x=1:16:512-16,
        % this is the hot pixel filter. Set pixel to previous pixel, if gradient is larger than
        % threshold in previous transition and next or one more next transition
        if (yhile(y,x)-yhile(y,x-1)>hotpixel)&((yhile(y,x)-yhile(y,x+1)>hotpixel)| (yhile(y,x+1)-yhile(y,x+2)>hotpixel)),
            yhile(y,x)=yhile(y,x-1);
        end
        % if this is the first bright pixel, record it as the identifier aperture
        if ((yhile(y,x)-background)>threshold)&(identifieraperturemeet==0),
            xleadingaperture=x;
            yleadingaperture=y;
            identifieraperturemeet=1;
        end
        % record pixel if we found identifier aperture and we are within the area of centroid 1
        if (identifieraperturemeet==1)&(x>xleadingaperture+2-16)&(x<xleadingaperture+2+16)&(y>yleadingaperture-16+96+2)&(y<yleadingaperture+16+96+2),
            pixelvalue=max(yhile(y,x)-background,0);
            xprod1=xprod1+(x-1)*pixelvalue;
            yprod1=yprod1+(y-1)*pixelvalue;
            sum1=sum1+pixelvalue;
        end
        % record pixel if we found identifier aperture and we are within the area of centroid 2
        if (identifieraperturemeet==1)&(x>xleadingaperture+2-16+32)&(x<xleadingaperture+2+16+32)&(y>yleadingaperture-16+96+2)&(y<yleadingaperture+16+96+2),
            pixelvalue=max(yhile(y,x)-background,0);
            xprod2=xprod2+(x-1)*pixelvalue;
            yprod2=yprod2+(y-1)*pixelvalue;
            sum2=sum2+pixelvalue;
        end
        % record pixel if we found identifier aperture and we are within the area of centroid 3
        if (identifieraperturemeet==1)&(x>xleadingaperture+2-16+64)&(x<xleadingaperture+2+16+64)&(y>yleadingaperture-16+96+2)&(y<yleadingaperture+16+96+2),
            pixelvalue=max(yhile(y,x)-background,0);
            xprod3=xprod3+(x-1)*pixelvalue;
            yprod3=yprod3+(y-1)*pixelvalue;
            sum3=sum3+pixelvalue;
        end
        % record pixel if we found identifier aperture and we are within the area of centroid 4
        if (identifieraperturemeet==1)&(x>xleadingaperture+2-16+96)&(x<xleadingaperture+2+16+96)&(y>yleadingaperture-16+96+2)&(y<yleadingaperture+16+96+2),
            pixelvalue=max(yhile(y,x)-background,0);
            xprod4=xprod4+(x-1)*pixelvalue;
            yprod4=yprod4+(y-1)*pixelvalue;
            sum4=sum4+pixelvalue;
        end
    end
end
end

```

Figure 8. 'Pseudo' code for the FPGA

V. COELOSTAT TESTING

JPL's Coelostat Sun Simulator facility (at Table Mountain Observatory) was used to test the sun sensor. The facility contains a coelostat, which is simply a "sun tracker". The heliostat consists of a mirror mounted on an axis parallel to the earth rotation axis. The sunlight bounces off this mirror and onto another mirror that corrects for small changes in declination primarily due to refraction in the atmosphere and directs the light onto the micro sun sensor. The light bundle will always come from the same direction. A picture of the coelostat is shown in Fig. 9.

A 2-axis gimbal holding the micro sun sensor is rotated through a large number of different angles and images are recorded. Based on all these measurements, it is possible to derive the relationship between the centroids and the sun

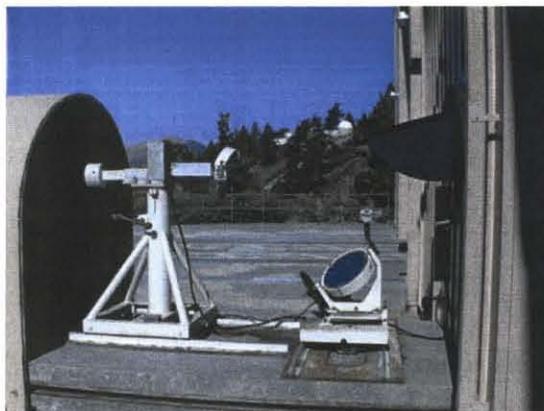


Figure 9. The coelostat at JPL

angles. It is basically an over determined set of equations, where hundreds of measurements are used to determine the camera parameters. A picture of the 2-axis gimbal with the micro sun sensor is shown in Fig. 10. A detailed discussion and the equations for doing this calibration is given in [5].



Figure 10. The 2-axis gimbal used to calibrate the micro sun sensor

An actual image acquired by the micro sun sensor from the calibration where the image is displayed in false color scale to enhance details is shown in Fig. 11. It is observed that there are ghost images in the top-right part of the image.

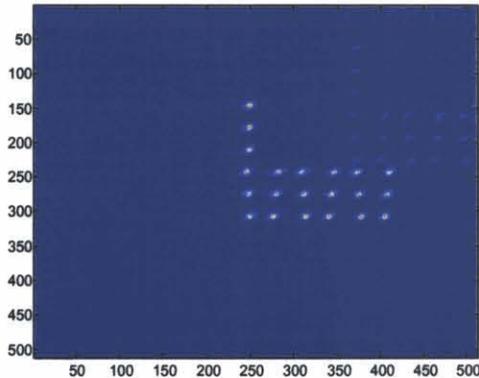


Figure 11. An image acquired by the micro sun sensor from the calibration

When the host receives the x sums, y sums, and brightness sums for each aperture, it divides the x and y sums with the brightness sum to avoid that the FPGA has to do the division. Based on the distances between the centroids, it is also able to identify which row of centroids it used. The next step in the algorithmic flow is to transform the (x,y) centroids into sun angles. A simple pinhole camera model is used.

The accuracy of the sun sensor depends on over how large a field of view that it is calibrated to operate and is defined as the average calibration residual. To determine the accuracy from a single aperture, data were collected for different sizes of FOV. The result is shown in Fig. 12.

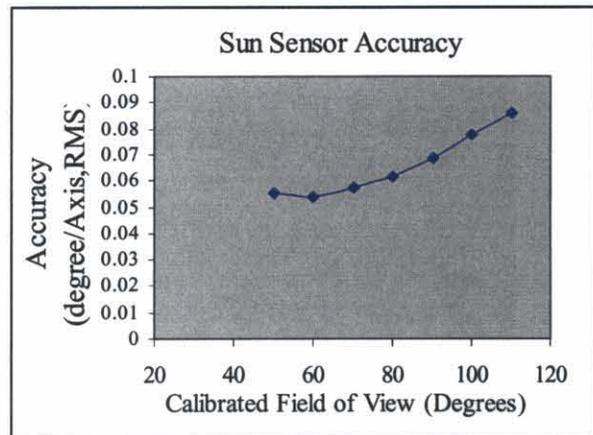


Figure 12. Sun sensor accuracy

It can be seen in Fig. 12 that reducing the FOV to less than 70 degrees does not improve the accuracy significantly. The reason for this was investigated and the cause was found to be the ghost images (seen in Fig. 11). Simulations have shown that the current accuracy is limited by ghost images with an intensity of 5-10%. A reflection from the focal plane onto the shiny gold mask and back to the focal plane causes the ghost images. Currently, work is undergoing to replace the bright gold mask with a less reflecting material.

VI. QUALIFICATION PROGRAM

The Thermal Cycle Resistance Electronics (TCRE) program has been initiated at JPL in order to develop a comprehensive electronics parts selection, design rules and packaging techniques for the future long duration Mars missions. These missions will need to survive the thermal cycle stresses induced on electronics when exposed to the Martian ambient environment. The TCRE is chartered to 1) develop a packaging technology and 2) identify electronics components to satisfy the requirements for Mars missions.

A. Electronics Components

The Commercial Off The Shelf (COTS) electronics components offer a very low cost solution for the construction of electronics systems for Mars applications including the MSS. COTS are nominally tested to military specifications (-55°C to 125°C) but there is no published data on their performance for colder temperatures on the Martian surface (-120°C to 25°C). Therefore a series of tests are being performed under the TCRE program to determine the functionality of the parts used in the MSS (APS, line drivers, regulators, clock, FPGA, resistors, capacitors, and connector) at -150°C (with -30°C added margin). For screening purpose at first the parts are subjected to a short-term low temperature. After passing this test they are then soaked for 1000 hours. Currently all MSS parts have been screened and are under 1000 hours of soak.

B. Packaging Evaluation

To maintain an overall small package the MSS electronics is designed to fit on a single two-sided board-employing chip on board technology (Fig. 13). The FPGA selected is a 32K gate device with the smallest footprint available.

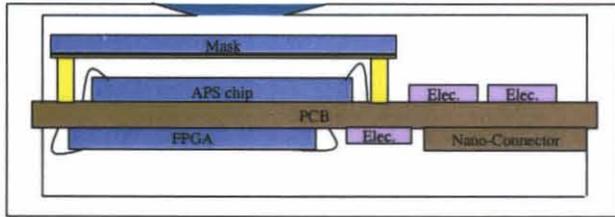


Figure 13. MSS Package

The MSS TCRE packaging tests entail 1) assess the reliability of the internal die and wire bond interconnects of the FPGA package (Fig. 14) and 2) Evaluate the structural attach reliability of different adhesives for the aperture to spacer and spacer to substrate interface and evaluate the dimensional stability of the surface of the aperture to the base substrate, in the -120°C to 85°C thermal cycling environment (Fig. 15).

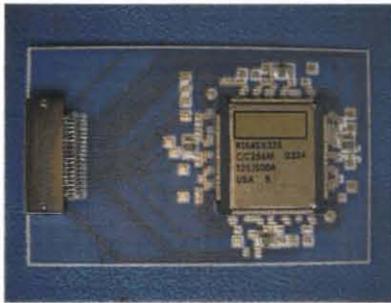


Figure 14. MSS FPGA TCRE Package

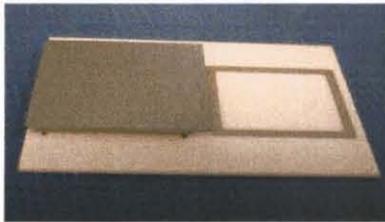


Figure 15. MSS Mask & Spacer TCRE Package

Currently there are 4 boards using different adhesives for bonding the FPGA are under TCRE tests and have accumulated between 250 to 400 cycles. Additionally there are 10 packages of the Mask/Spacer that are being tested and have accumulated between 100 to 1000 cycles.

VII. SUMMARY

A tiny gold and chrome plated silicon wafer is bonded on top of a spacer that is bonded to the PCB over the APS chip that is mounted with chip onboard technology. The APS chip contains all camera functions on the chip. The mask consists of 21 pinholes, but the MSS typically only outputs 4 centroids. The sun angle can be determined based on the position of the aperture centroids – just like a sundial.

Projected specifications for the MSS are shown in Table II.

TABLE II
SUMMARY OF MEASURED PARAMETER VALUES FOR VIDI

Parameter	Value
Mass	<35 grams
Power consumption	<300 mW
Accuracy	<0.2° when sun is <20° from the boresight, <0.5° when the sun is >20° from the boresight
Update rate	2 Hz
Interface	UART
Field of view	+/- 60°
Slew rate	>12°/sec

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