

Temperature-adaptive circuits on reconfigurable analog arrays

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Abstract

This paper describes a new reconfigurable analog array (RAA) architecture and integrated circuit (IC) used to map analog circuits that can adapt to extreme temperatures under programmable control. Algorithm-driven adaptation takes place on the RAA IC. The algorithms are implemented in a separate Field Programmable Gate Array (FPGA) IC, co-located with the RAA in the extreme temperature environment. The experiments demonstrate circuit adaptation over a wide temperature range, from extremely low temperature of -180°C to high 120° .

1. Introduction

In-situ planetary exploration requires extreme-temperature electronics able to operate at very low temperatures e.g. -230°C on the Moon in permanently shadowed areas, or very high temperatures, e.g. -470°C on the surface of Venus. Terrestrial applications mostly for high temperature electronics, include combustion systems, well logging, nuclear reactors and dense electronic packages.

In addition to material/device approaches to extreme temperature electronics, circuit solutions for the compensation of temperature effects have also been proposed. Circuit solutions that compensate offset voltage and current leakage are described for example in [1], where several circuit topologies for high-temperature design, including a continuous-time auto-zeroed OpAmp and an A/D circuit that uses error suppression to overcome high-temperature leakages, are given. Another circuit for high-temperature operation with current leakage compensation is

presented in [2]. Bias cancellation techniques for high-temperature analog application are presented in [3].

Previously proposed solutions are fixed circuit designs, which satisfy the operational requirements for a given temperature range; once the limits of the range are exceeded, the performance deteriorates and cannot be recovered. A reconfigurable chip that allows for a large number of topologies to be programmed, some more suitable for high-temperature, was introduced in [4]. The interconnections between components could be changed, and new circuits could be configured, in an arrangement that used the on-chip components/devices at a different operational point on their characteristics. These experiments were performed using ICs based on the Field Programmable Transistor Array (FPTA) architecture described in [5].

This paper introduces a different reconfigurable chip architecture, called the Reconfigurable Analog Array. Components of the RAA can be used to implement filters and amplifier circuits, in particular Gm-C filter architectures whose behavior can be tuned by bias voltages. These circuits have been previously identified as good candidates for evolutionary-driven correction/compensation by Higuchi's group in Japan, who demonstrated how evolution by genetic algorithms can correct functional deviations in filter characteristics, greatly improving the yield, saving area at design time, and reducing the power needs [6]. In the work described here, the same concept of operational transconductance amplifiers (OTAs) controllable by programmable biases is used, this time in the context of correcting for operational deviations induced by extreme temperatures. As opposed to a post-manufacturing calibration as is the case of the application described in [6], in our case the adaptation is continuous since the circuits have different optimal

points for different temperatures. Compared to adaptation by changing circuit topology as was the case of the circuits mapped into FPTA, the RAA employing bias voltage/current compensation offers the advantage of improved analog performance (bandwidth, signal to noise ratio) due to the fact that there are no switches in the signal path within the RAA cell.

The paper describes the RAA architecture and IC implementation, a system built around the RAA and an FPGA mapping the algorithms used to control/compensate the RAA, the setup for the temperature experiments and a set of tests that show how temperature induces functional deviations in the operation of analog filter, and the adaptation mechanisms are able to provide the correction to recover functional operation down to -180°C , as well as at high temperatures to 120°C . The paper is organized as follows: Section 2 provides architecture and circuit description of the RAA. Section 3 briefly describes the self-adaptive system which includes FPGA, ADC and DAC, a more detail description being provided in [7]. Section 4 illustrates the results and discusses future work. Section 5 presents the conclusions.

2. Reconfigurable Analog Array

The main component of the RAA are the analog cells using Operational Transconductance Amplifiers (OTAs) or Wide Range Transconductance Amplifiers (WRTA) [8]. These are used to implement Gm-C filters that can be tuned through the change in biasing voltages to meet specifications at extreme temperatures. The WRTA topology is shown in Figure 1.

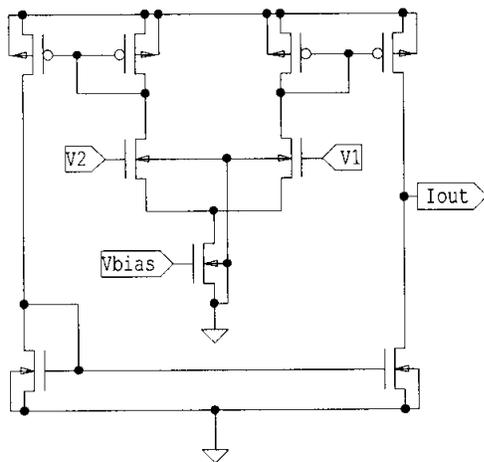


Figure 1. WRTA topology

The WRTA transconductance is G_m dependent both on the temperature and on the voltage applied to V_{bias} , which in fact can be used to attempt compensation for changes in temperature. Figure 2 depicts a first-order Gm-C filter implemented using two WRTAs [9]. This topology can implement different low-pass/high-pass filters depending on the values of V_{bias} and on the capacitors.

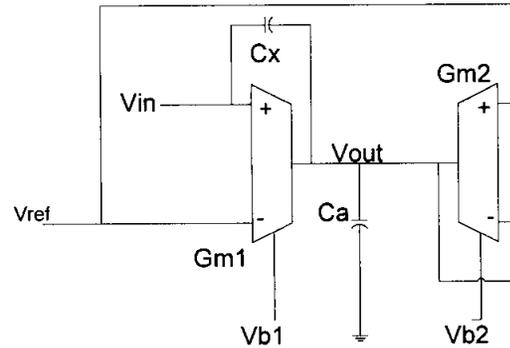


Figure 2: First Order Gm-C Filter

A prototype RAA IC was fabricated as an array of 4 first-order Gm-C filters interconnected by switches. The topology presented below utilizes a reduced number of switches on the signal path, which improves the bandwidth characteristics comparing to the FPTA chip [5]. The RAA IC was fabricated using TSMC 0.35u technology.

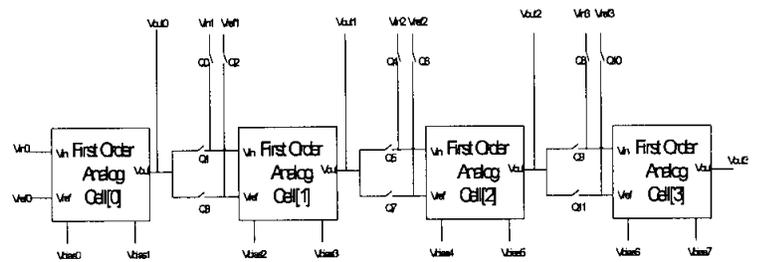


Figure 3. First-order filter array.

3. Self Adaptive System

A self adaptive system able to compensate the deviation of its analog functions was built around an RAA analog board and a FPGA Virtex-II Pro protoboard [7]. The analog board is a modular design, consisting of a motherboard (RAA board) and a number of daughter boards for data conversion and power distribution. Currently there are 3 daughter boards for digital to analog conversion (DAC boards using AD9772 devices); and one daughter board for

analog to digital conversion (ADC board using LTC1745 device). Two DAC boards send bias voltages (programmed by the FPGA) to configured the RAA, and the third one sends the input signal synthesized by the FPGA to the RAA. The ADC board reads back the RAA output to the FPGA board. In the future more daughter boards will be added as the applications become more complex. The FPGA controls reconfiguration based on search algorithms seeking solutions over bias voltage values. Current algorithms include a hill-climbing algorithm and a genetic algorithm.

4. Experimental Results

In initial experiments only the RAA chip was placed in the extreme temperature chamber, and only a single array cell was used, controlled by two bias voltages, Vb1 and Vb2. The initial setting of Vb1 and Vb2 were 0.9V and 0.7V respectively. This setting produces a low pass filter with a cut-off frequency around 100kHz and about 20dB gain in the passing band.

Figure 4 shows that a small deterioration in the filter response is observed at 120°C. After manually changing the bias voltages Vb1 and Vb2 to 1.1V and 0.6V respectively, a partially recovered response was achieved. The deterioration of the filter characteristic was more clearly observed at low-temperatures. Figure 5.a shows that the frequency response degrades for temperatures below -120°C. A functional recovery was performed through a manual local search over the two bias voltages Vb1 and Vb2 at -180°C. It was observed that a simple change in Vb1 from 0.9V to 0.8V produced a partial recovery in the circuit functionality. This is shown in Figure 5.b. Analog to digital converters and digital to analog converters were also tested as individual components before the entire system was executed.

Follow-on experiments were performed on the entire self-adaptive system consisting of both RAA board with RAA IC, ADC and DACs, and the FPGA board, in the temperature chamber. In the initial configuration, Vb1 and Vb2 were set to 1.02V and 0.66V respectively, configuring a low-pass filter with similar characteristics of the previous one. Figure 6 shows an oscilloscope picture of the input and output voltages at room temperature, where the voltage gain is around 10 (frequency of 50kHz). The filter response does not change too much until the temperature in the chamber goes down to around -170°C, when the gain at the passing band is drastically reduced. Figure 7 shows the degraded filter response at -180°C.

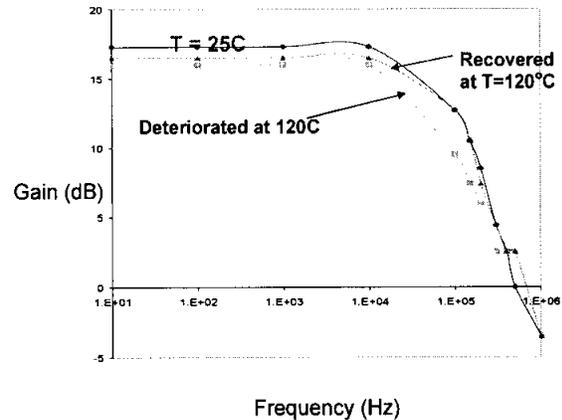


Figure 4. Low-pass filter frequency response when the temperature goes up to 120°C.

The circuit recovery was performed by a hill-climbing-inspired algorithm, which searched over the bias voltages Vb1 and Vb2, and also over the input voltage (V_{in} if Figure 2) offset (initially set at 1.5V). Several solutions in which the gain is partially recovery were found by the algorithm. The partially recovered response shown in Figure 8 corresponds to a circuit whose bias voltages are 1.89V and 1.31V respectively. The input offset voltage was reduced from 1.5V to 1.19V. The recovered voltage gain was around 3.

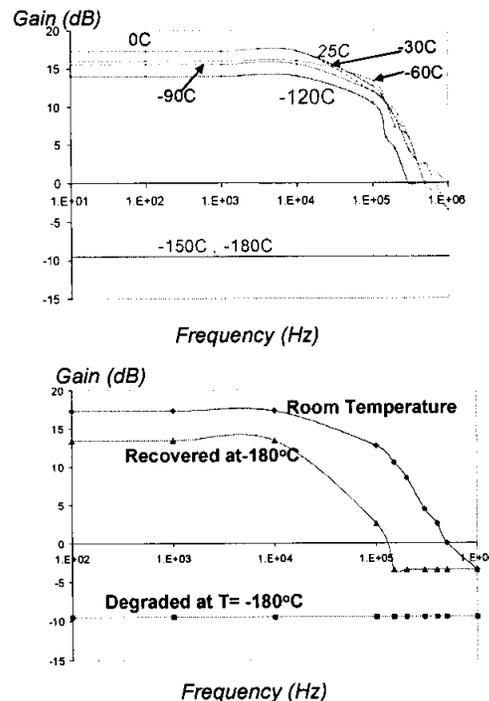


Figure 5. (a) Low-pass filter frequency response as temperature goes down to -180°C; (b) partial recovery at -180°C

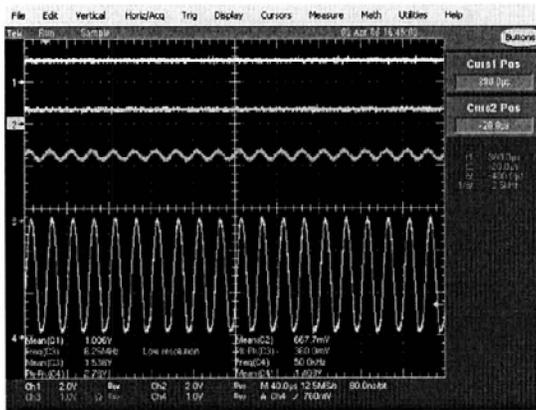


Figure 6. Oscilloscope response of first order filter at room temperature at 50kHz. Waveforms (from top to bottom) correspond to Vb1, Vb2, filter input and filter output.

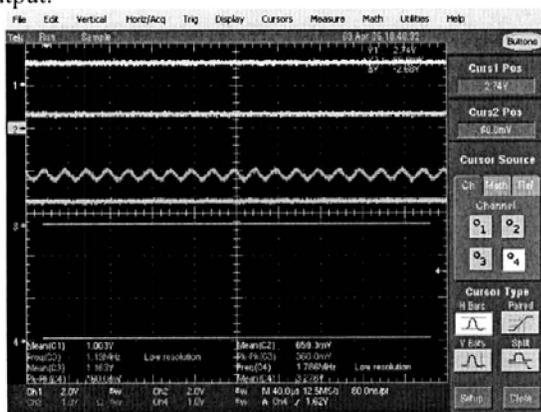


Figure 7. Oscilloscope response of first order filter at -180°C at 50kHz. Waveforms (from top to bottom) correspond to Vb1, Vb2, filter input and filter output.

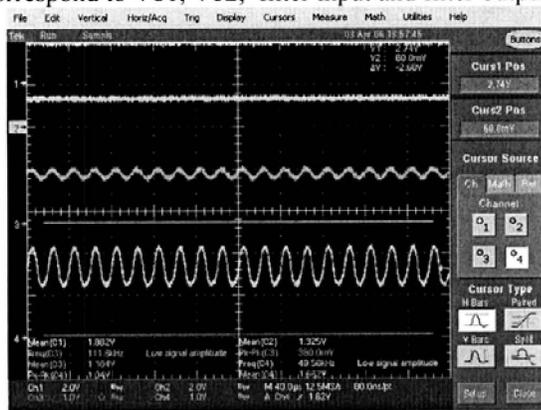


Figure 8. Oscilloscope response of first order filter at room temperature at -180°C at 50kHz (Recovery). Waveforms (from top to bottom) correspond to Vb1, Vb2, filter input and filter output.

5. Conclusions

The paper presented a system that adapts to temperature extremes, compensating for deviations of its analog behavior using search algorithms. The preliminary results presented in this paper will be followed by test for the recovery of higher order filters and also circuit recovery under the combined effects of extreme temperature and radiation.

6. Acknowledgments

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