

# 324GHz CMOS VCO Using Linear Superimposition Technique

Daquan Huang<sup>1</sup>, Tim R. LaRocca<sup>1</sup>, Lorene Samoska<sup>2</sup>, Andy Fung<sup>2</sup> and Frank Chang<sup>1</sup>

University of California, Los Angeles, CA<sup>1</sup>, Jet Propulsion Laboratory, California Institute of Technology,  
Pasadena, CA<sup>2</sup>

Terahertz (frequencies ranged from 300GHz to 3THz) imaging and spectroscopic systems have drawn increasing attention recently due to their unique capabilities in detecting and possibly analyzing concealed objects. The generation of terahertz signals is nonetheless nontrivial and traditionally accomplished by using either free-electron radiation, optical lasers, Gunn diodes or fundamental oscillation by using III-V based HBT/HEMT technology[1-3]. These prior techniques suffered major disadvantages of size, cost, complexity and sometimes even the need of cryogenic cooling[2]. CMOS has never been considered for terahertz applications due to its low cut-off frequency of  $f_{\max}$ . The highest reported CMOS oscillation frequency to date is 192GHz through a 2<sup>nd</sup> order push-push method[4]. We have substantially extended the operation range of deep-scaled CMOS by using a *linear superimposition method*, in which we have realized a 324GHz VCO in 90nm digital CMOS with 4GHz tuning range under 1V supply voltage. This may also pave the way for ultra-high data rate wireless communications beyond that of IEEE 802.15.3c and reach data rates comparable to that of fiber optical communications, such as OC768 (40Gbps) and beyond.

Our new approach does not rely on device nonlinearities, but employs linear superimposition of multiple phase-shifted ( $2\pi/N$  in sequence, where  $N$  is an integer greater than one) and rectified fundamental signals ( $\omega_0$ ) to produce a superimposed output signal at the intended frequency of  $N\omega_0$ . The algorithm can be comprehended graphically in Fig.1 by taking  $N=4$  as an example. Phase shifted signals of  $I_p=I_0\sin(\omega_0t)$ ,  $I_{Qp}=I_0\sin(\omega_0t+\pi/2)$ ,  $I_{Im}=I_0\sin(\omega_0t+\pi)$  and  $I_{Qm}=I_0\sin(\omega_0t+3\pi/2)$  are generated by a quadrature VCO. These signals are then rectified and linearly superimposed to produce the final output signal of

$$I_{\text{output}} = I_A + I_B = I_0 \left( |\sin(\omega_0 t)| + |\cos(\omega_0 t)| \right) = \frac{4}{\pi} A_I I_0 \left( 1 - \frac{2}{3 \cdot 5} \cos(4\omega_0 t) + \dots \right) \quad (1)$$

where  $A_I$  is the rectification gain. As clearly indicated in Eq.1, the superimposition has canceled the fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonics and leaves the 4<sup>th</sup> order term with a **fundamental-to-4<sup>th</sup> Harmonic** signal conversion efficiency of

$$\eta_I = (8/(15\pi) \cdot A_I I_0) / (I_0) = 8/(15\pi) \cdot A_I \quad (2)$$

By setting  $A_1 \sim 1$ , the results in  $\eta_1 = 17\%$  or  $-15.4\text{dB}$ , which is significantly higher than that of traditional harmonic generation or push-push approaches [2, 4] in order to achieve the equivalent frequency multiplication factor of four.

This new  $4\omega_0$  frequency generation technique has distinct advantages of: (1) higher signal conversion efficiency and output power due to self-cancellation of the fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonics, (2) simplified external filtering requirement to lower ( $<4$ ) harmonics leading to more compact circuit design and lower power consumption, (3) the  $4\omega_0$  output signal may be phase-locked by a PLL at the fundamental frequency  $\omega_0$  for achieving faster settling time and broader locking range.

The circuit schematic shown in Fig.2 explains the proposed linear superimposition algorithm. The fundamental oscillation frequency is chosen as  $f_0 = 81\text{GHz}$ , which is about half of the NMOS  $f_{\text{max}}$  (160GHz) for sufficient  $g_m$  to commence the oscillation. The quadrature VCO, consisting of cross-coupled twin VCO cores, generates quadrature phases of fundamental signals at frequency  $\omega_0$ :  $V_{ip}(0^\circ)$ ,  $V_{im}(180^\circ)$ ,  $V_{qp}(90^\circ)$  and  $V_{qm}(270^\circ)$ . These signals are then converted into corresponding output currents of  $I_{ip}$ ,  $I_{im}$ ,  $I_{qp}$  and  $I_{qm}$ , respectively, via the transconductance stage which also rectifies the output current signals. The four rectified currents are subsequently superimposed to deliver the output signal at the desired frequency of  $4\omega_0$  via an inductive load of  $Z_L$ .

Each VCO core consists of a cross-coupled NMOS pair ( $M_1$  to  $M_4$ ) of  $W/L = 2.4\mu\text{m}/90\text{nm}$  with a differential inductor load of  $L = 0.3\text{nH}$ . These cores are twist-coupled by  $M_5$  to  $M_8$  with  $W/L = 2\mu\text{m}/90\text{nm}$  to complete the quadrature VCO. Devices  $M_9$  to  $M_{12}$  with  $W/L = 10\mu\text{m}/90\text{nm}$  are used to form transconductance stages with a common output load of  $Z_L = 0.2\text{nH}$ . The transconductance stages rectify input quadrature signals and produce the output signal at  $4\omega_0$ .

The VCO performance is characterized by JPL with the test setup illustrated in Fig. 3. The DUT output is probed on-wafer using a custom-designed GSG WR3 waveguide probe with a cutoff frequency of 173 GHz, which ensures no signal will pass below the cutoff frequency into the mixer. The oscillator signal is fed into a sub-harmonic mixer (SHM) pumped with an LO signal of 160GHz. The LO is generated from a synthesizer set at 20GHz followed by a frequency quadrupler and doubler. Two W-Band PA modules and one variable attenuator are inserted between the quadrupler and doubler to boost the 80GHz tone while suppressing high-order harmonics. Under various bias conditions ( $V_{DD} = 1 \sim 1.2\text{V}$ ,  $I_{DC} = 12 \sim 16\text{mA}$ ), the output frequencies of more than ten VCOs vary between 319GHz to 325GHz.

Figure 4 shows a representative test data of the output frequency and power. The measured output power with a  $50\Omega$  load is about  $-76\text{dBm}$  before calibration. With the test setup loss of about  $30\text{dB}$ , the calibrated output power at  $324\text{GHz}$  is estimated as  $-46\text{dBm}$ . Additionally, a  $-26\text{dBm}$  output power at  $81\text{GHz}$  is measured from a separate fundamental-signal-only VCO on the same wafer. Considering the  $15.4\text{dB}$  signal conversion loss given by  $\eta_1$  of Eq. 2, this yields  $4\omega_0$  output power of  $-41.4\text{dBm}$  at the  $324\text{GHz}$ . The minor output power discrepancy from two methods,  $-46\text{dBm}$  versus  $-41.4\text{dBm}$ , may be caused by variations of loss between different test setups and equipment. Figure 5 illustrates measured VCO tuning range of  $4\text{GHz}$  by varying the control voltage between  $0\sim 2\text{V}$  across the varactor of  $C_{\text{var}}$ . The rejection of lower-order harmonics is also confirmed by measuring the fundamental tone at the output node. No fundamental tone is observed above the  $-80\text{dBm}$  noise floor. The high fundamental tone rejection at the output node ( $>39\text{dB}$ ) is attributed to the linear superimposition algorithm and the designated inductive loading at  $4\omega_0$ . The  $2^{\text{nd}}$  and  $3^{\text{rd}}$  harmonics are beyond the range of our  $110\text{GHz}$  spectrum analyzer but should have even lower output power than that of the fundamental tone. Due to the lack of equipment capable of measuring the phase noise directly at  $324\text{GHz}$ , we estimate its phase noise level of  $-78\text{dBc/Hz}$  at  $1\text{MHz}$  frequency offset by adding  $-20\text{Log}(4)\text{dB}$  (i.e.  $-12\text{dB}$ ) to the measured phase noise of  $-90\text{dBc/Hz}$  of the fundamental signal from a separate fundamental-signal-only VCO. Table 1 summarizes the  $324\text{GHz}$  CMOS VCO performance and Figure 6 shows the die photo.

In conclusion, a linear superimposition technique is devised to generate terahertz ( $324\text{GHz}$ ) output signal of  $-46\text{dBm}$  in  $90\text{nm}$  CMOS with a **fundamental-to-4<sup>th</sup> Harmonic** signal conversion efficiency of  $17\%$  or  $-15.4\text{dB}$ . The associated phase noise is estimated as  $-78\text{dBc/Hz}$  and  $-91\text{dBc/Hz}$  at  $1\text{MHz}$  and  $10\text{MHz}$  offset, respectively. The fundamental tone is rejected at the output node by at least  $39\text{dB}$  without additional filtering. The circuit draws  $12\text{mA}$  from  $1\text{V}$  supply and occupies a core area of  $210\times 180\mu\text{m}^2$ . The frequency tuning range is measured as  $4\text{GHz}$  with output power variation less than  $5\text{dB}$ .

#### References

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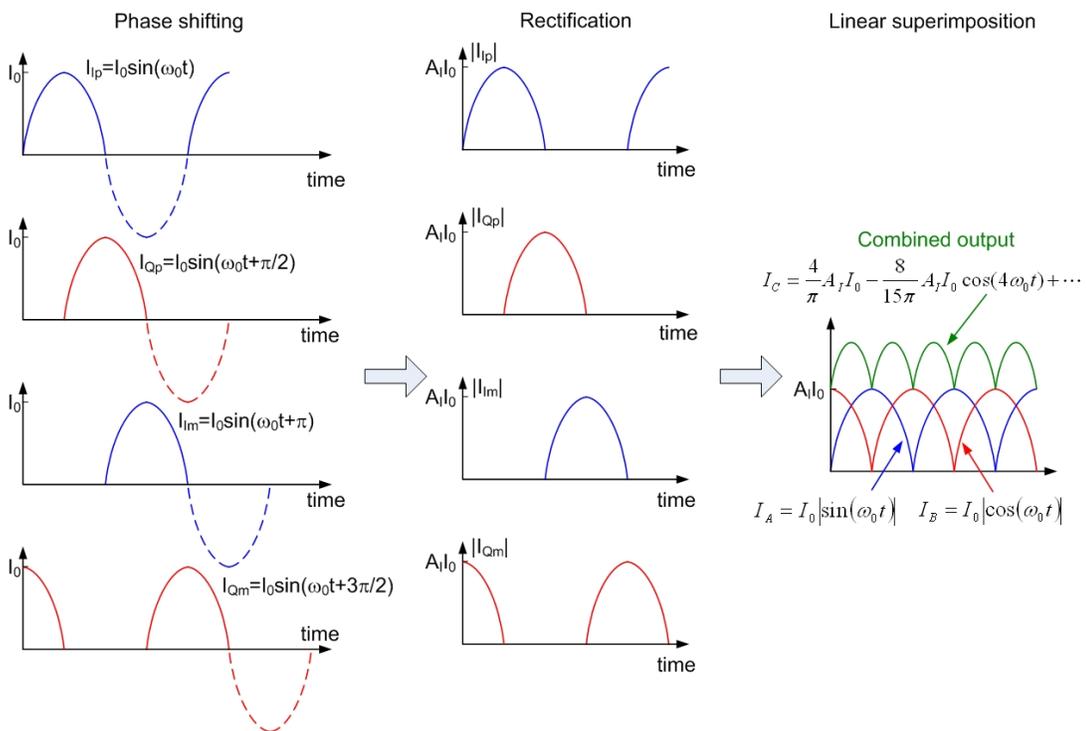


Fig. 1 Linear superimposition of phase shifted fundamental signals to generate  $4\omega_0$  output signal

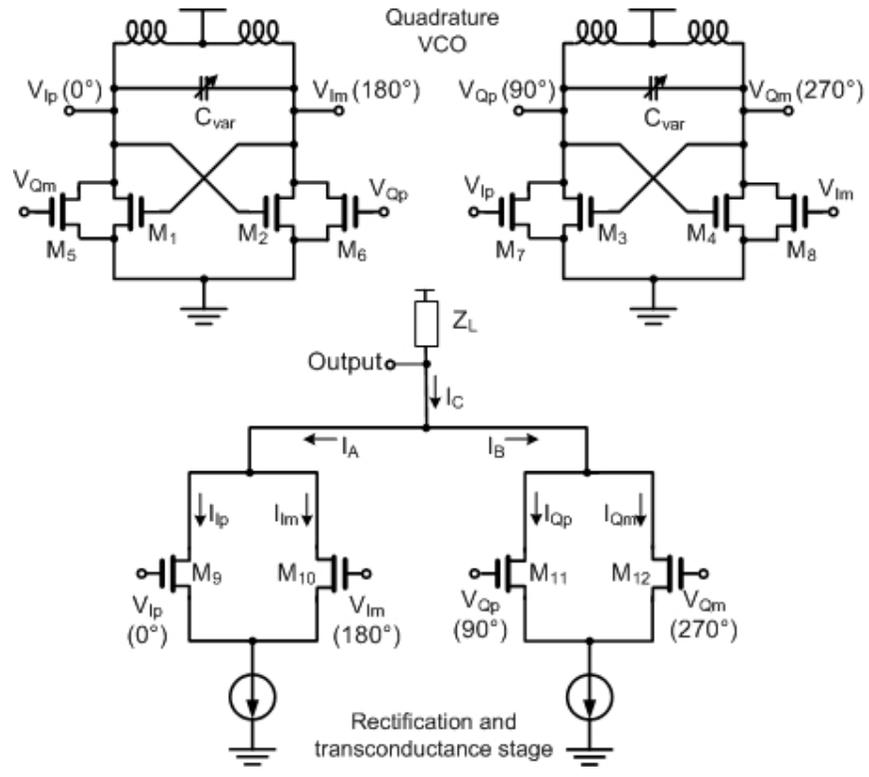


Fig. 2 324GHz ( $4\omega_0$ ) VCO implementation based on linear superimposition method

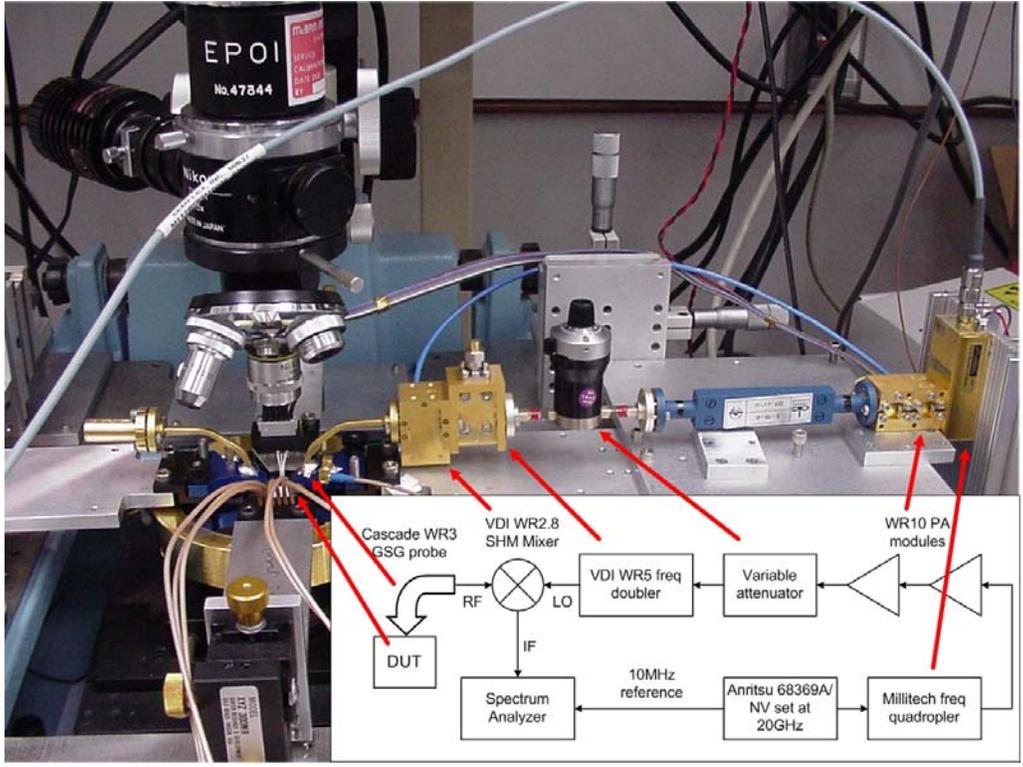
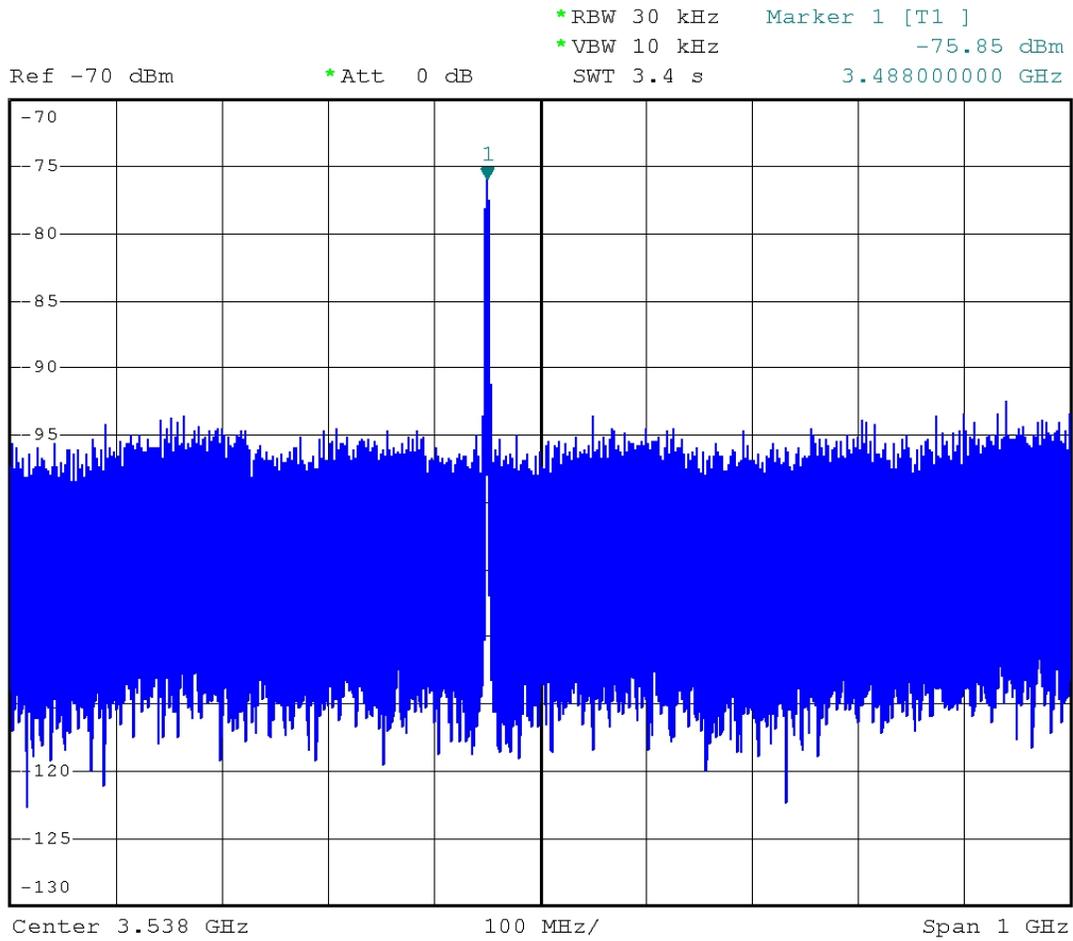


Fig. 3 324GHz test setup at JPL



Sub-harmonic mixing frequency is  $(f_{VCO} - 2 \cdot f_{LO}) = f_{IF}$ , or  $f_{VCO} - 2 \cdot (20 \cdot 4 \cdot 2) = 3.5$  GHz, yielding  $f_{VCO} = 323.5$  GHz.

Fig. 4 Measured  $4\omega_0$  or 324GHz output signal at a pre-calibrated -76dBm or post-calibrated -46dBm output power

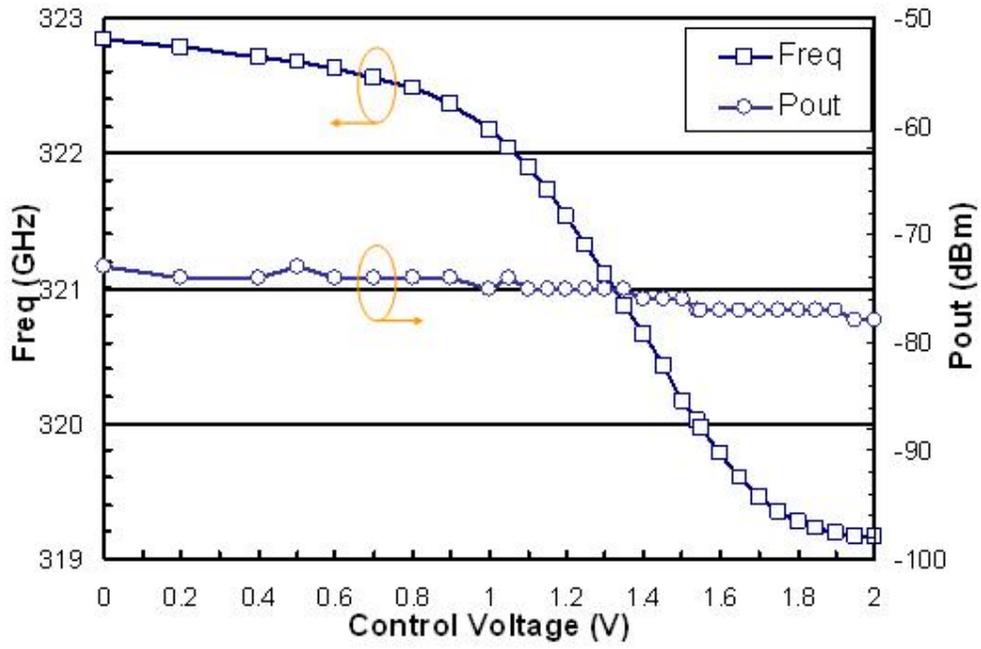


Fig. 5 Measured VCO frequency tuning range

Table 1 324GHz CMOS VCO Performance Summary

Functions	Performance
Output Frequency	324GHz
Frequency Multiplication Factor	4X
Calibrated Output Power	-46dBm
Maximum Fundamental-to-4 <sup>th</sup> Harmonic signal Conversion Efficiency	17% or -15.4dB
Measured Rejection of Fundamental signal	>39dB
Tuning Range	4GHz
Estimated Phase Noise based on Measured Phase Noise at Fundamental	-78dBc/Hz at 1MHz offset -86dBc/Hz at 5MHz offset -91dBc/Hz at 10MHz offset
Supply Voltage	1V
Current Consumption	12mA
Chip Core Area	210x180 $\mu\text{m}^2$

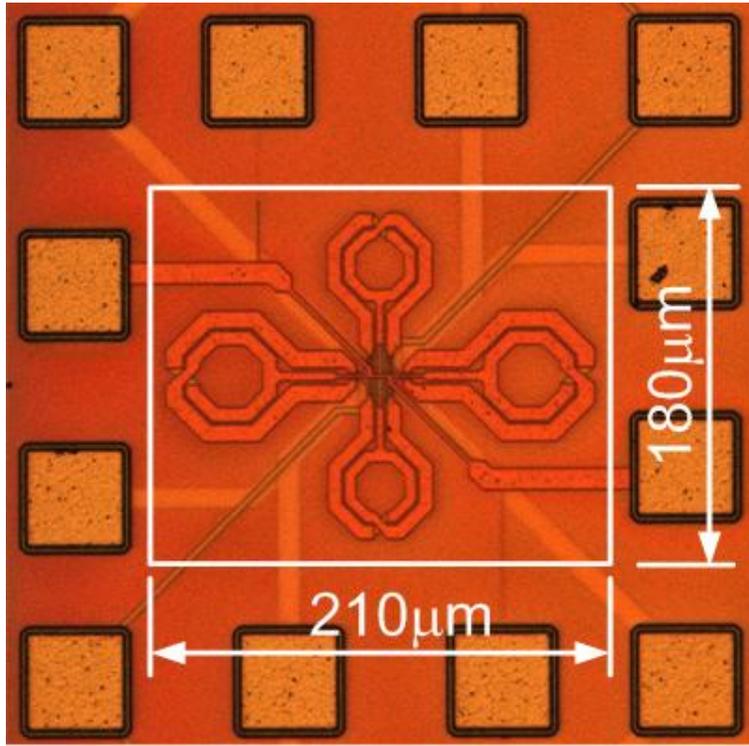


Fig. 6 Die photo