The Effect of Integration of Strontium-Bismuth-Tantalate Capacitors onto SOI Wafers.*

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We report for the first time the successful integration of Strontium-Bismuth-Tantalate ferroelectric capacitors on an SOI Substrate. We have verified that the unique processing requirements of SBT capacitors does not affect the properties of the surrounding FD-SOI transistors, and, conversely, we have verified that the SOI processing does not affect the quality of the SBT capacitors.

Motivation

The integration of SBT capacitors on SOI substrate was borne out of a request by NASA's Jet Propulsion Laboratory to develop a suitable replacement for a non-volatile memory element used for start-up/boot-up code for a processor selected for use on the Prometheus Deep Space mission.

The use of SOI was considered a natural selection due to its well known capabilities in terms of operation through and after exposure to intense ionizing radiation fields.[1] The use of SBT capacitors as data storage elements was also a natural selection due to its well-known improved performance and processability when compared to other materials, such as PZT (Lead-Zirconium-Tantalate).[2]

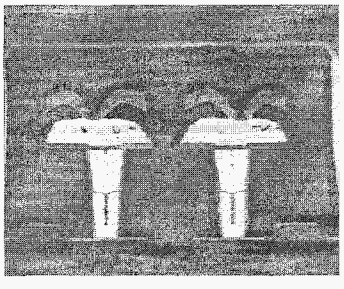

Figure 1: Fully integrated SBT capacitors on FD-SOI

For this development, Metal Organic Decomposition (MOD) SBT solution commercially available from Kojundo Chemicals, Japan was applied to Unibond SOI wafer by Oki Electric Industry at their Hachiouji fab. The technology chosen was Oki's 0.2 μm scale FD-SOI transistors.

Novelty

We have, for the first time, successfully integrated Ferro-electric capacitors of any type (in this case, SBT) onto SOI substrate by overcoming several factors, namely the etching of very-deep tungsten plugs with an aspect ratio of 5.5 on ultra-thin S/D region (50 nm) , the development of two-step plugs under ferroelectric capacitor without the use of an interstitial pad in order to mitigate the stress to ultra thin SOI, and the modification of the SBT capacitor formation temperature profile resulting in elimination of an increase in back-channel leakage.

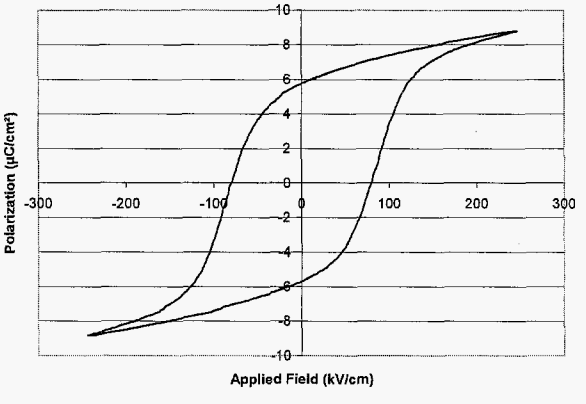

Figure2: Hysteresis of an integrated SBT capacitor (2 μm²) on FD-SOI

* This development funded, in part, by NASA's Jet Propulsion Laboratory, Pasadena, California, under contract 1265898, in support of NASA Task Order 7107141 and the NASA Prometheus Program.

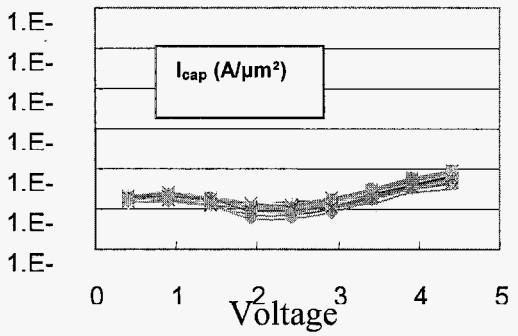

Figure 3: Leakage of an integrated SBT capacitor(2 μm²) on FD-SOI. Multiple point test.

Device Performance

Figure 2 and 3 show the characteristics of SBT ferroelectric capacitors fully integrated into 0.2 μm FD-SOI with three layers of metallization, nitride passivation, and $CoSi_2$ contact process. The SBT film thickness is 120 nm. As can be seen, good hysteresis loops with excellent leakage characteristics are obtained on these integrated capacitors thus qualifying them for memory operation. Figure 4 shows the Ids-Vg characteristics of SOI transistors. The two plots compare the transistor characteristics with and without SBT capacitor integration. The data confirms that integration process of SBT capacitor has negligible effect on the SOI transistor characteristics and thus FD-SOI transistors can be integrated with SBT ferroelectric capacitors for ultra high speed and ultra low power non-volatile memory fabrication.

Total Ionization Dose

For this purpose a test chip was designed with numerous transistor varying in the width-to-length ratio. Structures with the use of body ties and enclosed body architecture to control cell leakage were also designed.

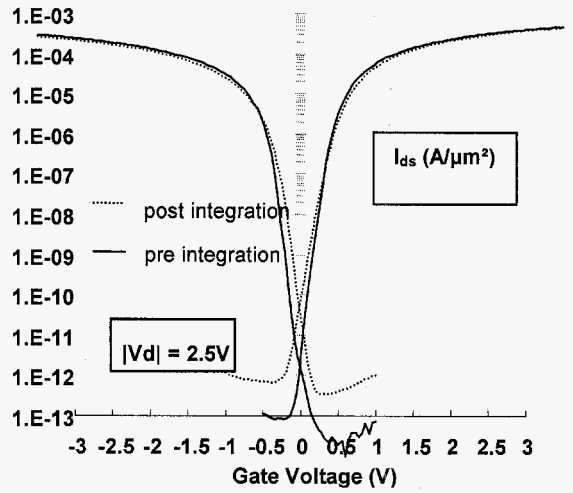

Figure 4: Comparison of Ids-Vgs curves of FD-SOI transistors (0.35 x 10 μm) with and without SBT capacitors.

Radiation testing was performed by Bruce Black of Raytheon, Sudbury Massachusetts [3]. Bias conditions were set to establish worst case conditions for the surface gate oxide.

Table 1 shows the conditions for each test. For transistors with the body ties to source, only the drain was biased.

Testing was performed from 0 kRads to a level of 300 kRads in six steps of 30, 60, 100, 200, and 300 kRad exposures. The transistors were tested *in-situ* immediately following exposure to alleviate the effects of annealing. Following exposure, two devices were annealed for approximately 168 hours at 100C to examined the stability of radiation induced trapped charge and to look for interface state formation.

A total of 22 NMOS devices from wafer wafers and of various configurations were tested. Similarly, 13 PMOS devices were tested as well.

Table 1 - Radiation Bias Conditions

Tran-sistor Type	Condition	Drain	Gate	Source	Body (separate contact)	Substrate
N	CMOS ON	0V	3.3V	0V	0V	0 or -2V
	CMOS OFF	3.3V	0V	0V	0V	0 or -2V
P	CMOS ON	3.3V	0V	3.3V	3.3V	0 or -2V
	CMOS OFF	0V	3.3V	0V	0V	0 or -2V

Test Results

For CMOS devices, the usual method of determining the effect of ionization is to look for shifts in voltage threshold. However, this is problematic in a Fully Depleted SOI device as the silicon film is so thin (< 75A) that there is a strong coupling between the top gate and the buried oxide.

Figure 5, below, shows the pre-exposure threshold dependence on Substrate voltage for one transistor type. Each curve corresponds to a different voltage applied to the substrate (back gate). As is apparent, the measured threshold voltage (corresponding to a drain current of around 1 □A) will vary by nearly a volt for a 15V change in substrate voltage. For this device a substrate voltage of more than about 6V will result in inversion of the back interface when the gate voltage is at 0V, leading to substantial current flow when the device is nominally OFF.

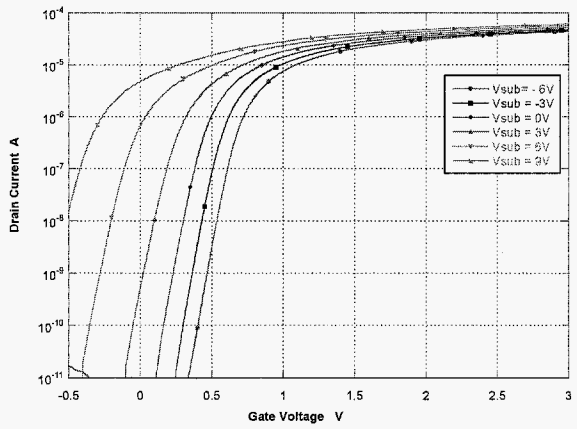

Figure 5 – Pre-Radiation Threshold Dependence on Substrate Voltage, NMOS

Figure 6 is a graph from one set of samples of NMOS type transistors. For all devices, the "ON" bias condition with the gate biased to 3.3V and all other terminals grounded resulted in the least threshold voltage shift. Note, however, that at the 200kRad mark, the threshold exhibits a notable shift, suggesting that interface states are being formed.

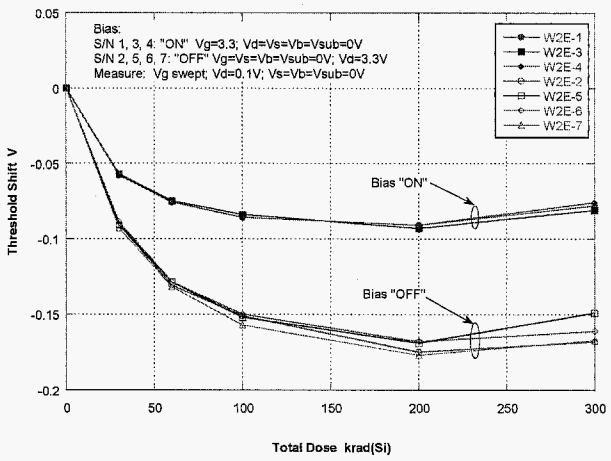

Figure 6 – Post-Irradiation Threshold Voltage Shift, NMOS

Anneal Effects

Following exposure, two NMOS transistors were subjected to high temperature annealing (100C) for approximately 168 hours. Both devices had been exposed to the 300kRad level. One device, from one wafer set, exhibited a "super recovery" effect consistent with interface state formation: having final thresholds some 200mV above pre-exposure levels. The other device did not exhibit this effect.

This suggests that the two sets of parent wafers experienced different processing techniques. Which is exactly the case. For the sake of establishing a Control, one wafer, the one exhibiting the Super Recovery, was extracted from the foundry run immediately prior to the establishment of the Ferro capacitors. However, to the wafer was exposed to processing temperatures consistent with sintering of the SBT material. The other wafer, the one exhibiting a "more normal" behavior received all processing steps.

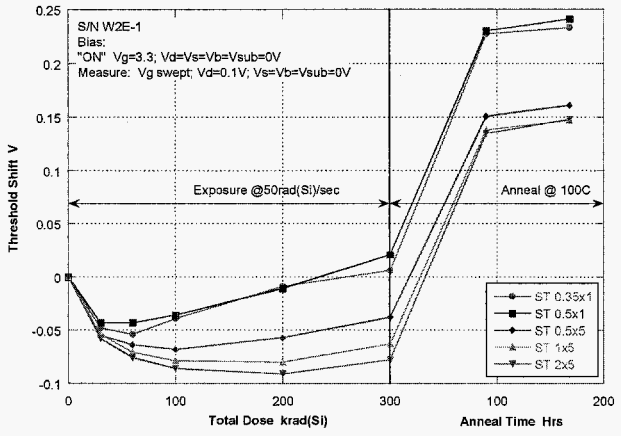

Figure 7 – Post-Irradiation Threshold Voltage Shift, NMOS, Wafer 2 parent

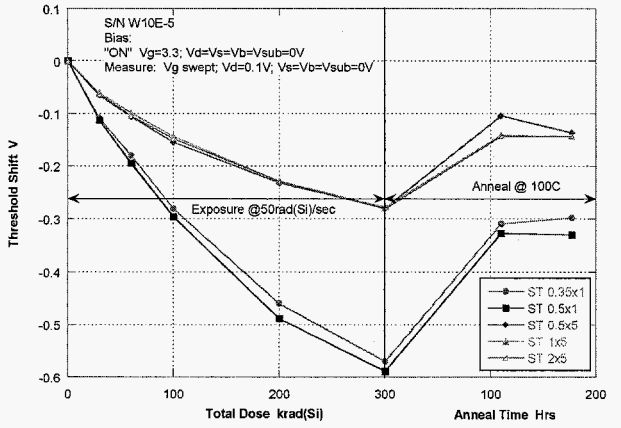

Figure 8 – Post-Irradiation Threshold Voltage Shift, NMOS, Wafer 10 parent

Conclusion

We have shown that SBT ferroelectric capacitors can be successfully integrated onto FD-SOI wafer with no degradation in either leakage or capacitor performance. We have shown that the process challenges of etching of deep tungsten plugs with large aspect ratios on ultra-thin Si is possible and finally we have shown processes specific to ferroelectric capacitor do not affect the FD-SOI transistor characteristics.

However, we have shown that the effect of such a narrow silicon film greatly affects the performance of the OKI FD-SOI process in a radiation environment. The dependence on radiation bias with threshold shifts for devices biased "OFF" much greater than for those biased "ON" is consistent with the previously proposed hypothesis that the "ON" bias condition maximizes any charge trapping in the gate oxide while the "OFF" bias condition maximizes charge trapping in the buried oxide due to fringe fields between the drain and body or source.

Future Developments

With the proof-positive that one can successfully integrate SBT ferroelectric capacitors onto SOI with no deleterious effect on either, opens the door to a new generation of memory devices for almost any practical use: from wristwatches and cell phones to deep space missions, the Holy Grail of non-volatility, low power, high speed and high radiation immunity is, at once, achieved. Further study is required to determine if the OKI partially depleted SOI process is amenable to the radiation environment.

References

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[2] C. A. Araujo, J. D. Cuchiaro, M. Scott, L.D. McMillan, "Fatigue free properties of SBT on Pt electrodes," Nature, vol. 374, pp. 627, 1995

[3] [3] Test Report, DRD004, Raytheon Company to Symetrix Corporation, JPL Subcontract 1265898