The Pulse Width Modulator ASIC for Deep Space Missions

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The Jet Propulsion Laboratory has started the development of a Pulse Width Modulator Application Specific Integrated Circuit (PWMA). This development is leveraging the previous development of the Switch Control ASIC (SCA). The purpose of the development is to provide the control for a selected range of power converter topologies and to meet the stringent environmental requirements of deep space missions. The PWMA will include several power control functions that are not normally included on the off-the-shelf components available today. One key functional requirement is the ability to implement an N + K redundant power converter with the ability to control the charging of a battery. Other applications will be the typical point of load isolated and non-isolated power converters. The purpose the development is not only to provide a much needed flight part, but also to accelerate the engineering process by using a standard cell library from previous ASIC developments.

Under previous developments with Boeing and Lockheed Martin, JPL has produced three ASICs. Each ASIC has been implemented by using an analog standard cell library. One such development was the SCA, which is design to provide a floating power switch control. The functional verification of this ASIC has been completed and the cells used have been targeted for the new development of the PWMA.

The primary function of the PWMA is to provide the control function of a point of load power converter. The design is an isolated 60 W converter with a 3.3 V output. In architecting the design, several functions were left up to the power converter design in order to make the ASIC more generic. The ASIC can be used for several power converter topologies and power levels.

Some additional features have been added to the ASIC to provide the interfaces for multi-phase topologies and battery control functions. An N+K fault tolerant strategy has been implemented in order to provide the battery control functions.

The PWMA has been developed to provide an ASIC with several functions not normally available in the off the shelf controllers. These functions have been added to enable the power converter designers to achieve fault tolerant designs and battery control functions. The footnote on the first page should list the Job Title and AIAA Member Grade for each author.

I. Introduction

The Deep Space Avionics is a Jet Propulsion Laboratory development currently funded under the technology program of the Jupiter Icy Moons Orbiter (JIMO) Project. The primary goal of the development is to develop avionics that can meet the Jovian environment. The technology was originally funded under the X2000 project and has continued to be funded under the JIMO project.

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The Deep Space Avionics development includes the power system electronic technology. The power system electronics development has focused on radiation hardened (Mrad) custom mixed signal ASICs for control circuits as well as advanced multi-chip-module packaging for power applications. The power products are targeted for an unregulated 28 volt power system. The power products leverage several building blocks from the mixed signal ASIC developments. To date, a command interface chipset, switch control chip set and a power converter control chip set have been developed. Each of these ASICs have been fabricated and functionally tested with good results.

The Pulse Width Modulator ASIC development is the next step in this development, which is to provide the control function of several different power converter topologies. The previous power converter control chipset was targeted for a single low power topology. The new ASIC will combine the chipset into a single ASIC and will be open to several different power converter topologies and power levels.

II. Development Goals

The goal of this development is to provide a controller that can be used for multiple power converter developments and meet the Jovian environmental requirements. The controller physical attribute can be as a single component or a chipset that can be packaged in a number of different formats such as a surface mount package, chip on board, hybrid or multi-chip-module.

The controller would need to apply to several different topologies that can cover the basic needs of a deep space spacecraft. The previous chipset development was for a 30W dual forward power converter. In the new development, we want to open up the topologies to cover a wider range of power levels and applications. One such application is a power control function for a spacecraft with energy storage. Another function is an isolated point of load power converter with a demanding flight computer as the load. The third application is a non-isolated house keeping power supply for the power system with bootstrap capability. Each application offers very different design requirements for the controller as well as packaging configurations.

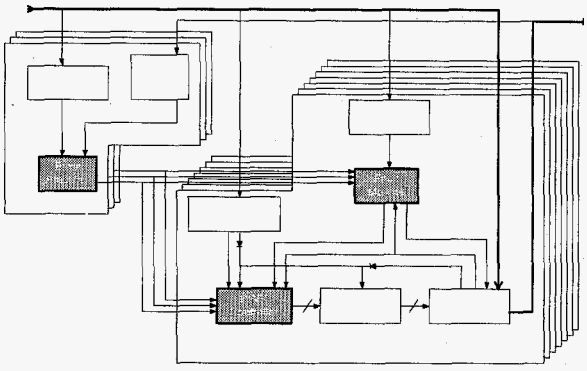


Figure 1: High Power Reference Application

The reference designs were selected to set the boundaries of what is required for this ASIC. The most challenging reference design is the fault tolerant high power battery controller (fig. 1). This requires fault tolerant interfaces, fault tolerant phasing of the power stages and power stage fault monitoring. These requirements make this ASIC unique as compared to available components. The two other reference designs provide constraints on the resources such as power, pins and capability to disable the functions. A design that requires too much power would not make it viable for the lower power applications. Several functions must have external access in order for it to be used ore disabled depending on the application. This approach increases the require pins and external components.

The Jovian environment pushes our development to a radiation hardened process at Honeywell. This process has been used for the previous ASIC developments and an extensive custom analog library has been developed. The environment is not only challenging for total dose, but provides a challenge in single event effects and heavy ion effects that must be considered in the design and layout of the ASIC.

Another goal is to develop a controller that is independent of the line voltage or bus voltage. External components will be used to provide the voltage isolation or level translation for housekeeping power and interfaces. The purpose of this goal is to be able to use the controller for higher power systems that might have an increased bus voltage.

III. Development Approach

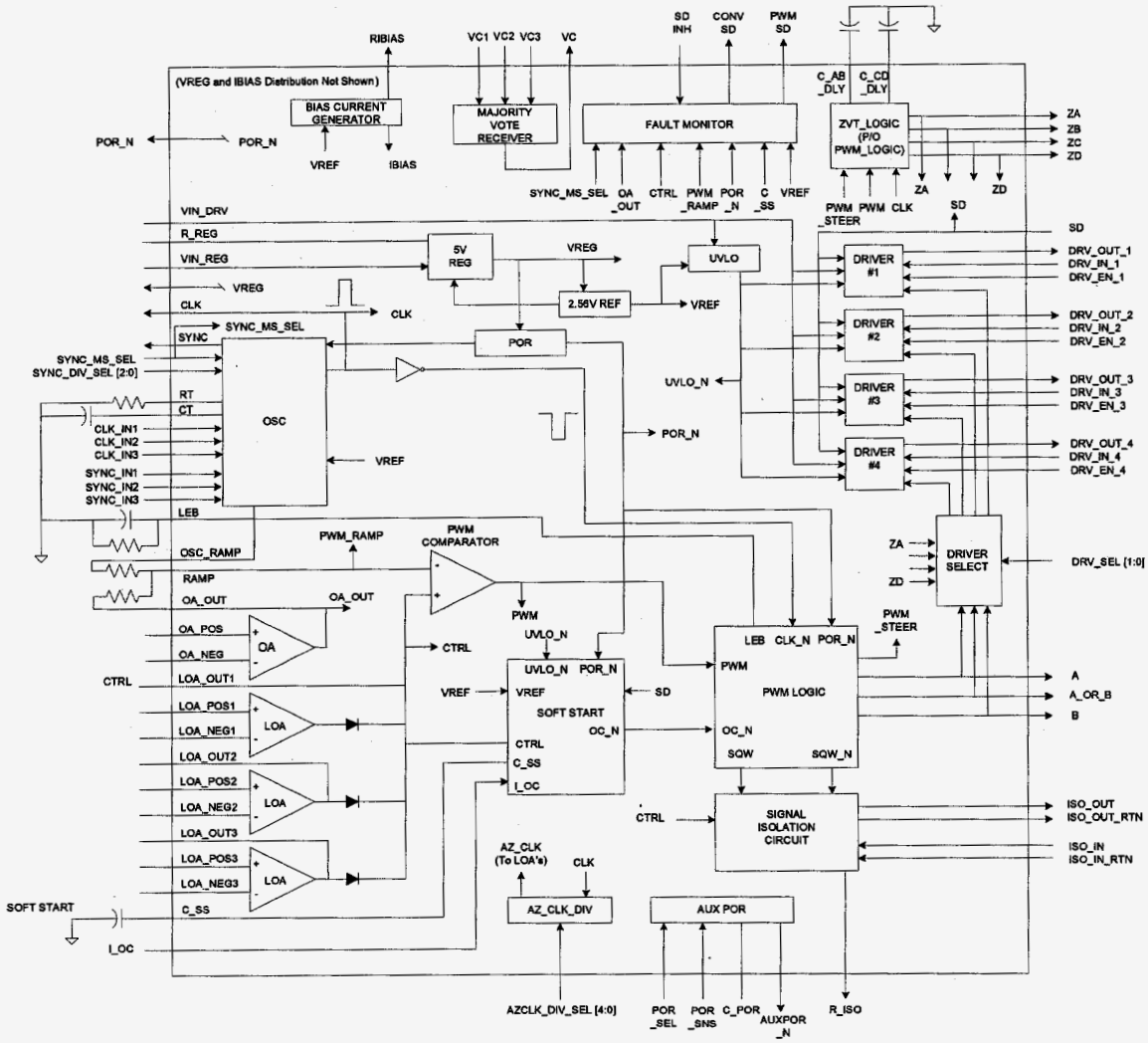
The development approach is similar to the previous developments that were started under the X2000 project. The initial step in the development was completed by Boeing Solid State Electronics Division. An analog library was fabricated on the Honeywell HX2000 process. The library was characterized and tested for total dose. That library is the foundation for several ASIC developments to follow.

The first development to use the library was the first pulse width modulator ASIC (PWMA) and synchronous rectifier controller ASIC (SRCA). These ASICs were designed for a 30W dual forward power converter. The ASICs

were fabricated and functionally tested in a power converter breadboard. The ASICs were approximately 90% functional with two design issues. One was a latch up into a lower voltage with a slow power supply ramp up and the other was a protection clam set at too low of a voltage. We learned that the library was functioning as predicted and that the only issue where with the functional design that it was difficult to simulate and verify prior to test.

The second development was the Switch Control ASIC (SCA) chipset. The two SCAs were designed to provide control for a power distribution switch for an unregulated 28V system. Both ASICs have been fabricated and functionally tested in a multi-chip-module. Several of the larger functional building blocks will be used for the next development. Under the SCA development, a library worst case data base was produce in to perform worst case analysis within the ASIC. This investment in the data base has reduced the amount of time it takes to develop an architecture and conceptual design. It also reduces the amount of simulations required for verification.

The previous ASIC developments lead into this development, which combines the previous PWMA and SRCA into a single ASIC also named the PWMA. Several of the larger level functional cells from the previous developments are targeted for this application. This development is focused on the system design and architecture of the ASIC with the lower level library cells being verified and fabricated. The purpose of this development is to provide many of the functions not available in the off-the-shelf PWM controllers such as interfaces for fault tolerance and multiple control loops.



PWMA FUNCTIONAL BLOCK DIAGRAM
(Preliminary 6-15-04)

Figure 2: Functional Block Diagram of the PWMA

IV. PWMA Functional Description

Based on the development goals, a functional design was developed to meet the requirements of the three reference designs. A functional block diagram was developed that captured the bulk of the functional requirements (fig. 2). The functional block diagram might look similar to many of the off-the-shelf pulse width modulator controllers with the exception of the majority voted interfaces, internal fault monitoring, multiple control loop capability and on chip drivers.

Starting with the flow of power, the on-chip voltage regulator is designed to use external high breakdown voltage components to decouple the ASIC from the line voltage. The Honeywell HX2000 process is a 5V process. We have added some higher voltage transistors for level translation and MOSFET drivers, but the bulk of the library is based on a 5V power supply. The circuit has been designed to startup on a linear regulator using external power devices to provide 12V to the ASIC, which can be biased off once the converter has started. The 5V power on the chip is provided by the linear regulator. The 12V power is available for the MOSFET drivers. Most of the linear control and digital components are powered off the 5V line. The 12V line has an under voltage lockout to prevent driving the power MOSFETs until the 12V line is stable. In a similar approach, the power on reset (POR) circuit holds off the logic and analog circuits until the 5V power is stable.

The voltage reference (2.56V REF) is a standard Honeywell cell that has been fabricated and tested several times. This reference is provided throughout the ASIC for many of the bias current generators, ramp functions, fault monitors and control circuits. The bias current generators provide the reference current for all of the amplifiers and comparators.

The oscillator is a challenging design because of the derived requirements for a power control function. The power control reference design is a high power step down converter that must provide fault tolerant control of the battery on the output. The architecture uses an N+K fault tolerant multi-phase power stage with a majority voted central controller. This architecture requires a majority voted master clock input for all of the power stages and a majority voted synchronization signal for proper phase control (fig, 3). The purpose of the oscillator cell is to enable an N+K fault tolerant architecture for power control applications. The multiphase approach works for large power converters as well as fast response lower power applications. There are up to eight phases that can be selected with external connections. The oscillator can be used in a non-synchronized application with a free running clock internal to the cell.

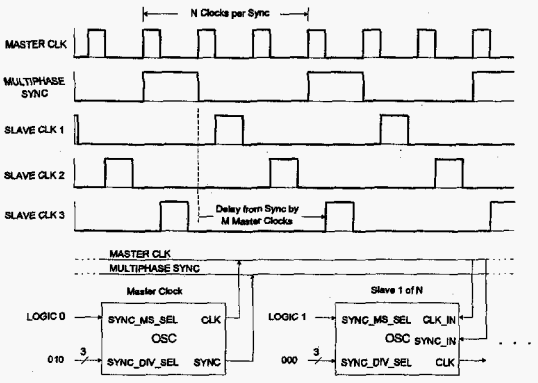


Figure 3: Clock and Phase Configuration

The ramp is controlled by external components and triggered by the oscillator. An amplifier has been added to allow for primary current compensation on the ramp that is fed into the PWM comparator. Three other amplifiers are provided for the error amplifier side of the PWM comparator. This enables the combining of three control loops into one control signal into the PWM comparator. The power control application would need three control loops in order to provide the battery charge control algorithm. An analog majority voted control interface is provided for the application that has multiple power stages with a centralized control authority. This enables N+K fault tolerance on the power stages with single fault tolerance on the control authority. Each of the control amplifiers are auto zeroing or low offset in order to provide current control and sensing across low value sense resistors. The auto zero clock circuit provides the clock for the ping-pong amplifiers to cancel out the offset effects. A soft start function is provided to control the turn of the power converter and provide a controlled response to a fault. Initial startup or a fault can trigger slow ramp up of duty cycle.

The PWM logic provides the signals based on the output of the PWM comparator for the different topology options. Additional logic is provided for high power applications that require zero voltage transition (ZVT logic) with dead time controlled by external capacitors. The logic and interfaces are setup to cover the standard topologies for low and high power applications.

A signal isolation circuit is provided for the isolated power converters that need to send the control voltage back through a transformer isolated interface. This is configures by having a separate ASIC on the primary and one on the secondary side of the power converter. This circuit would modulate the analog signal across the transformer.

The auxiliary power on reset circuit (AUX POR) is provided to provide a POR signal for the end user of the output voltage. The end user can determine the threshold and hold time based on their application. This interface is usually a key point of conflict in negotiating the requirements between the end user and power converter designer.

The power MOSFET drivers (DRIVER 1-4) are selected via the routing logic (DRIVER SELECT) depending on the topology. Four drivers were selected to provide the capability for a full bridge topology. The drivers are designed to provide 1A peak current output at 12V. The drivers a ground referenced can directly drive ground referenced MOSFETs or can be used to drive the MOSFETs through a gate transformer.

In summary, the functional design of the ASIC is driven by providing the flexibility for different power levels and applications. The penalty for a flexible design is the number of pins required to program the functions and provide the degrees of freedom. The on chip MOSFET drivers are a challenge to available silicon space, but an option to move the drivers of chip and provide as a separate ASIC is a packaging trade still under investigation. There are strong arguments for both approaches.

V. Verification Approach

Based on our experience with the previous ASIC developments, we have developed an approach combining analysis with simulation to verify the functional design. The issues identified with the previous ASIC fabrications have come in the functional design. The library and functional elements have performed as predicted with the simulation models; however, the larger system level functions have had problems due to limited simulation capability.

We use a worst case database for each cell to perform worst case analysis to determine the steady state performance of the ASIC for the larger system level functions. We use focused simulation to verify the system interfaces, but a risk will always remain because of the lack of the capability to run a full chip simulations for all of the dynamic applications. A good system engineering approach needs to be taken within the architecture of the ASIC due to the limited verification capability. We use behavioral models for closed loop verification for many configurations, but the final verification will come during testing in the actual application.

Our experience in system level and board level design plays a key role in the layout of the ASIC and architecting the design. Many of the functions within the ASIC need to be decoupled as much as possible in order to reduce the risk due to the lack of simulation. Interfaces need to be verified independently with partial simulations to reduce the risk.

VI. Conclusion

The goals of the PWMA development are very challenging and in particular design for a severe environment as well as adding fault tolerant architectures. We have experience in designing for this environment and are providing as much functionality in one ASIC to apply to several applications. The development risks lies in the amount of functionality needed for a single ASIC and whether it is still competitive for the lower level applications.

Currently, the design has passed a preliminary design review in June, 2004. The worst case analysis is complete and the layout is in progress. The layout will determine what functionality remains on the ASIC or if it is decided to accomplish this function with a combination of ASICs. The existing density study shows very little margin. The capability of the drivers is a variable that can be reduced to provide more layout margin. A reduction in the capability of the driver and/or a separate driver ASIC may be the final implementation at the CDR, which is scheduled for January 2005.

Acknowledgments

This work was performed at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.