

Large CMOS Imager Using Hadamard Transform Based Multiplexing

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ABSTRACT

We have developed a concept design for a large ($\sim 10k \times 10k$) CMOS imaging array whose elements are grouped in small subarrays with N pixels in each. The subarrays are code-division multiplexed using the Hadamard Transform (HT) based encoding. The Hadamard code improves the signal-to-noise (SNR) ratio to the reference of the read-out amplifier by a factor of $N^{1/2}$. This way of grouping pixels reduces the number of hybridization bumps by N . A single chip layout has been designed and the architecture of the imager has been developed to accommodate the HT base multiplexing into the existing CMOS technology. The imager architecture allows for a trade-off between the speed and the sensitivity. The envisioned imager would operate at a speed >100 fps with the pixel noise $< 20 \epsilon$. The power dissipation would be ~ 100 pW/pixel. The combination of the large format, high speed, high sensitivity and low power dissipation can be very attractive for space reconnaissance applications.

Keywords: CMOS imager, Hadamard Transform, code-division multiplexing

1. INTRODUCTION

The most demanding space reconnaissance applications require very large format, fast operating, and sensitive imaging cameras. The major target figures of performance can be summarized into the following. The desired imager should have a format of at least $4k \times 4k$ pixels. This very large array should support a very high frame rate (at least 100 frames per second) while providing noise performance approaching that of photon noise limited performance. Additionally, the detector should have a quantum efficiency approaching 100% over the entire visible spectrum, and should be capable of internal electronic snapshot shuttering. Finally the imaging system should dissipate a low level of power and should operate at or near room temperature. Neither currently existing CCD, nor CMOS imagers can simultaneously provide all of the required operation features. Both these types of imagers have pros and cons. For example¹, CMOS imagers are superior to CCDs in responsivity and speed. Also, because of the possibility to directly address individual pixels via a transistor circuit integrated with the light sensor on the pixel, CMOS imagers are naturally capable of doing windowing. They generally have natural blooming immunity and generally operate with a single bias voltage and clock level (CCDs require a few high voltages). In its turn, CCDs have high dynamic range, better uniformity and better shuttering ability. A more detailed comparison of these imaging technologies is given below.

1.1 CCDs

CCDs have been in existence since the early 1970's and are detectors of choice for most high performance and scientific applications. Commercially available devices exist with array sizes of greater than $9k \times 9k$ pixels². High frame rates can be supported through the use of multiple (parallel) output ports on the same imager, which in effect break a large array into some number of smaller arrays, which can be readout simultaneously. Near 100% quantum efficiency can be obtained from CCDs by thinning the back surface of the array and illuminating from the backside. While CCDs have many excellent performance characteristics, they cannot support all of the customer needs. While CCDs can provide excellent quantum efficiency in a standard staring mode, problems arise with the additional requirement of electronic snapshot shuttering. For effective shuttering at high frame rates it is necessary to make use of interline transfer format CCDs. Interline transfer CCDs use a portion of each pixel as a photosite and the remainder of the pixel to support charge transfer from the array. The portion supporting transfer must be opaque to the incident light in order to perform shuttering. Hence, 100% quantum efficiency is not possible with this approach. Frame-transfer CCDs, devices, which

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use a secondary opaque storage region of equal size and shape to the imaging area for electronic shuttering, suffer from other problems. There is a finite time required to transfer the integrated image from the imaging area to the shielded storage area. To minimize image smear, this transfer time is typically less than 1% of the integration time. For large area arrays this 1% transfer time requirement requires that the CCD gates be clocked at very high rates. These high rates adversely affect the image quality through the reduction in charge transfer efficiency (image transfer smear) and require the use of extreme amounts of current (and hence power) to charge and discharge the CCD transfer gates. Furthermore, backside thinned and illuminated imagers typically cannot support the required large current pulses since the thinning process greatly increases the resistance of the ground plane of the CCD.

1.2 CMOS Imagers

CMOS imagers are a highly touted imaging technology, which came into the mainstream in the 1990's. As such in many ways they are still in their infancy. Typically CMOS imagers offer a lower level of performance than comparable resolution CCD imagers but several strong points such as inherent low power and device sub-circuit capabilities of the fabrication technology make it attractive in some applications. In principle, large area CMOS imaging arrays can be constructed through the use of photomask mosaicing. However, in practice, commercially available arrays tend to be limited to the $1k \times 1k$ pixel count. Very high frame rates can be supported through the use of multiple (parallel) output ports on the same imager, which in effect break a large array into some number of smaller arrays, which can be readout simultaneously.

One of the major drawbacks to CMOS imaging technology is that of overall detectivity. All CMOS pixels contain optically "dead" regions, which are related to active circuitry residing in the pixel and the metal interconnections required to access each pixel. Hence quantum efficiency can never be 100%. Furthermore, backside thinning and illumination, the process used to boost quantum efficiency in CCDs, cannot be easily used with CMOS imagers. Complementary elements of CMOS devices require a low resistance path to ground in order to eliminate "latch-up", a well understood phenomenon of CMOS technology which causes very large amounts of current to pass through devices in an uncontrolled manner. Latch-up can be fatal to CMOS devices. Finally electronic shuttering can be implemented in CMOS imagers, but doing so increases the optically dead region, thereby reducing the overall quantum efficiency. Some of the lost photons can be regained by using small lenses fabricated onto the top of each photosite. The microlenses focus the incoming light into the active photosite area. The gain in quantum efficiency can be significant but is typically wavelength dependent and non-uniform across the entire surface of the array.

1.3 CMOS/Photodiode Hybrids

Of the existing imager technologies, the CMOS/Photodiode hybrid comes closest to meeting the needs of the customer. A CMOS/Photodiode hybrid is an imager constructed of two independent pieces: a photodiode array for photon detection and a CMOS readout array that senses the captured signal and transfers it to the outside world for readout. The two individual components are hybridized by means of a grid of indium bumps, which provide electrical connection between them. Typically one indium bump is required for each pixel in the array. Hybrid arrays have been used for many years in infrared imaging but have only recently been evaluated for use in the visible spectrum. The approach provides many attractive performance features including high frame rate capability, low power operation and electronic snapshot shuttering. Through the choice of an appropriate diode structure and material it is possible to provide nearly 100% quantum efficiency over the visible wavelength range. Commercially available devices with snapshot capability support array sizes as large as $1k \times 1k$ pixels³.

While the CMOS/Photodiode hybrid approach has many attractive features, there are issues with the technology, which limit the maximum number of pixels in an array as well as the minimum size of those pixels. Since an indium bump is required for each pixel interconnection, the minimum pixel size is limited to that of the smallest repeatable indium bump. At present this requires the pixel to be at least 18 microns per side. While this may be reduced somewhat in the future, the indium bump will always represent a fundamental limit to the smallest possible pixel size and, hence indirectly, the highest optical resolution. Another problem presented by the use of indium bumps is that of assembly force. Each indium bump requires a minimum amount of force to properly form during the hybridization process. As the number of pixel in the array grows, so does the force required for assembly. For large arrays on the order of $2k \times 2k$ pixels, this force can exceed the capability of material to withstand. In short, adding more pixels results in breakage of the detector assembly. To bypass this limit it is possible to construct mosaics of individual detector arrays to increase the overall pixel count. However, seams will always exist at the mosaic interface, which may be problematic from an imaging perspective.

In this paper we introduce a novel approach to the CMOS imager architecture that has a potential for overcoming the many limitations which current state-of-the-art imager have. The main idea is to group signals from several (N) pixels of a CMOS array with +1 or -1 weights in certain algebraic combinations. The algorithm for sequences of +1's and -1's is given by the Hadamard Transform (HT). The procedure represents some kind of the code-division multiplexing (CDM). After N readings, N original signals are restored with a suppressed contribution of the readout amplifier by a factor of $N^{1/2}$. The proposed array architecture also reduces the number of hybridization indium bumps by N . In the following sections we describe the mathematical foundation for the novel CDM technique and the results of the design study and modeling for a large ($4k \times 4k$) HT multiplexed CMOS array.

2. HADAMARD TRANSFORM AND HADAMARD MULTIPLEXING

Hadamard Transform based techniques have been used for various scientific measurement applications for years and the mathematical theory is well established. Yates⁴ seems to have been the first to point out that by weighing several objects together instead of separately it may be possible to determine the individual weights more accurately. The idea is applicable to various types of measured quantities.

2.1 Hadamard matrices.

Suppose 4 quantities are to be measured using an instrument, which makes an error ϵ each time it is used. Assume that ϵ is a random variable with mean zero and variance σ^2 . First, suppose the objects are measured separately. If the unknown quantities are x_1, x_2, x_3, x_4 , the measurements are y_1, y_2, y_3, y_4 , and the errors are $\epsilon_1, \epsilon_2, \epsilon_3, \epsilon_4$, the four measurements give four equations:

$$y_i = x_i + \epsilon_i, \quad i=1..4 \quad (1)$$

The best estimates of the unknown quantities are the measurements themselves:

$$\hat{x}_i = y_i = x_i + \epsilon_i \quad (2)$$

Since we assume the expected value (or average value over a large number of experiments) of the error to be zero, $E\{\epsilon\}=0$, then $E\{\hat{x}\}=x$ and $E\{(\hat{x}-x)^2\}=E\{\epsilon^2\}=\sigma^2$.

For the second experiment, let's measure x_i in combinations:

$$\begin{aligned} y_1 &= x_1 + x_2 + x_3 + x_4 + \epsilon_1 \\ y_2 &= x_1 - x_2 + x_3 - x_4 + \epsilon_2 \\ y_3 &= x_1 + x_2 - x_3 - x_4 + \epsilon_3 \\ y_4 &= x_1 - x_2 - x_3 + x_4 + \epsilon_4 \end{aligned} \quad (3)$$

or in the matrix form $\mathbf{y} = \mathbf{W}\mathbf{x} + \boldsymbol{\epsilon}$.

The valid question to ask is: how should one choose the matrix \mathbf{W} ? If the number of measurements equals to the number of unknowns then \mathbf{W} should be invertible, that is $\hat{\mathbf{x}} = \mathbf{W}^{-1}\mathbf{y}$. The mean square error of the estimate of the i th unknown x_i is

$$\epsilon_i = E\{(\hat{x}_i - x_i)^2\} \quad (4)$$

Ideally one would like to minimize simultaneously all ϵ_i . The most important result is due to Hotelling⁵, who showed that for any choice of matrix \mathbf{W} with $|w_{ij}| \leq 1$, the ϵ_i are bounded by $\epsilon_i \geq (\sigma^2/N)$ ($N=4$ in our example), and that it is possible to have $\epsilon_i = (\sigma^2/N)$ for all $i=1..N$ if and only if a Hadamard matrix \mathbf{H}_N of order N exists (by taking $\mathbf{W} = \mathbf{H}_N$). In our example above the Hadamard matrix \mathbf{H}_4 of order 4 was used.

A Hadamard matrix of order N is an $N \times N$ matrix \mathbf{H}_N of +1's and -1's that satisfies $\mathbf{H}_N \mathbf{H}_N^T = N \cdot \mathbf{I}_N$, \mathbf{I}_N is the square unity matrix. These matrices are thought to exist if and only if $N=1,2$, or a multiple of 4. Numerous constructions are known and a plentiful supply of Hadamard matrices is available⁶. One simple construction which generates Hadamard matrices of orders 1, 2, 4, 8, 16, 32, ..., is the following:

$$\mathbf{H}_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \mathbf{H}_4 = \begin{bmatrix} \mathbf{H}_2 & \mathbf{H}_2 \\ \mathbf{H}_2 & -\mathbf{H}_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}, \dots, \mathbf{H}_N = \begin{bmatrix} \mathbf{H}_{N/2} & \mathbf{H}_{N/2} \\ \mathbf{H}_{N/2} & -\mathbf{H}_{N/2} \end{bmatrix}. \quad (5)$$

These are called Sylvester-type Hadamard matrices.

2.2 Hadamard Transform based multiplexing

The multiplexing algorithm based on the Hadamard Transform is, in general, rather simple. Indeed, if we want to multiplex N signal sources we need to encode them using a Hadamard matrix \mathbf{H}_N , to measure the algebraic sums of the signal N times and then to decode the original signal using the inverse Hadamard Transform. The noise undergoes a similar procedure except the squares of noise voltages are always added.

2.2.1 Recovery of the signals

Let \mathbf{Sig} be the vector whose elements correspond to the electrical signals generated in N pixels. Instead of reading all \mathbf{Sig} -elements one by one N times, the Hadamard multiplexer reads *algebraic combinations of all N signals N times*. The rule on should an individual signal be added or subtracted in a given reading event is set by the Hadamard matrix. Correspondingly, let \mathbf{Read} be the vector whose elements correspond to the algebraically summed outputs for each of the N reading events. Then \mathbf{Read} is the Hadamard Transform of \mathbf{Sig} :

$$\mathbf{Read} = \frac{1}{N} \mathbf{H}_N \cdot \mathbf{Sig} \quad (6)$$

For example, for a 4-element array,

$$\begin{aligned} \text{Read}_1 &= \text{Sig}_1 + \text{Sig}_2 + \text{Sig}_3 + \text{Sig}_4 \\ \text{Read}_2 &= \text{Sig}_1 - \text{Sig}_2 + \text{Sig}_3 - \text{Sig}_4 \\ \text{Read}_3 &= \text{Sig}_1 + \text{Sig}_2 - \text{Sig}_3 - \text{Sig}_4 \\ \text{Read}_4 &= \text{Sig}_1 - \text{Sig}_2 - \text{Sig}_3 + \text{Sig}_4 \end{aligned} \quad (7)$$

$$\begin{aligned} \text{Sig}_1 &= 1/4 \cdot (\text{Read}_1 + \text{Read}_2 + \text{Read}_3 + \text{Read}_4) \\ \text{Sig}_2 &= 1/4 \cdot (\text{Read}_1 - \text{Read}_2 + \text{Read}_3 - \text{Read}_4) \\ \text{Sig}_3 &= 1/4 \cdot (\text{Read}_1 + \text{Read}_2 - \text{Read}_3 - \text{Read}_4) \\ \text{Sig}_4 &= 1/4 \cdot (\text{Read}_1 - \text{Read}_2 - \text{Read}_3 + \text{Read}_4). \end{aligned} \quad (8)$$

The generation of the Hadamard matrices using instrumentation can be done differently depending on the type of detector elements. For multiplexing of elements in a CMOS array, a scheme of Fig. 1 can be used. It implies a connection of each photosensor to either plus- or minus-bus via two switches. The order of connection is given by the Hadamard code. At each bus, the signals from all sensors are added and, after that, a differential amplifier puts out a difference of plus and minus outputs.

2.2.2 Modification of the noise

Noise modification is important for multiplexed detector arrays. In the case of grouping elements (like the HT MUX does) a multiplexer folds noise from all detectors into one readout amplifier. So, depending on the dominating noise source, multiplexing speed and presence/absence of the output filters on the detector elements the de-multiplexed noise associated with a single pixel can be very different from that in the non-multiplexed case. Let's first consider the situation when the noise originates in pixels and the readout amplifier

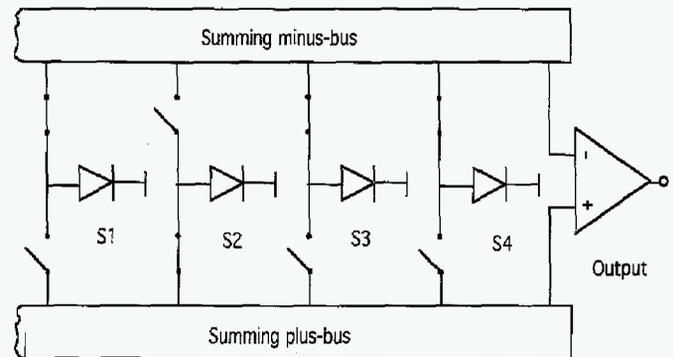


Fig. 1. Switch-encoded HT multiplexing scheme. Each pixel connects four times to either plus- or minus-bus to generate vector \mathbf{Read} of Eq. 6.

noise is negligibly small. We will consider three noise bands:

LF. This is the band with an upper cutoff frequency of $2/(N\tau)$, where τ is the single-measurement integration time. This low-frequency noise is unchanging during the course of the N measurements. The LF noise "cross-talk" does not represent a problem. The LF noise which is contributed by all $N-1$ detector elements to element j is completely removed by the Hadamard de-multiplexing. Indeed, a single measurement result would be:

$$Read_k = \sum_{j=1}^N h_{j,k} (Sig_j + LF_j). \quad (9)$$

Since LF_j , just like the signal Sig_j , does not change over the time scale of the measurements the inverse Hadamard Transform fully recovers $Sig_j + LF_j$.

MF. This is the medium-frequency range where the noise of each detector element remains nearly constant during the single-measurement integration time τ but varies during the time for N single-measurements. During a single-measurement integration time, the MF noise voltages are statistically independent from detector element to detector element. For each detector element the MF noise voltage varies slightly from single-measurement to single-measurement. Thus, MF noise of successive single-measurements has a high degree of correlation. The degree of correlation decreases between single-measurements as they are more widely separated in time. MF noises of measurements 1 and N are completely uncorrelated. Let index i identify the detector elements when they are read out in series and index j identify the single-measurements of series (summed) signals + noises. $MF_{i,j}$ is the ensemble of noise values that contributes to the entire Hadamard measurement scheme. The Hadamard extraction process sums over all these values: $Sig_k = \frac{1}{N} \sum_{j=1}^N \sum_{i=1}^N h_{k,i} h_{i,j} MF_{i,j}$. The sum over i adds N uncorrelated numbers that results in N numbers that are

weakly correlated. A careful rigorous analysis of the degradation to SNR caused by MF noise was not possible at this time. It is, however, unlikely that the Hadamard-extracted single-element SNR may be somewhat degraded by a yet to be determined quantity of time-correlated noise compared to the previous cases.

HF. This is the high-frequency band where the noise varies substantially during a single-measurement integration time. If the HF noise "cross-talk" is present the noise for each detector element changes completely and randomly from single-measurement to single-measurement. The HF rms noise voltage on a single measurement $Read_k$ is $N^{1/2}$ times that on a single detector element. But the N readings reduce this noise by $N^{1/2}$ so once again the HT de-multiplexing process returns the individual signal values plus an HF noise component equal to that of a single measurement of an isolated detector element. Depending on the nature of the array, the HF noise can be dealt with using low-pass filters (LPF) at each element. The white noise in the pixel above the filter cutoff will not cross-contaminate the signals.

Now let's consider the noise modification when the amplifier noise dominates. The LF noise, which is not different from the signal, recovers completely and, thus, the SNR, remains unchanged. The HF noise of the amplifier adds just once per each reading event, that is

$$Read_k = \sum_{j=1}^N h_{j,k} Sig_j + HF_{amp}. \quad (10)$$

After the HT, its rms value reduces by $N^{1/2}$. Indeed, during the inverse HT we have to algebraically add $Read_k$ (the noises add as squares) and then to divide the result by N . Therefore, the SNR increases by $N^{1/2}$. This is a great improvement of the performance. For very large N , this creates a large room for trading off the sensitivity increase vs the multiplexing speed.

3. HADAMARD TRANSFORM HYBRID IMAGING TECHNOLOGY (HT-HIT)

This is the approach proposed in this work. The HT-HIT overcomes all of the performance issues described in the Section 1. An HT-HIT array is a hybrid, which uses HT multiplexing of groups of pixels on the imaging chip. A

significant advantage is that this requires just two indium bumps per group, not per pixel. It reduces the bonding force and the bump capacitance and allows for a larger array.

The imaging array was assumed to be fabricated using "standard" 0.8 μm CMOS process with a 150 \AA oxide thickness, 1 level of polysilicon and 3 levels of metal interconnection, stacked contact and via technology. The hybridized CMOS Signal Processor uses "standard" 0.35 μm CMOS process, 70 \AA oxide thickness, 2 levels of polysilicon, 4 levels of metal interconnection, and stacked contact and via technology. The simulations were performed using a combination of Tanner Software T-Spice and a proprietary software program by Tangent Technologies..

The pixel layout is shown in Fig. 2. From the point of view of electrical schematics, it follows the circuit of Fig. 1. The integration of pixels into a group of 16 is shown in Fig. 3. The group uses just two indium bumps to connect to the CMOS processor chip. Figure 4 shows the organization of the corresponding circuitry on the signal processor chip.

Based on this topological solution, the following "strawman detector" concept has been evaluated:

- 4096 \times 4096 Pixels
- Frame Rate = 100 fps
- Shuttering Time = 100 μs (1% of integration)
- $N=16$ (16 Pixels per HT Group)
- Pixel Size = 10 μm \times 10 μm
- Use one sampling capacitor per pixel for "snap-shot" imaging ($C_{\text{sampling}} = 500 \text{ fF}$)
- Total Number of Hybrid Bumps = 2.1×10^6
- Group N Pixel Sections into Groups of 64 Subsections
- Place 1 ADC for Each 64 Element Subsection
- Use additional multiplexing to reduce number of outputs
- The differential amplifier noise is $25 \text{ nV/Hz}^{1/2}$
- The ambient temperature $T=300\text{K}$

With these parameters the capacitance of the pixel is 50 fF and the Pixel Full Well = 20,000-30,000 e^- . The pixel noise reduces by a factor of 4 to $\sim 15 e^-$ in comparison with the design not using the HT. This corresponds to the dynamic range >1500 .

The power balance of the imager is the following:

Pixel Clocking	72 mW
HT Analog	84 mW
Peripheral Analog	1089 mW
HT Digital	2 mW
ADC	350 mW
Total Estimated Power	1.6 W

This is 25 times less than the expected dissipation in a CCD imager with similar performance figures.

The actual performance limitations of the HT-HIT approach will be determined by the processing technology used for device fabrication. Specifically, process factors, which affect low frequency noise, maximum current capacity per unit area of transistors and density of metal interconnects will have major impacts upon the performance of the imager.

The maximum pixel count of the HT-HIT imager is controlled by the same issue that limits the size of CMOS/Photodiode hybrids - maximum hybridization force. However, since the HT-HIT approach requires fewer indium bumps for a given pixel count than a CMOS/Photodiode hybrid,

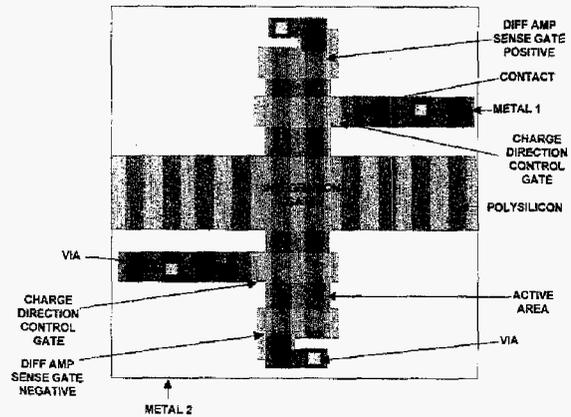


Fig. 2. The layout of a CMOS imaging pixel with the control gates for HT multiplexing.

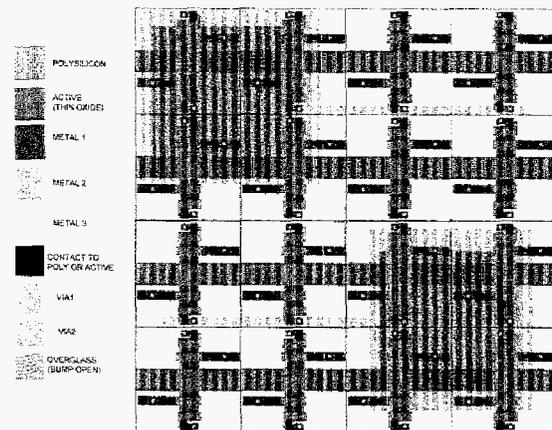


Fig. 3. A 16-pixel HT group. The topology of the design allows for the HT multiplexing using switching gates. The multiplexed signals are read by a differential amplifier on a separate chip connected via indium bumps.

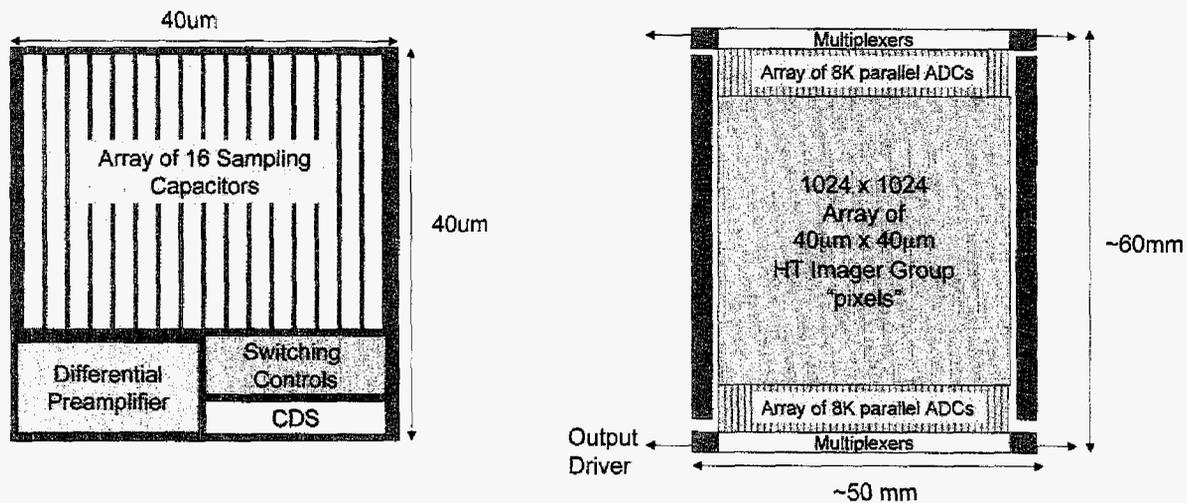


Fig. 4. The architecture of the CMOS signal processor. Left panel: the CMOS signal Imager Group contains a $40\ \mu\text{m} \times 40\ \mu\text{m}$ array of sampling capacitors, which matches to the 16-pixel HT group of Fig. 3, a differential amplifier, switching controls and a Correlated Double Sampling (CDS) circuit. Right panel: the CMOS Signal Imager Processor integrates ~ 1.05 million of HT groups with peripheral circuitry in the $5\ \text{cm} \times 6\ \text{cm}$ area.

HT-HIT can support arrays with larger pixels. Furthermore, as connections are not required for individual pixels, the minimum pixel size is not controlled by the minimum indium bump size. Based on the results of this study the HT-HIT approach can support arrays of greater than $10\text{k} \times 10\text{k}$ pixels with pixel sizes on the order of $10\ \mu\text{m} \times 10\ \mu\text{m}$.

4. CONCLUSIONS

We have proposed a new multiplexing techniques for CMOS arrays based on the Hadamard Transform encoding of the pixels. The HT MUX offers an almost 100% duty cycle and, as a result, a $N^{1/2}$ SNR improvement when the readout amplifier is the main source of noise.

A $4\text{k} \times 4\text{k}$ HT-HIT detector has been designed and evaluated. The HT-HIT approach supports

- frame rates of 100 fps or greater
- inherent internal snap-shot shuttering
- read noise of less than $20\ e^-$ (rms)
- dynamic range greater than 10 bits
- power of less than $100\ \text{nW}/\text{pixel}$ at 100 fps operating rate

HT-HIT is well suited for larger format devices since i) very large imagers will make use of larger N values ii) larger N values reduce the number of hybrid bumps.

The new approach promises to improve state-of-the art for visible range imagers. In particular, the HT-HIT approach has the following advantages over the existing imagers:

- In comparison with the best CCD imagers, the HT-HIT approach allows for similarly large array formats $\sim 10\text{k} \times 10\text{k}$ but with more than an order of magnitude less dissipated power and better shuttering capabilities;
- In comparison with the CMOS imagers, the HT-HIT approach allows for much larger array formats due to reduced number of hybridization indium bumps and it also reduces the pixel noise by a factor of $N^{1/2}$.

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REFERENCES

1. D. Litwiller, *Photonics Spectra*, JAN 2001; *ibid* **36** (1), pp. 102-103, JAN 2002.
2. http://www.fairchildimaging.com/main/prod_fpa_ccd_area.htm
3. http://www.rockwellscientific.com/imaging/ROIC_Ref_Table.html
4. F. Yates, *J.R. Stat.Soc. Suppl.* **2**, 181 (1935).
5. H. Hotelling, *Ann. Math. Stat.* **15**, 297 (1944).
6. W.D. Wallis, A.P. Street, and J.S. Wallis, *Combinatorics: Room Squares, Sum-Free Sets, Hadamard Matrices, Lecture Notes in Mathematics* **292**, New York: Springer-Verlag (1972); M. Hall, Jr., *Combinatorial Theory*, Waltham, Mass: Blaisdell (1967); R.J. Turyn, *J. Combinatorial Theory* **16A**, pp. 313-333 (1974).

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1. INTRODUCTION

The most demanding space reconnaissance applications require very large format, fast operating, and sensitive imaging cameras. The major target figures of performance can be summarized into the following. The desired imager should have a format of at least $4k \times 4k$ pixels. This very large array should support a very high frame rate (at least 100 frames per second) while providing noise performance approaching that of photon noise limited performance. Additionally, the detector should have a quantum efficiency approaching 100% over the entire visible spectrum, and should be capable of internal electronic snapshot shuttering. Finally the imaging system should dissipate a low level of power and should operate at or near room temperature. Neither currently existing CCD, nor CMOS imagers can simultaneously provide all of the required operation features. Both these types of imagers have pros and cons. For example¹, CMOS imagers are superior to CCDs in responsivity and speed. Also, because of the possibility to directly address individual pixels via a transistor circuit integrated with the light sensor on the pixel, CMOS imagers are naturally capable of doing windowing. They generally have natural blooming immunity and generally operate with a single bias voltage and clock level (CCDs require a few high voltages). In its turn, CCDs have high dynamic range, better uniformity and better shuttering ability. A more detailed comparison of these imaging technologies is given below.

1.1 CCDs

CCDs have been in existence since the early 1970's and are detectors of choice for most high performance and scientific applications. Commercially available devices exist with array sizes of greater than $9k \times 9k$ pixels². High frame rates can be supported through the use of multiple (parallel) output ports on the same imager, which in effect break a large array into some number of smaller arrays, which can be readout simultaneously. Near 100% quantum efficiency can be obtained from CCDs by thinning the back surface of the array and illuminating from the backside. While CCDs have many excellent performance characteristics, they cannot support all of the customer needs. While CCDs can provide excellent quantum efficiency in a standard staring mode, problems arise with the additional requirement of electronic snapshot shuttering. For effective shuttering at high frame rates it is necessary to make use of interline transfer format CCDs. Interline transfer CCDs use a portion of each pixel as a photosite and the remainder of the pixel to support charge transfer from the array. The portion supporting transfer must be opaque to the incident light in order to perform shuttering. Hence, 100% quantum efficiency is not possible with this approach. Frame-transfer CCDs, devices, which

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use a secondary opaque storage region of equal size and shape to the imaging area for electronic shuttering, suffer from other problems. There is a finite time required to transfer the integrated image from the imaging area to the shielded storage area. To minimize image smear, this transfer time is typically less than 1% of the integration time. For large area arrays this 1% transfer time requirement requires that the CCD gates be clocked at very high rates. These high rates adversely affect the image quality through the reduction in charge transfer efficiency (image transfer smear) and require the use of extreme amounts of current (and hence power) to charge and discharge the CCD transfer gates. Furthermore, backside thinned and illuminated imagers typically cannot support the required large current pulses since the thinning process greatly increases the resistance of the ground plane of the CCD.

1.2 CMOS Imagers

CMOS imagers are a highly touted imaging technology, which came into the mainstream in the 1990's. As such in many ways they are still in their infancy. Typically CMOS imagers offer a lower level of performance than comparable resolution CCD imagers but several strong points such as inherent low power and device sub-circuit capabilities of the fabrication technology make it attractive in some applications. In principle, large area CMOS imaging arrays can be constructed through the use of photomask mosaicing. However, in practice, commercially available arrays tend to be limited to the $1k \times 1k$ pixel count. Very high frame rates can be supported through the use of multiple (parallel) output ports on the same imager, which in effect break a large array into some number of smaller arrays, which can be readout simultaneously.

One of the major drawbacks to CMOS imaging technology is that of overall detectivity. All CMOS pixels contain optically "dead" regions, which are related to active circuitry residing in the pixel and the metal interconnections required to access each pixel. Hence quantum efficiency can never be 100%. Furthermore, backside thinning and illumination, the process used to boost quantum efficiency in CCDs, cannot be easily used with CMOS imagers. Complementary elements of CMOS devices require a low resistance path to ground in order to eliminate "latch-up", a well understood phenomenon of CMOS technology which causes very large amounts of current to pass through devices in an uncontrolled manner. Latch-up can be fatal to CMOS devices. Finally electronic shuttering can be implemented in CMOS imagers, but doing so increases the optically dead region, thereby reducing the overall quantum efficiency. Some of the lost photons can be regained by using small lenses fabricated onto the top of each photosite. The microlenses focus the incoming light into the active photosite area. The gain in quantum efficiency can be significant but is typically wavelength dependent and non-uniform across the entire surface of the array.

1.3 CMOS/Photodiode Hybrids

Of the existing imager technologies, the CMOS/Photodiode hybrid comes closest to meeting the needs of the customer. A CMOS/Photodiode hybrid is an imager constructed of two independent pieces: a photodiode array for photon detection and a CMOS readout array that senses the captured signal and transfers it to the outside world for readout. The two individual components are hybridized by means of a grid of indium bumps, which provide electrical connection between them. Typically one indium bump is required for each pixel in the array. Hybrid arrays have been used for many years in infrared imaging but have only recently been evaluated for use in the visible spectrum. The approach provides many attractive performance features including high frame rate capability, low power operation and electronic snapshot shuttering. Through the choice of an appropriate diode structure and material it is possible to provide nearly 100% quantum efficiency over the visible wavelength range. Commercially available devices with snapshot capability support array sizes as large as $1k \times 1k$ pixels³.

While the CMOS/Photodiode hybrid approach has many attractive features, there are issues with the technology, which limit the maximum number of pixels in an array as well as the minimum size of those pixels. Since an indium bump is required for each pixel interconnection, the minimum pixel size is limited to that of the smallest repeatable indium bump. At present this requires the pixel to be at least 18 microns per side. While this may be reduced somewhat in the future, the indium bump will always represent a fundamental limit to the smallest possible pixel size and, hence indirectly, the highest optical resolution. Another problem presented by the use of indium bumps is that of assembly force. Each indium bump requires a minimum amount of force to properly form during the hybridization process. As the number of pixel in the array grows, so does the force required for assembly. For large arrays on the order of $2k \times 2k$ pixels, this force can exceed the capability of material to withstand. In short, adding more pixels results in breakage of the detector assembly. To bypass this limit it is possible to construct mosaics of individual detector arrays to increase the overall pixel count. However, seams will always exist at the mosaic interface, which may be problematic from an imaging perspective.

In this paper we introduce a novel approach to the CMOS imager architecture that has a potential for overcoming the many limitations which current state-of-the-art imager have. The main idea is to group signals from several (N) pixels of a CMOS array with +1 or -1 weights in certain algebraic combinations. The algorithm for sequences of +1's and -1's is given by the Hadamard Transform (HT). The procedure represents some kind of the code-division multiplexing (CDM). After N readings, N original signals are restored with a suppressed contribution of the readout amplifier by a factor of $N^{1/2}$. The proposed array architecture also reduces the number of hybridization indium bumps by N . In the following sections we describe the mathematical foundation for the novel CDM technique and the results of the design study and modeling for a large ($4k \times 4k$) HT multiplexed CMOS array.

2. HADAMARD TRANSFORM AND HADAMARD MULTIPLEXING

Hadamard Transform based techniques have been used for various scientific measurement applications for years and the mathematical theory is well established. Yates⁴ seems to have been the first to point out that by weighing several objects together instead of separately it may be possible to determine the individual weights more accurately. The idea is applicable to various types of measured quantities.

2.1 Hadamard matrices.

Suppose 4 quantities are to be measured using an instrument, which makes an error ϵ each time it is used. Assume that ϵ is a random variable with mean zero and variance σ^2 . First, suppose the objects are measured separately. If the unknown quantities are x_1, x_2, x_3, x_4 , the measurements are y_1, y_2, y_3, y_4 , and the errors are $\epsilon_1, \epsilon_2, \epsilon_3, \epsilon_4$, the four measurements give four equations:

$$y_i = x_i + \epsilon_i, i=1..4 \quad (1)$$

The best estimates of the unknown quantities are the measurements themselves:

$$\hat{x}_i = y_i = x_i + \epsilon_i \quad (2)$$

Since we assume the expected value (or average value over a large number of experiments) of the error to be zero, $E\{\epsilon\} = 0$, then $E\{\hat{x}\} = x$ and $E\{(\hat{x} - x)^2\} = E\{\epsilon^2\} = \sigma^2$.

For the second experiment, let's measure x_i in combinations:

$$\begin{aligned} y_1 &= x_1 + x_2 + x_3 + x_4 + \epsilon_1 \\ y_2 &= x_1 - x_2 + x_3 - x_4 + \epsilon_2 \\ y_3 &= x_1 + x_2 - x_3 - x_4 + \epsilon_3 \\ y_4 &= x_1 - x_2 - x_3 + x_4 + \epsilon_4 \end{aligned} \quad (3)$$

or in the matrix form $\mathbf{y} = \mathbf{W}\mathbf{x} + \boldsymbol{\epsilon}$.

The valid question to ask is: how should one choose the matrix \mathbf{W} ? If the number of measurements equals to the number of unknowns then \mathbf{W} should be invertible, that is $\hat{\mathbf{x}} = \mathbf{W}^{-1}\mathbf{y}$. The mean square error of the estimate of the i th unknown x_i is

$$\epsilon_i = E\{(\hat{x}_i - x_i)^2\} \quad (4)$$

Ideally one would like to minimize simultaneously all ϵ_i . The most important result is due to Hotelling⁵, who showed that for any choice of matrix \mathbf{W} with $|w_{ij}| \leq 1$, the ϵ_i are bounded by $\epsilon_i \geq (\sigma^2/N)$ ($N=4$ in our example), and that it is possible to have $\epsilon_i = (\sigma^2/N)$ for all $i=1..N$ if and only if a Hadamard matrix \mathbf{H}_N of order N exists (by taking $\mathbf{W} = \mathbf{H}_N$). In our example above the Hadamard matrix \mathbf{H}_4 of order 4 was used.

A Hadamard matrix of order N is an $N \times N$ matrix \mathbf{H}_N of +1's and -1's that satisfies $\mathbf{H}_N \mathbf{H}_N^T = N \cdot \mathbf{I}_N$, \mathbf{I}_N is the square unity matrix. These matrices are thought to exist if and only if $N=1, 2$, or a multiple of 4. Numerous constructions are known and a plentiful supply of Hadamard matrices is available⁶. One simple construction which generates Hadamard matrices of orders 1, 2, 4, 8, 16, 32, ..., is the following:

$$\mathbf{H}_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \mathbf{H}_4 = \begin{bmatrix} \mathbf{H}_2 & \mathbf{H}_2 \\ \mathbf{H}_2 & -\mathbf{H}_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}, \dots, \mathbf{H}_N = \begin{bmatrix} \mathbf{H}_{N/2} & \mathbf{H}_{N/2} \\ \mathbf{H}_{N/2} & -\mathbf{H}_{N/2} \end{bmatrix}. \quad (5)$$

These are called Sylvester-type Hadamard matrices.

2.2 Hadamard Transform based multiplexing

The multiplexing algorithm based on the Hadamard Transform is, in general, rather simple. Indeed, if we want to multiplex N signal sources we need to encode them using a Hadamard matrix \mathbf{H}_N , to measure the algebraic sums of the signal N times and then to decode the original signal using the inverse Hadamard Transform. The noise undergoes a similar procedure except the squares of noise voltages are always added.

2.2.1 Recovery of the signals

Let **Sig** be the vector whose elements correspond to the electrical signals generated in N pixels. Instead of reading all **Sig**-elements one by one N times, the Hadamard multiplexer reads *algebraic combinations of all N signals N times*. The rule on should an individual signal be added or subtracted in a given reading event is set by the Hadamard matrix. Correspondingly, let **Read** be the vector whose elements correspond to the algebraically summed outputs for each of the N reading events. Then **Read** is the Hadamard Transform of **Sig**:

$$\mathbf{Read} = \frac{1}{N} \mathbf{H}_N \cdot \mathbf{Sig} \quad (6)$$

For example, for a 4-element array,

$$\begin{aligned} \text{Read}_1 &= \text{Sig}_1 + \text{Sig}_2 + \text{Sig}_3 + \text{Sig}_4 \\ \text{Read}_2 &= \text{Sig}_1 - \text{Sig}_2 + \text{Sig}_3 - \text{Sig}_4 \\ \text{Read}_3 &= \text{Sig}_1 + \text{Sig}_2 - \text{Sig}_3 - \text{Sig}_4 \\ \text{Read}_4 &= \text{Sig}_1 - \text{Sig}_2 - \text{Sig}_3 + \text{Sig}_4 \end{aligned} \quad (7)$$

$$\begin{aligned} \text{Sig}_1 &= 1/4 \cdot (\text{Read}_1 + \text{Read}_2 + \text{Read}_3 + \text{Read}_4) \\ \text{Sig}_2 &= 1/4 \cdot (\text{Read}_1 - \text{Read}_2 + \text{Read}_3 - \text{Read}_4) \\ \text{Sig}_3 &= 1/4 \cdot (\text{Read}_1 + \text{Read}_2 - \text{Read}_3 - \text{Read}_4) \\ \text{Sig}_4 &= 1/4 \cdot (\text{Read}_1 - \text{Read}_2 - \text{Read}_3 + \text{Read}_4). \end{aligned} \quad (8)$$

The generation of the Hadamard matrices using instrumentation can be done differently depending on the type of detector elements. For multiplexing of elements in a CMOS array, a scheme of Fig. 1 can be used. It implies a connection of each photosensor to either plus- or minus-bus via two switches. The order of connection is given by the Hadamard code. At each bus, the signals from all sensors are added and, after that, a differential amplifier puts out a difference of plus and minus outputs.

2.2.2 Modification of the noise

Noise modification is important for multiplexed detector arrays. In the case of grouping elements (like the HT MUX does) a multiplexer folds noise from all detectors into one readout amplifier. So, depending on the dominating noise source, multiplexing speed and presence/absence of the output filters on the detector elements the de-multiplexed noise associated with a single pixel can be very different from that in the non-multiplexed case. Let's first consider the situation when the noise originates in pixels and the readout amplifier

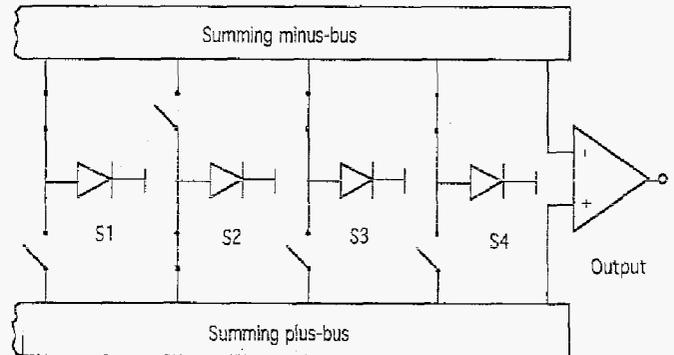


Fig. 1. Switch-encoded HT multiplexing scheme. Each pixel connects four times to either plus- or minus-bus to generate vector **Read** of Eq. 6.

noise is negligibly small. We will consider three noise bands:

LF. This is the band with an upper cutoff frequency of $2/(N\tau)$, where τ is the single-measurement integration time. This low-frequency noise is unchanging during the course of the N measurements. The LF noise "cross-talk" does not represent a problem. The LF noise which is contributed by all $N-1$ detector elements to element j is completely removed by the Hadamard de-multiplexing. Indeed, a single measurement result would be:

$$Read_k = \sum_{j=1}^N h_{j,k} (Sig_j + LF_j). \quad (9)$$

Since LF_j , just like the signal Sig_j , does not change over the time scale of the measurements the inverse Hadamard Transform fully recovers $Sig_j + LF_j$.

MF. This is the medium-frequency range where the noise of each detector element remains nearly constant during the single-measurement integration time τ but varies during the time for N single-measurements. During a single-measurement integration time, the MF noise voltages are statistically independent from detector element to detector element. For each detector element the MF noise voltage varies slightly from single-measurement to single-measurement. Thus, MF noise of successive single-measurements has a high degree of correlation. The degree of correlation decreases between single-measurements as they are more widely separated in time. MF noises of measurements 1 and N are completely uncorrelated. Let index i identify the detector elements when they are read out in series and index j identify the single-measurements of series (summed) signals + noises. $MF_{i,j}$ is the ensemble of noise values that contributes to the entire Hadamard measurement scheme. The Hadamard extraction process sums over all these values: $Sig_k = \frac{1}{N} \sum_{j=1}^N \sum_{i=1}^N h_{k,i} h_{i,j} MF_{i,j}$. The sum over i adds N uncorrelated numbers that results in N numbers that are weakly correlated. A careful rigorous analysis of the degradation to SNR caused by MF noise was not possible at this time. It is, however, unlikely that the Hadamard-extracted single-element SNR may be somewhat degraded by a yet to be determined quantity of time-correlated noise compared to the previous cases.

HF. This is the high-frequency band where the noise varies substantially during a single-measurement integration time. If the HF noise "cross-talk" is present the noise for each detector element changes completely and randomly from single-measurement to single-measurement. The HF rms noise voltage on a single measurement $Read_k$ is $N^{1/2}$ times that on a single detector element. But the N readings reduce this noise by $N^{1/2}$ so once again the HT de-multiplexing process returns the individual signal values plus an HF noise component equal to that of a single measurement of an isolated detector element. Depending of the nature of the array, the HF noise can be dealt with using low-pass filters (LPF) at each element. The white noise in the pixel above the filter cutoff will not cross-contaminate the signals.

Now let's consider the noise modification when the amplifier noise dominates. The LF noise, which is not different from the signal, recovers completely and, thus, the SNR, remains unchanged. The HF noise of the amplifier adds just once per each reading event, that is

$$Read_k = \sum_{j=1}^N h_{j,k} Sig_j + HF_{amp}. \quad (10)$$

After the HT, its rms value reduces by $N^{1/2}$. Indeed, during the inverse HT we have to algebraically add $Read_k$ (the noises add as squares) and then to divide the result by N . Therefore, the SNR increases by $N^{1/2}$. This is a great improvement of the performance. For very large N , this creates a large room for trading off the sensitivity increase vs the multiplexing speed.

3. HADAMARD TRANSFORM HYBRID IMAGING TECHNOLOGY (HT-HIT)

This is the approach proposed in this work. The HT-HIT overcomes all of the performance issues described in the Section 1. An HT-HIT array is a hybrid, which uses HT multiplexing of groups of pixels on the imaging chip. A

significant advantage is that this requires just two indium bumps per group, not per pixel. It reduces the bonding force and the bump capacitance and allows for a larger array.

The imaging array was assumed to be fabricated using "standard" 0.8 μm CMOS process with a 150 \AA oxide thickness, 1 level of polysilicon and 3 levels of metal interconnection, stacked contact and via technology. The hybridized CMOS Signal Processor uses "standard" 0.35 μm CMOS process, 70 \AA oxide thickness, 2 levels of polysilicon, 4 levels of metal interconnection, and stacked contact and via technology. The simulations were performed using a combination of Tanner Software T-Spice and a proprietary software program by Tangent Technologies..

The pixel layout is shown in Fig. 2. From the point of view of electrical schematics, it follows the circuit of Fig. 1. The integration of pixels into a group of 16 is shown in Fig. 3. The group uses just two indium bumps to connect to the CMOS processor chip. Figure 4 shows the organization of the corresponding circuitry on the signal processor chip.

Based on this topological solution, the following "strawman detector" concept has been evaluated:

- 4096 \times 4096 Pixels
- Frame Rate = 100 fps
- Shuttering Time = 100 μs (1% of integration)
- $N=16$ (16 Pixels per HT Group)
- Pixel Size = 10 $\mu\text{m} \times 10 \mu\text{m}$
- Use one sampling capacitor per pixel for "snap-shot" imaging ($C_{\text{sampling}} = 500 \text{ fF}$)
- Total Number of Hybrid Bumps = 2.1×10^6
- Group N Pixel Sections into Groups of 64 Subsections
- Place 1 ADC for Each 64 Element Subsection
- Use additional multiplexing to reduce number of outputs
- The differential amplifier noise is $25 \text{ nV/Hz}^{1/2}$
- The ambient temperature $T=300\text{K}$

With these parameters the capacitance of the pixel is 50 fF and the Pixel Full Well = 20,000-30,000 e^- . The pixel noise reduces by a factor of 4 to $\sim 15 e^-$ in comparison with the design not using the HT. This corresponds to the dynamic range >1500 .

The power balance of the imager is the following:

Pixel Clocking	72 mW
HT Analog	84 mW
Peripheral Analog	1089 mW
HT Digital	2 mW
ADC	350 mW
Total Estimated Power	1.6 W

This is 25 times less than the expected dissipation in a CCD imager with similar performance figures.

The actual performance limitations of the HT-HIT approach will be determined by the processing technology used for device fabrication. Specifically, process factors, which affect low frequency noise, maximum current capacity per unit area of transistors and density of metal interconnects will have major impacts upon the performance of the imager.

The maximum pixel count of the HT-HIT imager is controlled by the same issue that limits the size of CMOS/Photodiode hybrids - maximum hybridization force. However, since the HT-HIT approach requires fewer indium bumps for a given pixel count than a CMOS/Photodiode hybrid,

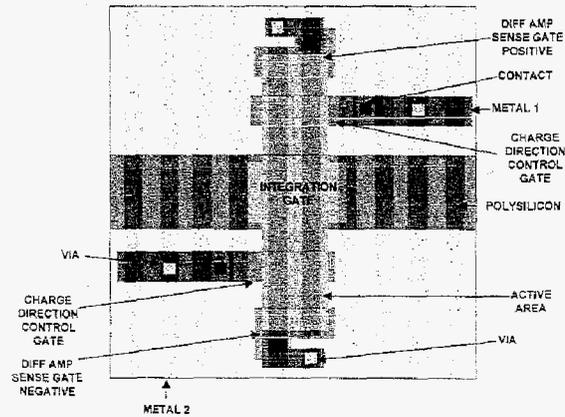


Fig. 2. The layout of a CMOS imaging pixel with the control gates for HT multiplexing.

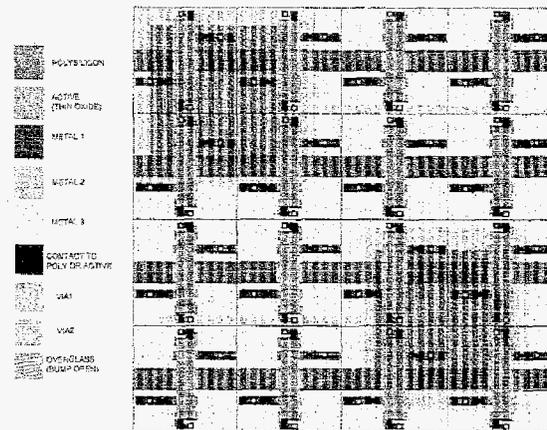


Fig. 3. A 16-pixel HT group. The topology of the design allows for the HT multiplexing using switching gates. The multiplexed signals are read by a differential amplifier on a separate chip connected via indium bumps.

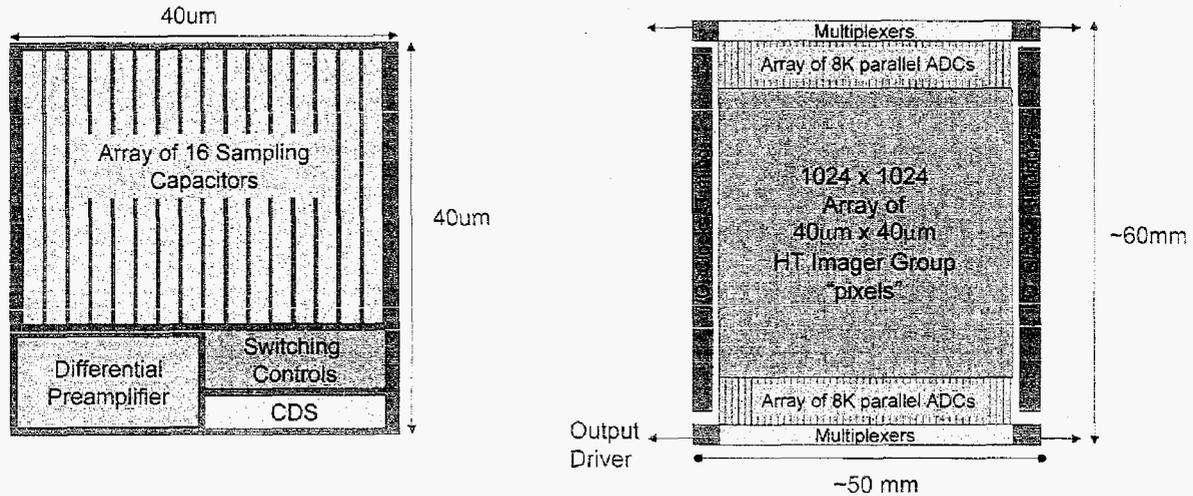


Fig. 4. The architecture of the CMOS signal processor. Left panel: the CMOS signal Imager Group contains a $40\ \mu\text{m} \times 40\ \mu\text{m}$ array of sampling capacitors, which matches to the 16-pixel HT group of Fig. 3, a differential amplifier, switching controls and a Correlated Double Sampling (CDS) circuit. Right panel: the CMOS Signal Imager Processor integrates ~ 1.05 million of HT groups with peripheral circuitry in the $5\ \text{cm} \times 6\ \text{cm}$ area.

HT-HIT can support arrays with larger pixels. Furthermore, as connections are not required for individual pixels, the minimum pixel size is not controlled by the minimum indium bump size. Based on the results of this study the HT-HIT approach can support arrays of greater than $10\text{k} \times 10\text{k}$ pixels with pixel sizes on the order of $10\ \mu\text{m} \times 10\ \mu\text{m}$.

4. CONCLUSIONS

We have proposed a new multiplexing techniques for CMOS arrays based on the Hadamard Transform encoding of the pixels. The HT MUX offers an almost 100% duty cycle and, as a result, a $N^{1/2}$ SNR improvement when the readout amplifier is the main source of noise.

A $4\text{k} \times 4\text{k}$ HT-HIT detector has been designed and evaluated. The HT-HIT approach supports

- frame rates of 100 fps or greater
- inherent internal snap-shot shuttering
- read noise of less than $20\ e^-$ (rms)
- dynamic range greater than 10 bits
- power of less than $100\ \text{nW}/\text{pixel}$ at 100 fps operating rate

HT-HIT is well suited for larger format devices since i) very large imagers will make use of larger N values ii) larger N values reduce the number of hybrid bumps.

The new approach promises to improve state-of-the art for visible range imagers. In particular, the HT-HIT approach has the following advantages over the existing imagers:

- In comparison with the best CCD imagers, the HT-HIT approach allows for similarly large array formats $\sim 10\text{k} \times 10\text{k}$ but with more than an order of magnitude less dissipated power and better shuttering capabilities;
- In comparison with the CMOS imagers, the HT-HIT approach allows for much larger array formats due to reduced number of hybridization indium bumps and it also reduces the pixel noise by a factor of $N^{1/2}$.

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REFERENCES

1. D. Litwiller, *Photonics Spectra*, JAN 2001; *ibid* **36** (1), pp. 102-103, JAN 2002.
2. http://www.fairchildimaging.com/main/prod_fpa_ccd_area.htm
3. http://www.rockwellscientific.com/imaging/ROIC_Ref_Table.html
4. F. Yates, *J.R. Stat.Soc. Suppl.* **2**, 181 (1935).
5. H. Hotelling, *Ann. Math. Stat.* **15**, 297 (1944).
6. W.D. Wallis, A.P. Street, and J.S. Wallis, *Combinatorics: Room Squares, Sum-Free Sets, Hadamard Matrices, Lecture Notes in Mathematics* **292**, New York: Springer-Verlag (1972); M. Hall, Jr., *Combinatorial Theory*, Waltham, Mass: Blaisdell (1967); R.J. Turyn, *J. Combinatorial Theory* **16A**, pp. 313-333 (1974).