# T-SHAPED EMITTER METAL HETEROJUNCTION BIPOLAR TRANSISTORS FOR SUBMILLIMETER WAVE APPLICATIONS

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**Abstract**

We report on the development of submillimeter wave transistors at JPL. The goal of the effort is to produce advance-reliable high frequency and high power amplifiers, voltage controlled oscillators, active multipliers, and high-speed mixed-signal circuits for space borne applications. The technology in development to achieve this is based on the Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT). The HBT is well suited for high speed, high power and uniform (across wafer) performance, due to the ability to tailor the material structure that electrons traverse through by well-controlled epitaxial growth methods. InP with its compatible lattice matched alloys such as indium gallium arsenide (InGaAs) and indium aluminium arsenide (InAlAs) provides for high electron velocities and high voltage breakdown capabilities. The epitaxial methods for this material system are fairly mature, however the implementation of high performance and reliable transistors are still under development by many laboratories. Our most recently fabricated, second generation mesa HBTs at JPL have extrapolated current gain cutoff frequency ($F_t$) of 142GHz and power gain cutoff frequency ($F_{max}$) of approximately 160GHz. This represents a 13% and 33% improvement of $F_t$ and $F_{max}$, respectively, compared to the first generation mesa HBTs [1]. Analysis based on the University of California, Santa Barbara (UCSB) device model, RF device characteristics can be significantly improved by reducing base contact resistance and base metal contact width. We will describe our effort towards increasing transistor performance and yield.

**Background**

Indium phosphide (InP) heterojunction bipolar transistors (HBTs) are one of the highest speed transistor technologies available. The advantages of this technology are enabled from the precise control of the semiconductor epitaxial properties that electrons traverse through. In HBTs, electrons move in the direction of epitaxial growth, as a result, the environment of the electrons at each region of transport in the transistor can be more easily and accurately controlled for optimum performance within the narrowest spatial dimensions. Because of this, InP HBTs can be grown with a large bandgap emitter region to reduce injection of holes from the base into the emitter that decreases gain with increasing base doping for reducing base resistance; the emitter-base junction can be alloy graded to minimize turn-on voltage; an alloy or doping graded base region can be grown in the epitaxy to produce a built in electric field to increase electron transport velocity through the base. Also through epitaxial growth for the collector region of the transistor, a high electric field breakdown material such as InP can be deposited so that the transistor may operate at higher voltages while maintaining short electron transport distances for speed. In contrast, other high speed transistor technologies, such as high electron mobility transistors (HEMTs), the electrons travel perpendicular to the direction of epitaxial growth and are confined to particular material layers with fixed properties. Modifications for material properties in the direction of electron transport for improving performance can only be done via processes after epitaxial growth, generally with less precision and more complications. Silicon Germanium HBTs, another high-speed technology, consists of semiconductor

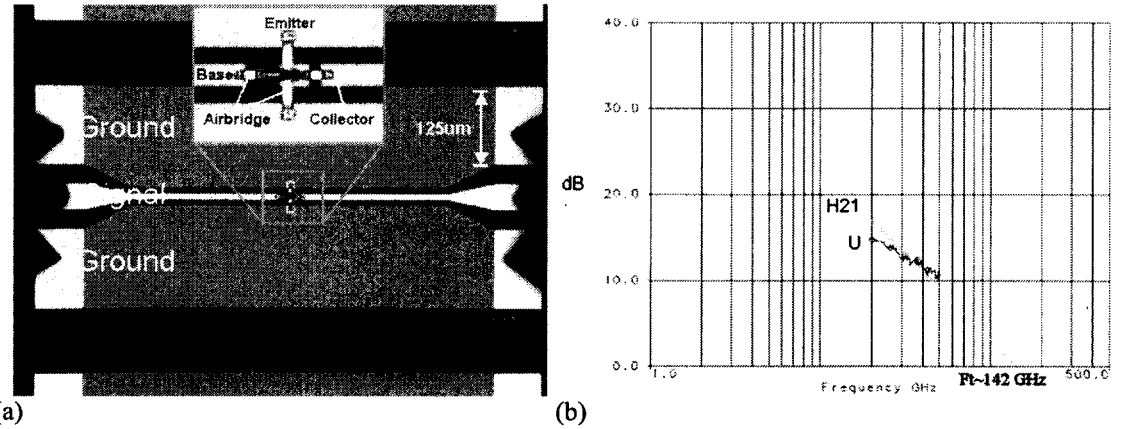
materials with lower breakdown voltages and are less suitable for power applications. InP HBTs are well suited for both high speed and high output power operation, which are desired for our applications.

**Motivation**

The goal of the effort at JPL is to develop the fastest reliable transistor process beyond what is available from industry and have the capability to easily add features for performance not typically allowed in foundry services that are fixed. We are pursuing HBTs as they have shown very high power gain, >20dB at 100GHz [2] and higher power handling capability due to epitaxial engineering of the collector region of the transistor, in contrast to HEMTs. We expect that HBTs will provide more power per unit area at higher frequencies than HEMTs, and will yield higher transistor count ICs due to its particular fabrication procedures. Recent studies have reported HBTs with $F_t$ of 509GHz and $F_{max}$ of 219GHz [3], and in another study $F_{max}$ of 478GHz with $F_t$ of 154GHz [4]. To date, InP HBTs have demonstrated single stage power amplifiers with 7.5mW output power at 172GHz and 5dB associated gain [5]. ICs with transistor counts approaching five thousand have also been demonstrated [6]. Upon implementation of an ultra-high-speed and high-power HBT process we plan to fabricate power amplifiers to provide more power to local oscillator chains for space heterodyne systems [7]. Additionally, high-frequency voltage controlled oscillators can potentially be fabricated to simplify local oscillator chains by reducing component count and size. Ultimately we would like to have a high yield process so that we can develop ultra-high speed mixed-signal ICs. Systems that we would like to utilize this technology in are for THz imaging systems, which are in development at JPL [8], and also future space hardware such as advanced autocorrelators for high-resolution remote sensing spectral analysis.

**Development of Mesa InP HBTS**

At JPL, we recently completed fabrication of second-generation mesa HBTs with extrapolated $F_t$ and $F_{max}$ of approximately 142 and 160GHz, respectively. The epitaxial wafer used consisted approximately of a 120nm InP silicon doped emitter, 30nm carbon doped InGaAs base layer and a 210nm InGaAs/InAlAs alloy graded to InP silicon doped collector layer. HBTs fabricated on this epitaxial structure had submicron emitter features of 0.3x4, 0.5x4 and 0.7x4$\mu m^2$ defined with electron beam lithography. All other transistor features are fabricated with 2 μm minimum feature size contact lithography, wet etching and electron beam metal evaporation. Polyimide is used for planarization and passivation. For RF characterization, on-wafer measurements are performed with an Agilent 8510C vector network analyzer. Through-Line-Reflect (TRL) on-wafer standards are used to calibrate the measurement setup. S-parameter measurements are taken between 10 and 50GHz. S-parameters as a function of frequency are converted to current gain (H21) and Mason's unilateral gain (U) as a function frequency. A -20dB/dec extrapolation from H21 and U is used to determine $F_t$ and $F_{max}$, respectively, at the frequencies where the gains extrapolate to 0dB (see Figure 1 (b)). This standard extrapolation is based on the behavior expected from the hybrid-pi model.




(a) (b)

*Figure 1: (a) Optical photo of an InP mesa HBT. (b) Gain plots of a 2x0.7x4$\mu m^2$ InP mesa HBT calculated from S-parameter measurements. $F_t$ and $F_{max}$ are 142 and 160 GHz, respectively. Bias condition for the emitter current density $J_e$ is 190 kA/cm$^2$ and collector-emitter voltage is 1.25V.*

Since the RF and DC measurements of the second generation HBTs and test patterns, we have performed analysis of the device structure to determine how performance can be improved. Using the UCSB device model, we find that performance can be substantially improved by reducing parasitic resistances and capacitances associated with base contact resistance and base metal contact width (base-collector capacitance). Figure 2 (a) and (b) show the general trend of $F_t$ and $F_{max}$ as a function of base contact resistance and base contact width of the next generation of HBTs we are presently developing. To realize improvements in performance we are also currently examining UCSB's base metal fabrication process, which can provide for specific contact resistances of 20 ohm·μm$^2$ or less. To reduce base metal contact width, the JPL in-house process is being migrated from contact lithography to stepper projection lithography, so that smaller 1μm minimum feature size structures can be produced.

To improve HBT yield we have implement T-shaped emitter metal structures at the beginning of the second generation of HBTs fabricated at JPL. Electrical measurements of first generation HBTs indicated that yield is greatly reduced during the base-emitter junction fabrication process. Scanning electron microscopy in some cases showed that while some emitters are properly etched some still did not have complete undercut etching around the entire periphery of the emitter metal stripes. As a consequence, after deposition of the self-aligned base metal, many emitter-base junctions would be electrically shorted. The T-emitter metal structure is implemented so that an additional spacer is provided to keep evaporated base metal from shorting to the emitter epitaxy (see Figure 3). Additional benefit of this structure is that it allows the base metal thickness to be increased, reducing electrical and thermal resistance, and inductance of the base metal.

**Summary**

JPL in collaboration with UCSB and RJM Semiconductor is developing an in-house advanced mesa InP HBT and Transferred Substrate HBT process [1]. These processes can be utilized to produce components to improve systems for future astrophysics, planetary and Earth science THz missions. At JPL we have demonstrated, second generation emitter mesa HBTs with $F_t$ of 142GHz and $F_{max}$ of 160 GHz, first generation mesa HBTs with $F_t$ of 126GHz and $F_{max}$ of 120GHz, and first generation Transferred Substrate HBTs with $F_t$ of 110GHz and $F_{max}$ of 150GHz. Performance of the HBTs will improve by reducing parasitic resistances and capacitances, and reducing the distance electrons need to travel through the device. These requirements can be addressed through the minimization of base contact resistance, the reduction of base metal width, and the scaling of epitaxial layers.

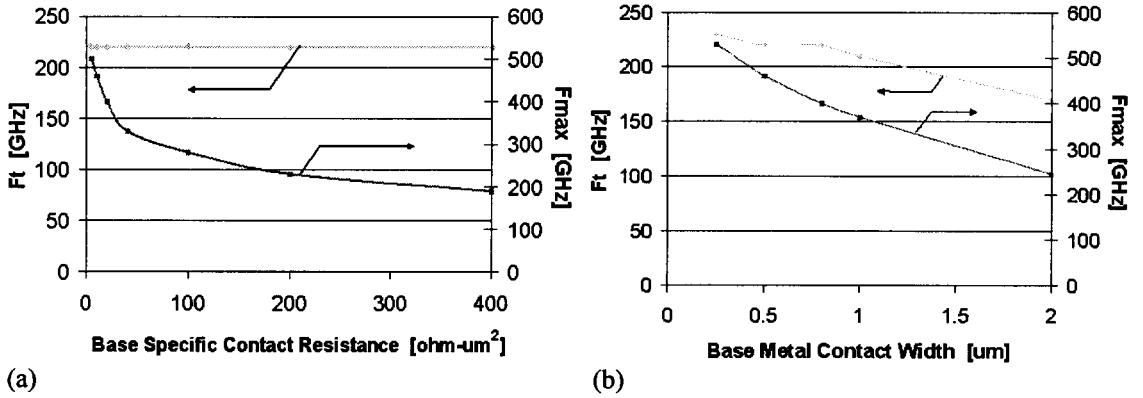



*Figure 2: Simulations for the next generation of mesa HBTs based on the UCSB device model. Emitter area is 0.7x12 um$^2$ and emitter to base metal spacing is 0.25 um. Base-emitter voltage bias is 0.68V and collector-emitter voltage bias is 1.2V. (a) Cutoff frequencies versus base contact resistance for a HBT with 0.8 um base metal width. (b) Cutoff frequencies versus base contact width for a HBT with 20 ohm-um$^2$ specific base contact resistance.*

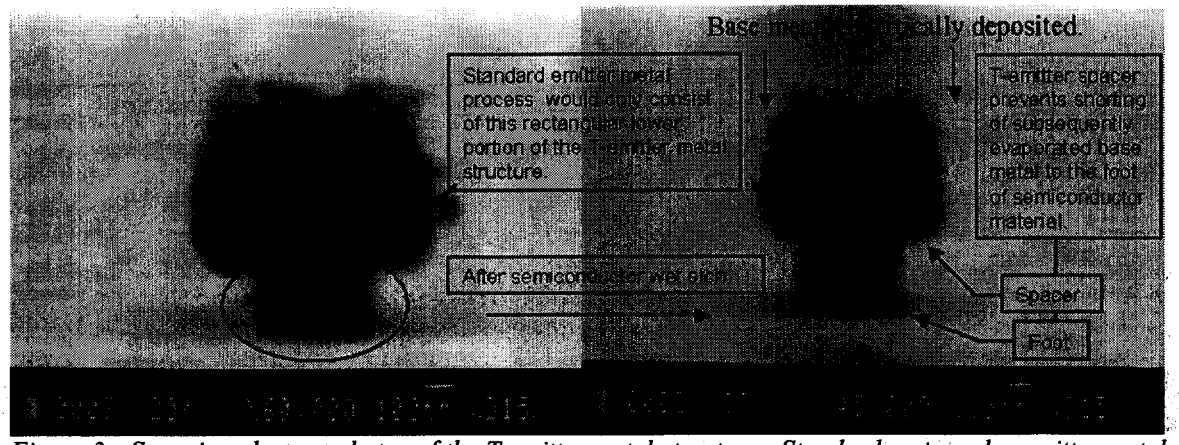



*Figure 3: Scanning electron photos of the T-emitter metal structure. Standard rectangular emitter metal structures do not have spacers and require more control to obtain enough undercut of the semiconductor emitter epitaxy so that the emitter metal can properly shadow mask the subsequently vertically deposited base metal from shorting to the emitter epitaxy. In this example it can be seen that the foot of the semiconductor emitter material protrudes out enough that without the spacer provided by the T-emitter metal, evaporated base metal would short to the emitter.*

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