

## **Flexible electronics for space applications**

Erik Brandon, William West, Lisong Zhou<sup>1</sup>, Tom Jackson<sup>1</sup>, Greg Theriot<sup>2</sup>, Rod A.B. Devine<sup>2</sup>, David Binkley<sup>3</sup>, Nikhil Verma<sup>3</sup> and Robert Crawford<sup>3</sup>

NASA Jet Propulsion Laboratory, California Institute of Technology  
Pasadena, CA 91109

<sup>1</sup>Pennsylvania State University  
University Park, PA 16802

<sup>2</sup>Air Force Research Laboratory, Kirtland Air Force Base  
New Mexico 87117

<sup>3</sup>University of North Carolina, Charlotte  
Charlotte, NC 28223

### **ABSTRACT**

NASA is currently developing a host of deployable structures for the exploration of space. These include balloons, solar sails, space-borne telescopes and membrane-based synthetic aperture radar. Each of these applications is driven by the need for a thin, low mass, large area structure (i.e., polymer-based) which could not be implemented using conventional engineering materials such as metals and alloys. In each case, there is also the need to integrate sensing and control electronics within the structure. However, conventional silicon-based electronics are difficult to integrate with such large, thin structures, due to a variety of concerns including mass, reliability and manufacturing issues. Flexible electronics, particularly thin film transistors (TFTs), are a potentially key enabling technology that may allow the integration of a wide range of sensors and actuators into these types of structures. There are numerous challenges, however, regarding the survivability of such devices during stowage and deployment of the structure, as well as during operation in the harsh environments of space. We have fabricated TFTs on polyimide substrates, and are investigating the durability of these devices with respect to relevant space environments. We are also developing flexible sensor technologies for the integration of distributed sensor networks on large area structures.

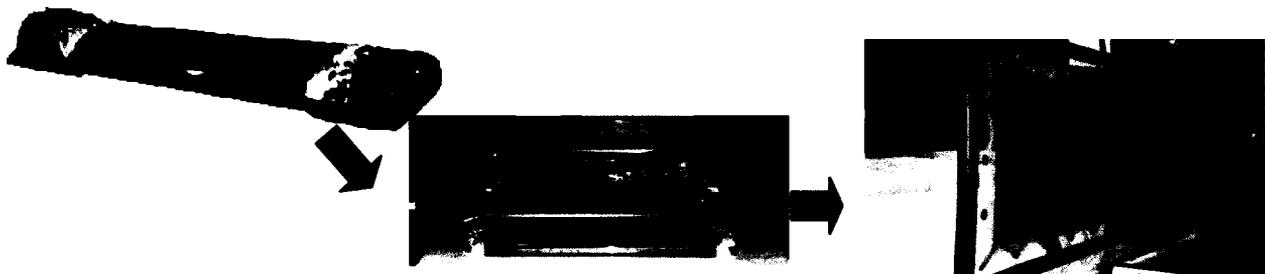
### **INTRODUCTION**

Research and development efforts focusing on flexible electronics is currently an area of rapid growth in the microelectronics industry [1]. Applications as wide ranging as flexible displays and electronic textiles are under consideration for various commercial markets. Despite the significant challenges, there are also numerous opportunities for employing flexible electronics in the realm of aerospace applications.

For example, NASA is designing and developing various large area deployable spacecraft concepts for both earth science applications and deep space exploration [2]. The use of deployable structures reaches back into the 1950s, when the 30 meter inflatable ECHO balloon was launched as a reflector for radar signals. A variety of other inflatable/deployable structures have been conceived and/or launched. In each case, the structure is comprised of a large, flexible polymeric substrate. The main goal of this approach is aimed at overcoming the limitations in the maximum size of spacecraft which can fit in the fairing of a standard launch vehicle. This is

critical in applications such as antenna arrays, where launching rigid space structures based on traditional engineering materials imposes an unacceptable mass and volume penalty.

The structures are constructed to readily collapse to a size much smaller than that of the fully deployed spacecraft, so that it can be readily mated with the launch vehicle. At the appropriate time following launch, a variety of deployment mechanisms can be used to bring the spacecraft to its operational configuration. This may include the use of inflation and/or rigidizeable thermosetting polymers, to form the final structure. A key aspect of this approach is the use of a large thin “membrane” which serves as the main structure. This can be utilized, for example, to build large earth-orbiting antenna arrays for use in synthetic aperture radar.



**Figure 1.** A deployable synthetic aperture radar, shown in its stowed and deployed configuration.

The use of these deployable structures, however, introduces numerous technical challenges. One application of deployable structures is in the area of solar sails, which would utilize a large, thin membrane to gain momentum from impinging photons of light from the sun as a means of propulsion. The solar sail must be very large (hundreds of meters on a side) and very light (targeted areal density of  $<1 \text{ g/m}^3$ ). Despite these restrictions, an entire suite of health monitoring sensors must be integrated with the surface of the sail to monitor temperature, strain, charge build-up, radiation exposure, and other critical aspects of the sail health. Other applications such as large antenna structures or optical telescopes would benefit from integrated sensors for use in determination of the structures shape and planarity, which is often critical in pointing operations. These sensors could also be combined with integrated actuators to add an element of control.



**Figure 2.** Conceptual image of a solar sail, in the fully deployed configuration.

Use of conventionally packaged sensors and electronics and standard attachment techniques for integrating the various parts to the large, thin structure leads to a number of vexing problems, however. The first key issue is that of assembly. Conventional pick-and-place assembly is made difficult when dealing with 100 m x 100 m structures which are  $\leq 0$   $\mu\text{m}$  thick, and “touch labor” becomes a significant issue particularly when hundreds or thousands of sensor nodes may be required. Other critical issues include the mismatch in thermal expansion between the electronic parts and the underlying thin, flexible structure, the reliability concerns related to the attachment materials and the reduced mechanical flexibility resulting from the use of rigid parts.

Flexible electronics provides a potential means to address these concerns. The mechanical flexibility of these devices obviates many concerns with the use of rigid packaging, and the possibility of directly integrating the electronics with the structure can potentially remove many of the attachment concerns. The most appealing advantage, however, is the possible use of “roll-to-roll processing,” to circumvent the issues of touch labor involved in assembly.

To successfully employ flexible electronics in this arena will require answering many difficult technical questions. The main question is the issue of reliability and robustness. This arises from the fact that the design space of commercial and aerospace interests do not overlap. Commercial interests are largely focused on high volume, low cost, expendable applications (such as smart cards, electronic labels and radio-frequency identification tags), whereas space applications will require high reliability, long life, robust technologies. Other questions also persist. For example, how will these devices be incorporated into the structure and what type of processing technologies will be employed? More fundamentally, what types of devices will be needed to construct distributed sensor arrays, and how will circuit-level design issues be addressed in light of the poorer performance of flexible electronics vs. traditional silicon-based integrated circuits?

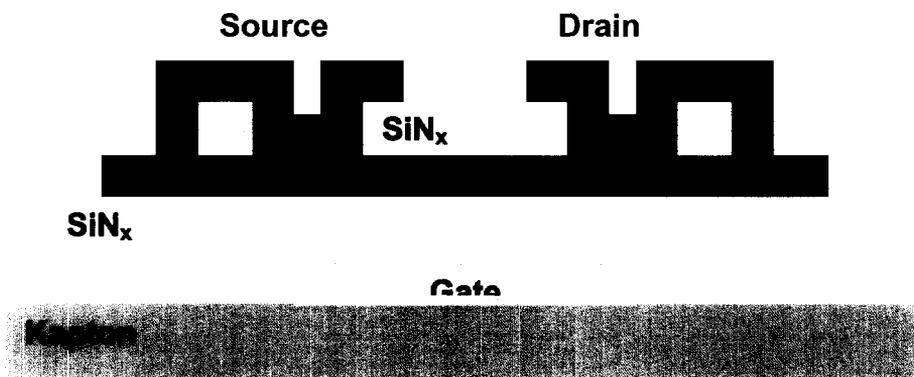
To start answering these questions and to help pave the road for the use of flexible electronics in aerospace applications, work in our labs has focused on testing the reliability of these devices in relevant space environments, particularly with regard to radiation and mechanical stress. This work is, therefore, focused on addressing the mismatch in the design space between the commercial and aerospace interests. We are also investigating barriers to integration of these devices on large structures, and the circuit-level design issues. If addressed, flexible electronics could play a role in applications beyond deployable space structures, including the development of flexible spacesuit health monitors for use by astronauts.

## **EXPERIMENTAL DETAILS**

Several different test structures were designed and fabricated for the evaluation of flexible transistor performance. In each case, a thin film transistor (TFT) architecture was utilized. Two thin film semiconductor materials were employed: hydrogenated amorphous silicon (a-Si:H) and pentacene.

**Fabrication of a-Si:H TFTs.** The a-Si:H TFTs were fabricated at Penn State University. A 50  $\mu\text{m}$  thick Kapton<sup>®</sup> E polyimide material was used as the flexible substrate. The substrate was first heated at 250°C for several hours under vacuum to reduce the level of moisture and volatile contaminants, and to pre-shrink the material for improved thermal dimensional stability prior to

the TFT processing. To facilitate fabrication of the devices on the flexible material, the film was mounted on a glass carrier with a silicone-based pressure sensitive adhesive. The adhesive allows the substrate to be readily removed from the rigid carrier following fabrication. Gate electrodes for the a-Si:H TFTs were patterned by standard photolithography and wet etching techniques from a 75 nm thin film of chromium deposited by thermal evaporation. A tri-layer stack comprised of a SiN<sub>x</sub> gate dielectric layer (300 nm), a-Si:H active layer (50 nm) and a SiN<sub>x</sub> passivation layer (300 nm) was then deposited using a three chamber loadlock plasma-enhanced chemical vapor deposition (PECVD) system with a maximum processing temperature of 250°C. After the a-Si:H active layer and SiN<sub>x</sub> passivation layer were patterned, a 50 nm n-type microcrystalline silicon (n<sup>+</sup> μ-Si) contact layer was deposited at 250°C using PECVD, and 200 nm thick molybdenum source and drain contact electrodes were deposited using a DC sputtering system. These layers were both patterned by a combination of CF<sub>4</sub> reactive ion etching (RIE) and wet etching. The bottom SiN<sub>x</sub> patterning step was completed only after the n<sup>+</sup> μ-Si was etched by potassium hydroxide, which otherwise serves as an etchant for Kapton<sup>®</sup>. A similar method was used to investigate the post-process deposition of a-Si:H TFTs on radar patch substrates. In this case, a patterned DuPont Pyralux<sup>®</sup> polyimide substrate was used in which the radar patches were patterned from copper using a photolithography and wet etch process.



**Figure 3.** Cross-sectional depiction of the a-Si:H TFT test structure.

**Fabrication of pentacene TFTs.** Bottom contact pentacene-based TFTs were also fabricated and tested. For these devices, a silicon wafer served as the substrate. A 110 nm dry oxide was first grown at 900°C on n<sup>++</sup> degenerate Si (100) wafers for the gate dielectric layer. The source and drain electrodes were then patterned by first spin coating ~400 nm of photoresist onto the oxide, followed by a bake step to remove solvent. The photoresist was subsequently patterned and ~200 nm of gold deposited on the developed photoresist using a thermal evaporator. A lift-off process was then used to reveal the source and drain pads formed directly on the oxide. The oxide and electrodes were then vapor treated with octatrachelorsilane (OTS) to reduce the overall surface energy of the substrate and contacts and to promote optimal growth of the organic semiconductor. Pentacene was then deposited using thermal evaporation onto the OTS treated oxide and electrodes to form the devices.

**Radiation and mechanical testing.** The a-Si:H TFTs were evaluated following irradiation by 1 MeV fast electrons at the JPL Dynamitron Facility, with total doses up to 1 Mrad (Si). Devices were probed using a Hewlett Packard 4145B transistor parameter tester at both JPL and Penn State University. Device characteristics were then extracted from the electrical data. Typically,

devices were characterized by sweeping the gate electrode-source voltage ( $V_{gs}$ ) from 0 to  $-20$  V for different, stepped values of the drain-source voltage ( $V_{ds}$ ) and measuring the drain-source current ( $I_{ds}$ ). Measurements were also performed by sweeping  $V_{ds}$  for fixed  $V_{gs}$  values to obtain the saturation drain-source currents. Channel carrier mobilities and the threshold voltages for the different devices were determined from the data. The mobilities were determined from plots of the slope  $dI_{ds}/dV_{gs}$  as a function of  $V_{ds}$  while the threshold voltages were determined from plots of  $\sqrt{I_{ds}}$  versus  $V_{gs}$  measured in the saturation current regime. Following the initial characterization of the irradiated devices, they were thermally annealed at  $200^{\circ}\text{C}$  for two hours and re-measured.

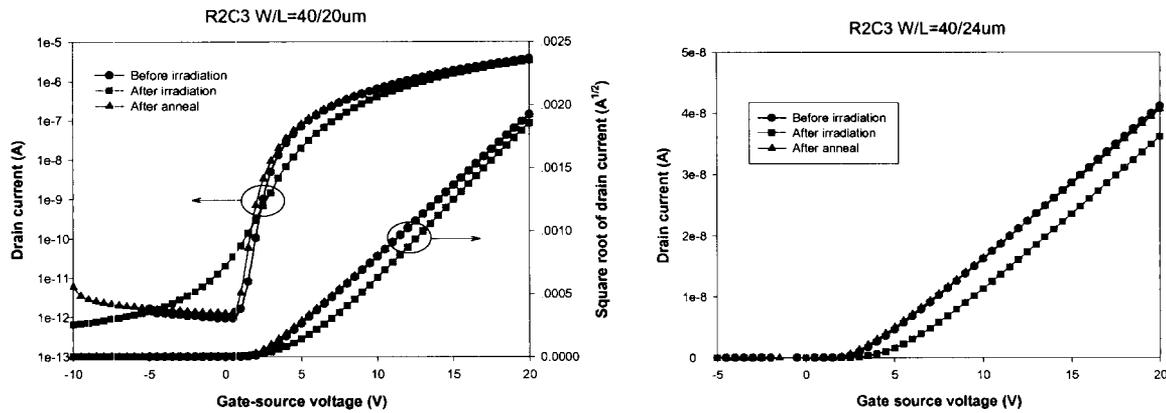
Pentacene TFTs were irradiated and tested at Kirtland Air Force Base. Electrical characterization of the pentacene devices was also carried out using a Hewlett Packard 4145B transistor parameter tester. The devices were tested in a probe station attached to an ARACOR 940 X-ray irradiation facility with a tungsten target. Typical dose rates used were  $\sim 280$  rads ( $\text{SiO}_2$ ) per second with the X-ray tube voltage at 50 keV and a current of 10 mA. Doses up to 1 Mrad ( $\text{SiO}_2$ ) were accumulated.

For mechanical testing of the a-Si:H TFTs on polyimide, an Instron 1331 load frame was used to apply the uniaxial in-plane tension to the flexible substrate and devices (fabricated using the same substrate and process outline above), with subsequent electrical characterization of the TFTs at both JPL and Penn State University.

## DISCUSSION

**Radiation testing of a-Si:H TFTs.** The main goal of this effort was to evaluate the influence of the space environment on the operation of flexible TFTs. Since radiation is ubiquitous in space and always a primary concern for electronics reliability, significant effort was focused on the evaluation of devices before and after exposure to ionizing radiation. An array of thirty a-Si:H TFTs was evaluated, with the devices exposed to an annealing step following the initial irradiation. For these a-Si:H TFTs, devices with a channel geometry of  $L=24$   $\mu\text{m}$  and  $W=40$   $\mu\text{m}$  were first measured at Penn State University with subsequent electron irradiation at JPL.

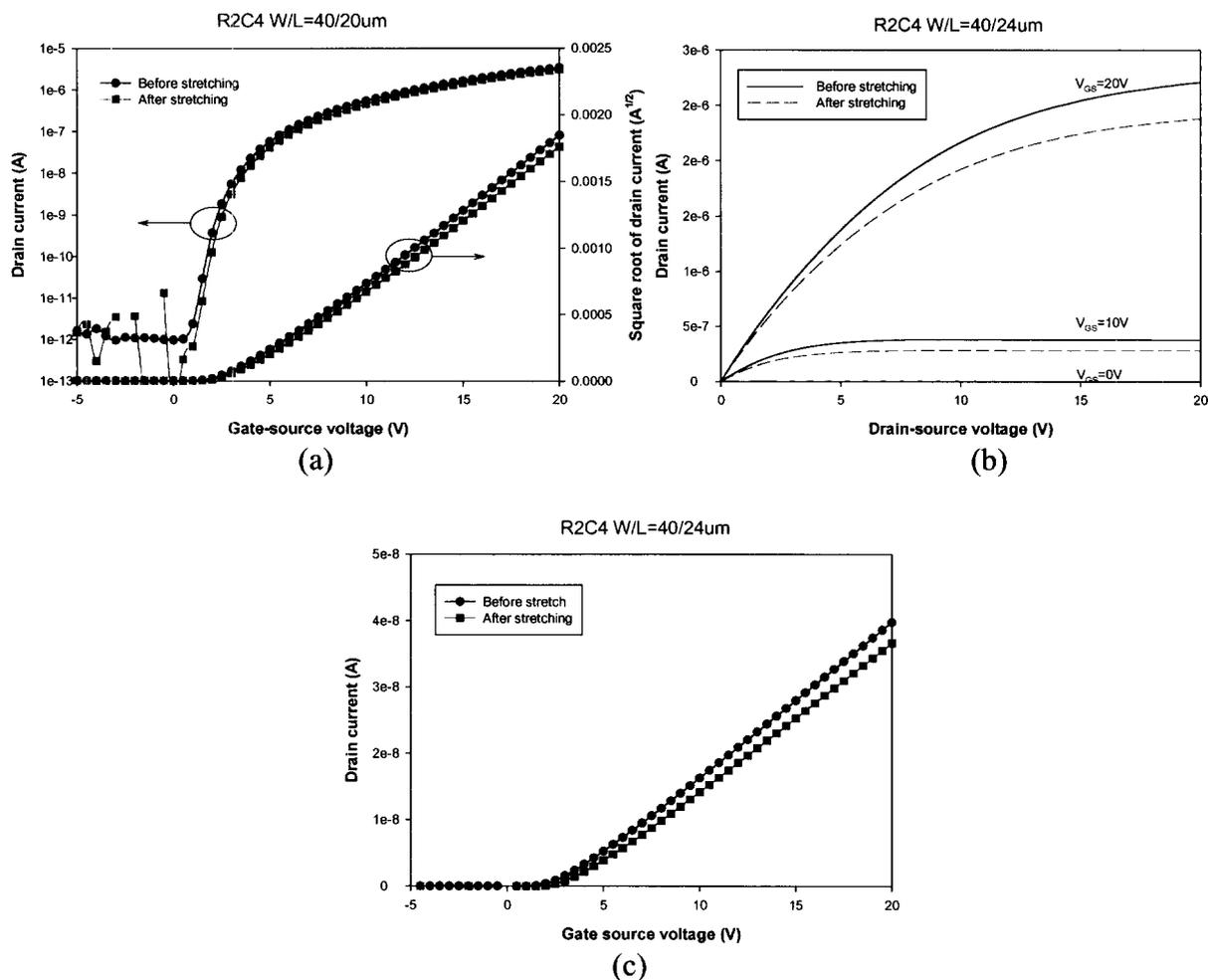
Only two of the devices were completely inoperable following the 1 Mrad (Si) total dose of 1 MeV fast electrons. For the 28 surviving TFTs, the measured off-current was at  $<1$  pA despite irradiation. This value was maintained following a subsequent anneal step. About half of the irradiated devices displayed either a positive or negative shift in the threshold voltage ( $V_{th}$ ) of  $>1$  V, from their initial values of 3-4 V prior to irradiation. Following a thermal anneal at  $200^{\circ}\text{C}$  for two hours, most of the devices displayed a  $V_{th}$  similar to their initial value. Increases in saturation field-effect mobility ( $\mu_{sat}$ ) of up to 20% from the initial value of 0.5-0.8  $\text{cm}^2/\text{V}\cdot\text{s}$  were also observed for about half of the devices, while about one-quarter of the devices increased between 10-20%, and about one quarter kept their  $\mu_{sat}$  value to within  $\pm 10\%$  of the initial value. Sub-threshold slope values were observed to increase and often double from their initial values of  $\sim 0.5$  V/decade, with a return to initial values for most devices following the annealing step. Representative electrical data is shown in Figure 4, before and after irradiation and following the thermal anneal.



**Figure 4.** Electrical properties of a-Si:H TFTs before and after 1 Mrad (Si) total dose of 1 MeV electrons, and following a thermal anneal.

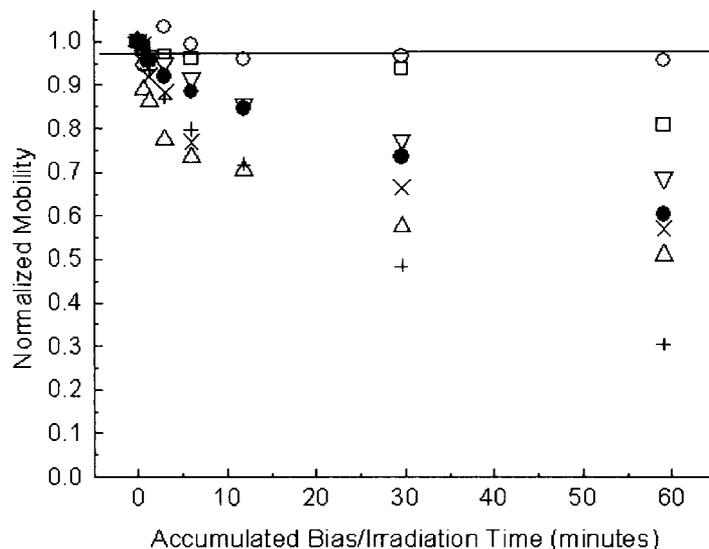
The data for a-Si:H devices may be largely interpreted in the context of existing models for TFTs on rigid substrates. The results indicate that shifts in TFT parameters do occur upon irradiation, but that performance can be recovered via healing by thermal annealing, as seen in Figure 4. This is despite the fact that the dielectric layer quality is lower than devices found on rigid substrates, due to the lower process temperatures involved.

**Mechanical testing of a-Si:H TFTs.** In the case of deployable structures, electronics integrated within the flexible structures would experience various forces during deployment operations (e.g., unrolling and tensioning) raising the concern of device failure. For example, devices experiencing prolonged tensioning may fail due to the influence of creep and/or delamination of the films. To evaluate the potential influence of these factors on device performance, mechanical testing was carried out under conditions meant to replicate selected service conditions experienced during deployment. To simulate a tensioning of the membrane structure, unidirectional tensile testing was carried out at JPL using an Instron 1331 load frame. The substrate was placed under uniaxial, in-plane tension for one hour at 2500 psi of force, as measured by the load cell. An array of twenty a-Si:H TFTs were evaluated before and after application of the tension. Two of the twenty devices were inoperable following application of this tension. Of the eighteen devices which survived, 70% of them displayed only minor changes in mobility, threshold voltage, and sub-threshold slope. Typical data, which is representative of the surviving devices, are depicted in Figure 5.



**Figure 5.** Electrical performance of a-Si:H TFTs before and after application of 2500 psi in-plane uniaxial tension for one hour.

**Radiation testing of pentacene TFTs.** Pentacene devices were tested before and after exposure to X-ray radiation at Kirtland Air Force Base. Devices tested varied in their geometry with the channel  $L = 5$  to  $20 \mu\text{m}$  and  $W = 100 \mu\text{m}$ . Irradiation of the devices was carried out with the source and drain contacts connected in parallel and a bias voltage applied between the gate electrode and the common source/drain terminal. Electric fields of  $\pm 0.5 \text{ MV cm}^{-1}$ ,  $\pm 1 \text{ MV cm}^{-1}$  and  $0 \text{ MV cm}^{-1}$  were used during irradiation. In one set of measurements, bias electric fields were applied in the absence of irradiation but for the same length of time as the radiation exposure. The latter process was undertaken to determine the bias stress induced effects in the absence of irradiation. The effective mobility ( $\mu_{\text{eff}}$ ) normalized to unity for unstressed and unirradiated devices is displayed in Figure 6. The data indicates that  $\mu_{\text{eff}}$  decreases upon exposure to the X-ray radiation. Devices simply exposed to a voltage bias stress demonstrated no significant decrease in mobility.



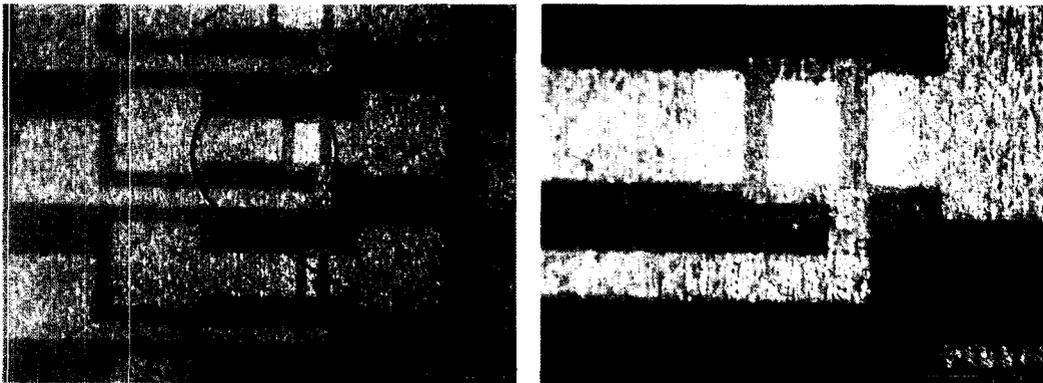
**Figure 6.** Variation of the effective mobility in various devices subjected to bias stress with or without X irradiation at a dose rate  $\sim 280$  rad ( $\text{SiO}_2$ ) per second. ( $\square$ )  $+1 \text{ MV cm}^{-1}$  bias field, ( $\circ$ )  $-1 \text{ MV cm}^{-1}$  bias field, ( $\Delta$ )  $-0.5 \text{ MV cm}^{-1}$  bias field and X rays, ( $\nabla$ )  $-1 \text{ MV cm}^{-1}$  bias field and X rays, (+)  $+1 \text{ MV cm}^{-1}$  and X rays, (x)  $+0.5 \text{ MV cm}^{-1}$  bias and X rays, ( $\bullet$ )  $0 \text{ V cm}^{-1}$  bias and X rays

An extensive data base exists for the influence of ionizing radiation on the performance of bulk transistors comprised of inorganic semiconductors such as silicon and gallium arsenide, and there is a fairly good understanding of how to make these devices less sensitive to the effects of radiation through the use of modified microelectronics processing methods (i.e., “radiation hardening”) [3]. There are also some limited data on silicon based TFTs, based on their use in medical imaging [4]. However, there is essentially no information regarding the influence of ionizing radiation on the performance of organic-based TFTs.

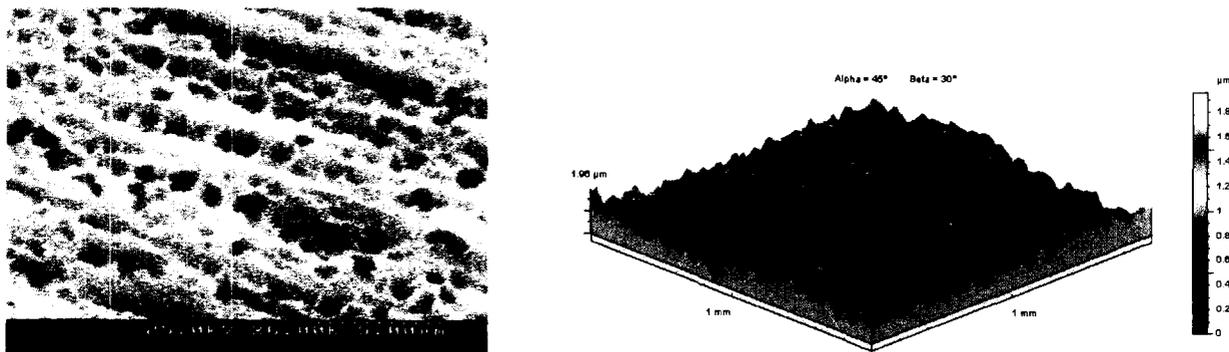
Based on the covalent nature of the pentacene semiconductor, ionizing radiation might be expected to induce the formation of significant populations of free radicals. Although the lifetime of these radicals is unknown, it is expected that their formation is followed by rapid intramolecular rearrangement and/or intermolecular cross-linking. This is in addition to the formation of positive charges which are trapped in the thermal oxide (giving rise to negative threshold voltage shifts). Therefore, a combination of several effects must be considered, including fundamental changes in the nature of the semiconductor film, as well as radiation induced charge trapping in the dielectric layer and at the semiconductor/oxide interface. In general, devices show a decrease in mobility as seen in Figure 5, although this decrease was small when accompanied by a voltage bias stress. To further understand these complex effects, radiation testing of pentacene devices is ongoing. It is critical to also understand the slow degradation in performance with time of these pentacene devices, which is coupled with the damage induced by the radiation.

**Post-processing of deployable substrates.** We have also investigated in our labs a key processing issue related to the use of flexible TFTs for deployable structures. It is envisioned that for numerous NASA applications, these flexible TFTs would be added in a post-processing step to a variety of large substrates which would serve as the main spacecraft structure. One likely scenario, for example, would be the addition of strain and temperature sensors to a patch antenna array (such as the one depicted in Figure 1). A typical array would be constructed by etching the antenna patches from a double sided copper-clad substrate such as flexible Pyralux® polyimide, with a subsequent post-processing addition of flexible TFT sensing electronics.

An attempt was made to fabricate a-Si:H TFTs on a Pyralux® polyimide substrate with a copper patch on back using the same process used for the pristine Kapton® E polyimide. A top view of these devices is depicted in Figure 7. It was found, however, the surface of the etched Pyralux® polyimide is too rough, which was measured by atomic force microscope (AFM) with peak to valley roughness about 2.28  $\mu\text{m}$  and mean square roughness about 0.3  $\mu\text{m}$ . This resulted in an essentially a zero yield for the devices. Scanning electron microscopy (SEM) and 3-D profilometry measurements are depicted in Figure 8, showing an etched Pyralux® polyimide surface.



**Figure 7.** Optical microscope images of the a-Si:H TFTs on Pyralux®



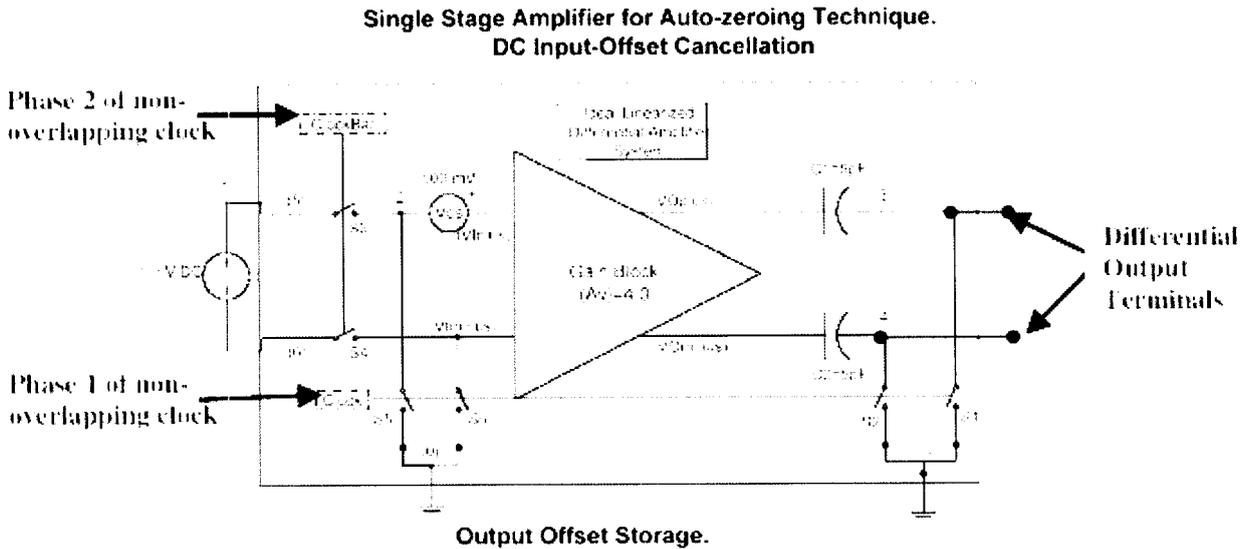
**Figure 8** Scanning electron micrograph (left) and 3-D profilometry image (right) of etched Pyralux® surface

**Design of organic TFT circuits.** Finally, viable circuit topologies for use in constructing distributed sensor arrays over large areas were conducted at the University of North Carolina, Charlotte. The use of organic or thin film based TFTs presents distinct challenges with respect to the use of conventional CMOS technologies, due to their inherently lower performance [1]. In order to implement these novel materials in TFTs which can be used to construct the sensor arrays, the circuit level issues must be addressed.

Despite their differences, organic TFTs do possess similar characteristics to MOSFET devices, suggesting that modifications to existing circuit techniques may be used to implement analog TFT technology. Low mobilities and poor n-type material require unique circuit topologies, however. In order to process small signals over large areas, it would highly beneficial to construct flexible amplifiers from the TFTs. It is anticipated that TFTs for use in signal conditioning would require a dc gain of 100 to 1,000 V/V, with dc offset  $\ll 1$  mV and a bandwidth of  $< 1$  kHz. Organic TFTs, however, are hampered by a relatively low transconductance, which results in low amplifier gain. This also results in low bandwidths, on the order of hundreds of KHz. Also, due to the unique nature of the materials involved, large supply voltage are required. Despite these drawbacks, good  $I_{on}/I_{off}$  ratios of near  $10^8$  can be achieved, which enables these devices to be readily employed as switches. These switches are critical for multiplexing the sensor nodes, to reduce the number of required interconnects. On resistances of  $1 \text{ k}\Omega$  are possible.

Another potentially serious drawback are the high dc offsets resulting from inherent process variations. This is detrimental for differential circuits which may be employed in the front end of operational amplifiers. Critical device parameters such as transconductance and drain source conductance must be closely matched for differential pairs.

It is important to realize, however, that organic transistors can indeed be used under conditions where slowly changing signals (such as for monitoring temperature, strain, etc.) must be monitored and amplified. Our initial assessment indicates that auto-zeroing techniques could be utilized to reduce charge injection effects and to cancel dc offset present in the input [5],[6]. This concept is depicted in Figure 9, for an amplifier with a gain of 4 V/V. The effect of the differential amplifier mismatch is represented as an offset of 500 mV at the input, and this offset is cancelled by the auto-zeroing circuit. For example, a dc input signal of 1 mV was applied in the model, resulting in a final output of 4 mV, as expected with the 500 mV input offset cancellation.



**Figure 9.** Auto-zeroed amplifier for use with organic TFTs.

## CONCLUSION

To address the potential use of flexible electronics in aerospace technology, various TFT devices have been evaluated with respect to several relevant space environments. An array of a-Si:H TFTs on Kapton<sup>®</sup> have been tested with respect to irradiation with fast electrons and tensioning of the underlying substrate. Although the radiation induces numerous changes in the device electrical characteristics, these changes can be readily recovered following a thermal anneal at 200°C, suggesting the damage is somewhat shallow. Addition of a-Si:H TFTs to non-pristine surfaces, however, resulted in very poor device yield. Furthermore, devices experiencing prolonged tensioning of the underlying substrate showed remarkable performance, with little change in electrical performance. This will require further development to enable post-processing addition of sensors to flexible substrates. Organic TFTs based on pentacene displayed a decrease in effective mobility with X-ray radiation, which was mitigated by the application of a bias voltage. Also, a variety of circuit techniques are currently being developed for use in the design of TFT based sensor arrays.

Future studies will focus on the possibility of developing “radiation-hardened” TFTs. Given the limited processing conditions available when flex substrates are involved, it is unclear to what extent these devices can be made more robust. However, recovery with annealing indicates healing mechanisms present in bulk CMOS devices are accessible in TFTs processed at low temperatures on flexible, polymeric substrates.

## ACKNOWLEDGEMENTS

We would like to thank Tom Hill of JPL for the mechanical testing, and Roy Scrivner of JPL for the operation of the Dynamitron facility. We would also like to thank Alina Moussessian of JPL for providing the etched antenna patches and Elizabeth Kolawa of JPL for her support of this work. This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology under a contract with National Aeronautics and Space Administration.

## REFERENCES

1. C.D. Dimitrakopolous and P.R.L. Malenfant, *Adv. Mater.* **14**, 99 (2002).
2. J. Huang, *IEEE Ant. Prop. Mag.* **43**, 44 (2001).
3. *Ionizing Radiation Effects in MOS Devices and Circuits*, T. P. Ma and Paul V. Dressendorfer, ed., Wiley-Interscience (1989).
4. J.M. Boudry and L.E. Antonuk, *Med. Phys.* **23**, 743 (1996).
5. *Design of Analog CMOS Integrated Circuits*, B. Razavi, McGraw-Hill (2001).
6. C.C. Enz and G.C. Temes, *Proc. IEEE.* **84**, 1584 (1996).