HIGH EFFICIENCY SYNCHRONOUS RECTIFICATION IN SPACECRAFT POWER SYSTEMS

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ABSTRACT

This paper examines the implementation of MOSFETs as synchronous rectifiers which results in a substantial improvement in power processing efficiency and therefore may result in significant reduction of spacecraft mass and volume for the same payload. Four topologies presented here are: two-switch forward, one-switch forward, boost with current-fed chopper and dual forward. In each case, parts count, mass, board area, part-load efficiencies at different input voltages, and qualification confidence were considered. It was found that each topology had the potential of providing improved overall performance. Synchronous rectification provided conversion efficiency of up to 93 percent compared to about 83 percent for power converters currently in use. It is also found that given the present status of magnetic devices, MOSFETs and their drive circuitry suitable for spacecraft applications, switching frequency above 100 KHz is not suitable if an efficiency higher than 90 percent is to be realized with the implementation used. Hybrid synchronous rectifier implementation is considered and is found to provide. savings in surface area, mass and ease of design.

[(is conceivable that the implementation of synchronous rectification may pmvidc increased efficiency improvements for 3Vdc converters for future spacecraft compared to SVdc converters

Key words: spacecraft power systems, converters, synchronous rectifiers.

1. INTRODUCTION

Spacecraft mass and volume depend on characteristics and per formance of its power generation, distribution, storage and power processing subsystems. A very large proportion of today's spacecraft provide prover to loads at 5 Vdc and 15 Vdc. However, there is a trend towards 3 Vdc for future spacecraft loads. In either case, it is imperative that the efficiency of power processing subsystems be as high as possible for significant reduction in spacecraft mass and volume.

Ilowever, tow voltage converters presentl y using conventional Schottky diodes arc less efficient because of significant forward-voltage drop. The situation worsens in 3Vdc converters. Fortunately, newer generation MOSFETs have much lower on-resistance [ban before and hence offer attractive potential of replacing Schottky diodes. A scheme. of such a replacement of Schottky diodes by MOSFETs is referred to as synchronous rectification. A synchronous rectifying circuit, in general, behaves like a diode that has an unusually low voltage drop during forward-voltage half cycles. Synchronous rectification has the added advantage that it eliminates the discontinuous conduction mode in a PWM converter.

Before 1990, Jet Propulsion Laboratory (JPL) concentrated on a two-terminal diode replacement IC (Ref. 1). As part of this effort, JPL contracted for design and fabrication of two-terminal synchronous rectifier with California State University at Long Beach (Ref. 2). The MOSIS (MOS Implementation Service) process was used in this study, The comparator and driver were found to be major stumbling blocks in realizing the efficiency goal. As a result of this effort, it was concluded that the entire converter should be built as a hybrid unit with externally driven synchronous rectifiers. A hybridized power stage will have less parasitic lead resistances and inductances which can deteriorate the efficiency and the noise performance of the converter (Ref. 3).

1 he only disadvantage. of this approach to the synchronous rectifier design is that it requires an extra drive circuit to command the MOSFET to operate as the passive switch. In non-isolated converters the requirement of an extra drive circuit is hardly a problem, but in isolated converters with multiple outputs, such as the push-pull or the forward converters, the requirement of extra drive circuitry may increase the. complexity of th converter circuit

1 his paper examines the require ments, the advantages and th limitations of synchronous rectifier circuits, Several circuit configuratior arc proposed and evaluated.

2. SYNCHRONOUS RECTIFIER TOPOLOGIES

While synchronous rectifiers are applicable to many topologies, th paper considers their usc in four topologies: two. switch forward, one switch forward, boost with current-fed chopper and dual forward. In wha follow's, first each topology is presented and then it is analyzed in terms c its performance.

2.1 Two-Switch Forward Converter

The two-switch forward converter, shown in Figure 1, is a buck-derive isolated converter. Because it is one. of the least stressful and one of th simplest converters to design and control, it is widely used for low an medium power applications (typically less than a few hundred watts Synchronous rectification can be easily implemented in this converter usin a single, penta-filar gate-drive transformer as shown in Figure 2. 1 h proper polarities of the windings ensure synchronous operation o(the fou switches. A single PWM waveform is applied to the gale-drive whit simultaneously turns switches S_1, S2 and S_3 on while turning S4 off, an vice-versa, During the on-time the input voltage is applied to the magnetizing inductance of the isolation transformer and to the output low pass filter scaled by the [urns ratio of the isolation transformer. During th off-lime, S_1, S2 and S3 arc turned off while S4 is turned on. Also. durir this time, the diodes D_1 and D2 (urn on to return the magnetizing current t the source. in order to reset the transformer. Since the magnetizing curre is small, the reset diodes need only to be fast recovery PN diodes. Ibis typ of reset mechanism ensures that the switches S_1 and S2 are never subjecte to a voltage stress larger [ban the input voltage even if there is some leakag inductance associated with the isolation transformer.

An experimental two. switch forward converter switched at 50KHz an using power MOSFETs (14mΩ on resistance) was built and tested. "1 h input voltage ranged from 21 .5V to 31.5V and delivered 5V at 6A. '1 h efficiency of the converter including the house-keeping power supply i shown in Figure 3 and is seen to be above 90% when the output power i large than 7 or 8 watts. 1 he maximum efficiency measured was about 92. S%.

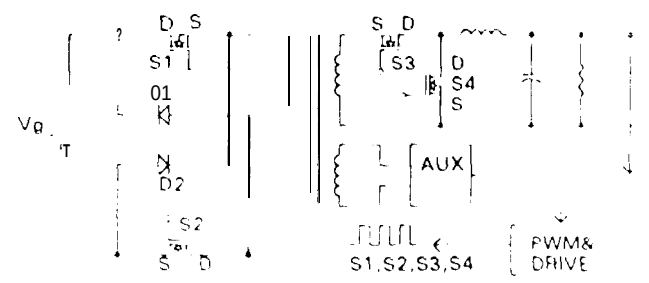

Figure 1, Two.Switch ForwardConverter

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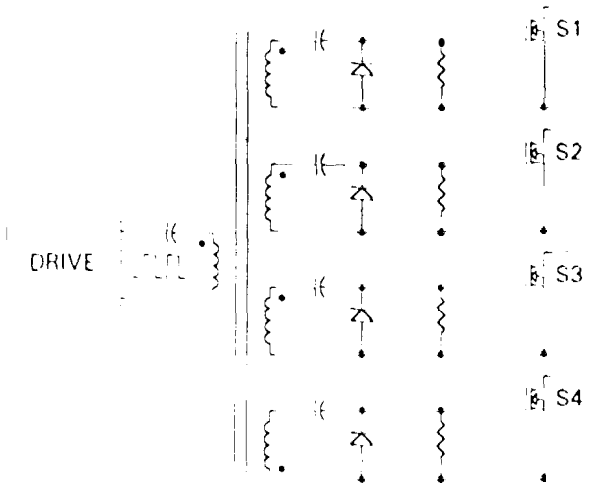

Figure 2. Synchronous Rectification Using a Single, Penta-Filar Gate.hive Transformer

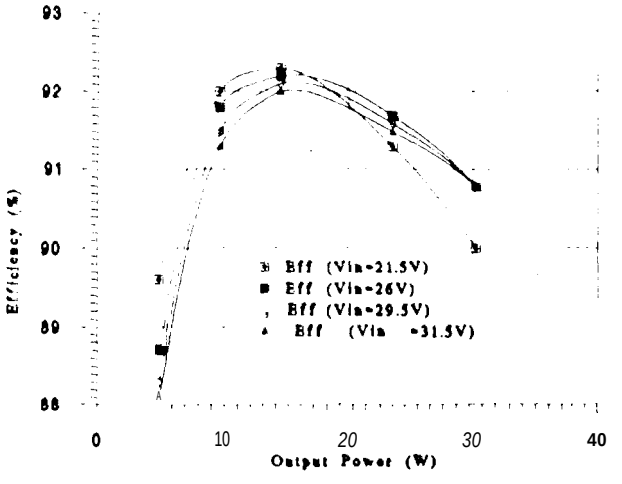

Figure 3. Plot of Efficiency Versus Output Power As a Function of Input Voltage

2.2 One-Switch Forward Converter

1 he simplified schematic circuit diagrdm of Figure 4 shows a basic one- switch (Q3) forward converter using synchronous rectification. The rectifier switch, Q1, and catch diode switch, Q2, are driven alternately from the same transformer T2 to prevent simultaneous conduction. Each of the three switches have identical gate drive circuits. Capacitor C 1 and inner diode VR1 function as a DC restorer with VR 1 also providing voltage spike protection for the MOSFET gate to source. Resistor RI and diode CR I provide a slower turn-on and a faster turn-off drive, thereby providing some dead time to insure no simultaneous conduction between Q2 and Q1, (Q3) during the switch transition interval. Unique so catch diode switch Q2 is the turn-off drive provided by transistor Q4 during system power down. This is essential to prevent output filter capacitor, Co, from discharging through L.I and Q2. Should Q2 turn off with this discharge current flowing through 11, a large destructive voltage spike would occur at the drain of Q1 and Q2.

The MOSFETs used were IRF150 types with a typical value of $R_{ds}(on)$ of 0.045Ω. The total conduction losses in Q1 and Q2 is:

$$P_{loss} = I^2R = (4)^2(.045) = 0.72W.$$

If a 45V, 16A Schottky rectifier SSR1645A (SSDI) is used, it's typical V_F is *0,436 v* at I_F = 5A. Therefore,

$$P_{loss} = I_F V_F = 4(0.436) = 1.744W$$

With an output power of 5V x 4A = 20W, this topology will provide an efficiency improvement of

$$An \approx \frac{\Delta P_{loss}}{P_{out}} = \frac{1.744 - .72}{20} = .0512,$$

or approximately 5%. Including the effect of reverse leakage losses would make Schottky rectifier approach less efficient than this converter *using synchronous rectification.*

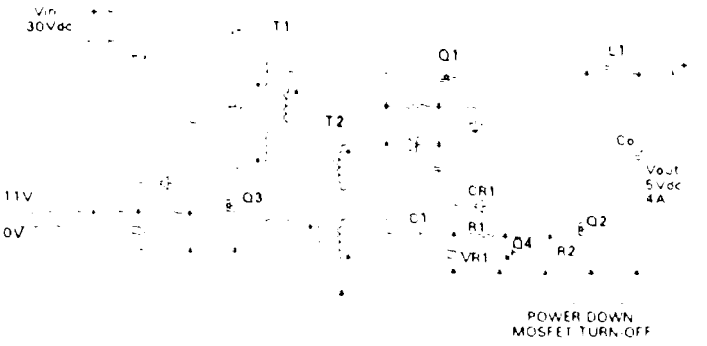

Figure 4. One-Switch Forward Converter Using Synchronous Rectification

2.3 Boost with Current-Fed Chopper

The topology shown m Figure 5 consists of a preregulator followed by a 100% duty cycle chopper. The chopper stage provides isolation and the possibility of multiple outputs. Although a boost preregulator is shown for purposes of illustration, any type Of converter would suffice. This topology minimizes the reverse voltage stress on the synchronous rectifier MOSFETs, resulting in two benefits. First, chc capacity losses due to the output capacitance Coss (Cgd + Cds) are reduced. Second, lower voltage FETs can be used, which significantly reduces the Rds(on) for a given die size.

In this topology, it is critical that the MOSFETs do not conduct simultaneously as this will short the output filter capacitor. 1 hus the drive scheme may be more complicated than that for the other topologies.

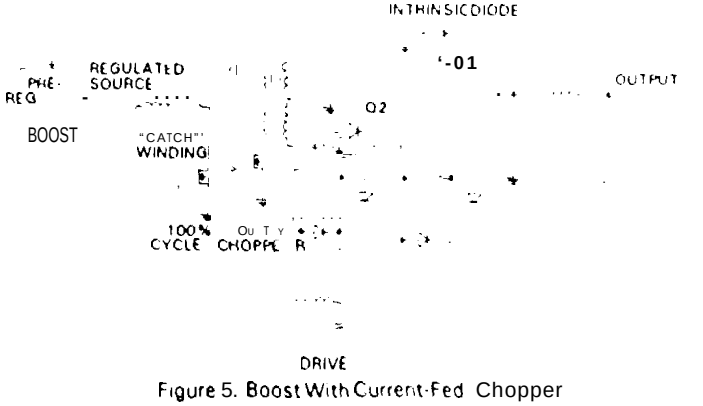

Figure 5. Boost With Current-Fed Chopper

2.4 Dual Forward Converter

The dual forward converter topology shown in Figure 6 shows two MOSFETs Q1 and Q2 which switch alternately and produce variable duty cycle pulse in the output of transformers. Q3 and Q4 also switch alternately and constitute a synchronous rectifier. Q5 clamps the current m the choke.

In an attempt to compare performance of dual forward converter with a converter using Schottky diode, Cassini spacecraft prover requirements were considered. The two designs were breadboarded and converter performances were compared. It was found that for 29V input voltage and 6A at 5V load, the loss with synchronous rectification was significantly lower Lhan with Schottky rectifier. Similar results were obtained at other input voltages and load currents. An efficiency of 90.7% was obtained for the conveter using synchronous rectification (Ref. 4).

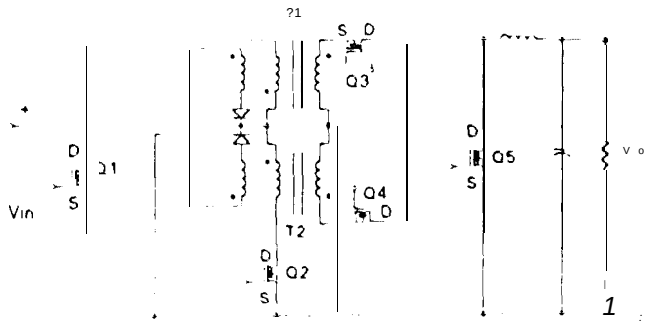

Figure 6 Dual **Forward** Converter Topology

3. OPTIMAL MOSFET SIZING

Component selection and minimization of losses is crucial to the successful implementation of synchronous rectification. This section presents a discussion on sizing hfOSF11"s in power switching applications to minimize switch losses. The three primary switch losses arc: (1) conduction loss due 10 $R_{ds(on)}$, (2) capacitive losses due to C_{gs}, C_{gd}, and C_{ds}, and (3) lure-Off crossover losses. For MOSFETs having identical breakdown voltages, there is an approximate inverse relationship between $R_{ds(on)}$ and C_{xx}, where C_{xx} denote.s any of the three terminal capacitances. This fact provides the basis for our optimization approach. The product R_{ds} C_{xx} is the crucial figure of merit for MOSFETs (Ref. S).

3.1 Simplified Analysis

Consider the following table of values for $R_{ds}(on)$ and C_{xx} for various International Rectifier (IR) HF XFET die sizes (IRF540, IRF530, IRF520 and IRF5 10), The capacitances are taken at V_{DS} = 10V. Table I shows Interdependence of R_{ds} (on) and device capacitances.

1 able 1, Interdependence of $R_{ds}(on)$ and device capacitances.

$R_{ds}(on)$ (ohms)	C_{gs}(pf)	C_{gd}(pf)	C_{ds}(ps)	Rds(C_{gd}+C_{ds})(ps)
0.077	1500	*125*	*7a)*	*64*
0.16	675	75	375	72
0.27	400	50	200	68
054	200	30	*100*	70

10 a good approximation, the product $R_{ds}C_{xx}$ is constant and we can write:

$$R_{ds} = \frac{1}{r} R_{ds0} \qquad (1)$$
$$C_{xx} = rC_{xx0}$$

where r is the MOSFET size scaling factor, and R_{ds0}, C_{xx0} can be obtained from the table.

The following analysis assumes that the device capacitances are constant despite the fact that they are actually nonlinear. A later section will provide a more exact analysis that takes the capacitance nonlinearity into account. We will ignore the turnoff crossover losses because they arc influenced primarily by external circuit factors such as switching speeds, parasitic inductances, and snubbing circuit%

Let Vp denote the peak dmin-to-source voltage, let V_{gs} be the gate-to-source voltage when the transistor is on, and let F_s be the switching frequency. For simplicity assume that the supply providing the gate drive power also have value V_{gs}. Then

$$\text{Conduction loss} = I^2_{rms} R_{ds} \qquad (2)$$
$$\text{Gate loss} = (C_{gs}+C_{gd})V^2_{gs}F_s + V_{gs}V_pC_{gd}F_s \qquad (3)$$

$$\text{Output capacitance loss} = \frac{1}{2}(C_{ds}+C_{gd})V^2_pF_s \qquad (4)$$

Substituting (1) mto the above expressions and adding the losses yields the following equation for the total loss P_T

$$P_T = \frac{1}{r}(I^2_{rms}R_{ds0}) + r((C_{gs}+C_{gd})V^2_{gs} + \frac{1}{2}(C_{ds}+C_{gd})V_p^2)F_s \qquad (5)$$

This function has the form $(A\frac{1}{r} + Br)$ hence the minimum occurs when the two terms are equal ($r=\sqrt{A/B}$), and the value at the minimum is twice the geometric mean of the two terms, i.e., $P_T(min)=2\ I/AR$. Thus,

$$P_T(min) = 2\sqrt{(I^2_{rms}R_{ds0})((C_{gs}+C_{gd})V^2_{gs} + \frac{1}{2}(C_{ds}+C_{gd})V^2_p)F_s} \qquad (6)$$

In many cases the output capacitance loss dominates the gale Capacitance loss. ([n zero-voltage switching topologies this is not true .) Then the loss expression simplifies to

$$P_T = I_{rms}V_p\sqrt{2F_sR_{ds0}(C_{gd0}+C_{ds0})} \qquad (7)$$

Notice that the optimal switch loss increases as the square root of the switching frequency,

As a numerical example, consider I_{rms} = 0.64A, V_p = 30V and F_s = I(MI K}{z, Then the minimum loss (using the simplified equation) is 71mW, and it occurs for an R_{ds} of 0.086 ohm, One would then choose the FET within the family having the closest R_{ds} (on), It should be noted that the function $(\frac{A}{r} + Br)$ has relatively bred minimum and, as a result, one may wish to choose a smaller MOSFET than the optimal equation may suggest

3.2 A More Exact Analysis

This analysis considers gate-drive loss, output capacitance switching loss. and conduction loss. Gate charge (Q_g) values from the IR data sheet will be used 10 estimate the gate losses. 1 he following data assumes V_{GS} = IOV, V_{DS} = 50V. There is little difference in the total gate charge for V_{DS}>30V. As a rule of thumb we estimate the gate charge at V_{DS} = 10V by multiplying the 50V value by 0,8 The gate charge does depend significantly on the peak gate voltage. Table 2 shows interdependence of R_{ds}(on) and gate charge,

I'able 2. Interdependence of R_{ds} (on) and gate charge

De Vice	R_{ds}(on)(ohms)	Q_g(nc)	$R_{ds}Q_g$(ohm-nc)
IRF540	*0.77*	*37*	*2.85*
IRF530	.*16*	17	2.72
IRF520	.?7	9.5	2.57
LRF'51o	,54	5	2.70

The gate loss *per* cycle is Q_gV drive. V drive is the voltage source supplying the gale drive power. Its value is usually approximately the peak gate-to-source voltage.

The output capacitance C_{oss} - C_{gd} + C_{ds} is highly non-linear. From the IR data sheet for the IRF510 device we find the following dependence of output capacitance on drain-source voltage:

V_{DS}	C_{oss}
4	193pf
10	123pf
20	87pf
40	63pf

Assuming a capacitance-volmgc dependence of the form C_{oss} = $C_0V_{DS}^{-n}$ and using a least-squares fit. onc finds

$$C_{oss} = 378\,V_{DS}^{-.488}\,(pf). \qquad (8)$$

To validate this equation, we compare its predictions wrth the actual data

VDS	C_{oss} (data sheet)	C_{oss} (Predicted)
4	193pf	192pf
10	123pf	123pf
20	87pf	88pf
40	63pf	62pf

The energy lost per cycle in the output capacitance is given by the equation:

$$E_s = \int_0^{V_p} C(v)v\,dv$$
$$= \int_0^{V_p} C_0 V^{1-n} dv$$
$$= \frac{C_0 V_p^{2-n}}{2-n} \qquad (9)$$

Therefore, [he total switching loss is given by the equation:

$$P_T = \frac{1}{T}(I^2 rms R_{ds0}) + f(Q_{g0} Vdrive + \frac{C_0 V_p^{2-n}}{2-n})F_s \qquad (10)$$

$$P_T(\min) = 2\sqrt{(I_{rms}^2 R_{ds0})(Q_{g0} Vdrive + \frac{C_0 V_p^{2-n}}{2-n})F_s} \qquad (11)$$

Note that the parameters C_0, Q_{g0}, R_{ds0} can be taken from a representative member of the family or from a curve fit of the FET family's parameters. They will differ significantly for FETs with different voltage ratings.

For example, if I_{dc} = 10A, V_p = IOV, V_{gs} = 10V, V_{drive} = 10V, F_s = 100KHz, then P_t (min)= 1.0W. A Schottky diode would dissipate approximately 4W.

4.HYBRIDIZATION C) F- SWITCHINGCOMPONENTS

During development some disadvantages of synchronous recufication were observed. 1 hese are: circuit complexly, cost increment and increased board area For example, in a dual forward topology, at 30W output, it was found that the parts count increased by 24 pares and the board area increased by 2.9 in^2. In addition, some need for development cost associated with non-recurring engineering, par ts, space qualification, documentation and testing became very apparent. As a result, hybrid implementation was considered.

The power switching components of a de-Lo. dc converter for low voltage applications can be hybridized m provide savings in surface area and ease of design. The main electrical specification of this application are (a) 22-35 V input voltage range (b) 5V output voltage at 30 W at temperatures between -35°C to 85° C. The topology best suited for this application is the dual forward converter with synchronous rectification because it combines the low peak voltage stresses with a very simple drive scheme (Ref. 5).

The power switching circuit for this forward converter is shown in Figure 7. It includes (a) 4 power MOSFETs, (b) the gate-drive circuit electronics, (c) current-sense transformer and (d) reset diodes. The module is driven by a single PWM signal and is powered by 10V bus. The remaining terminals are connected to the primary side (4 terminals) and the secondary side (3 terminals) of the power convener, Figure 8 shows a hybrid circuit implementation. The layout of the circuit on the hybrid substrate is very crucial for reduced common mode noise, radiated noise and control noise interference. Figure 9 shows che hybrid implementation layout.

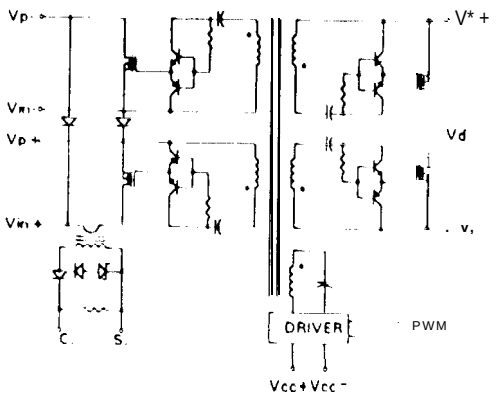

Figure 7. Power Switching Circuit For a Forward Converter

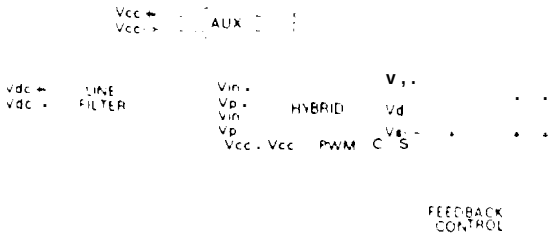

Figure 8 The Synchronous RectifierHybridModule

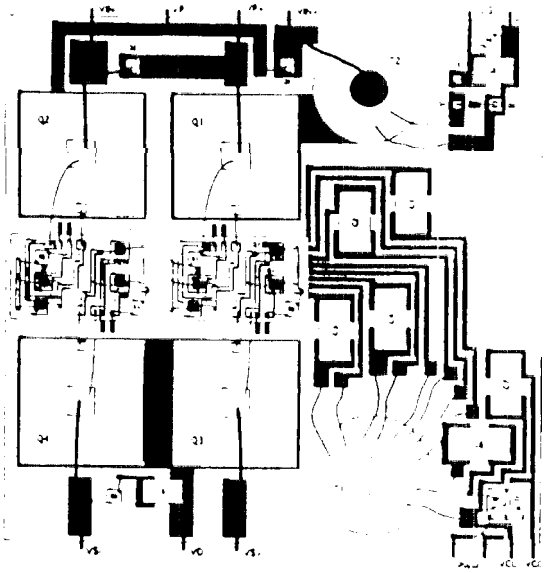

Figure 9. Hybrid Implimentation Layout

5. CONCLUSIONS

1. Efficiencies of up to 93% at an output of 30W at 5V_{dc} are attainable over temperature range, including control losses

2. All four topologies of de-de conveners using synch ronous rectification showed an efficiency chat was higher than the efficiency of converters using Schottky diodes. However, mass, volume, parts count and development cost make the implementation of synchronous rectification using discrete components less attractive compared to its hybridized implementation.

3. Careful selection of components for minimum total loss and maximum conversion efficiency is essential for synchronous rectification. Therefore, attempts must be made to select components which result in minimum 10ss several qualitative observations can be made from equation (11): (1) losses increase linearly with RMS current (2) losses increase with peak reverse voltage, and *(3) losses* increase linearly wuh the FET voltage rating.

4. It is concluded Lhal if the ultimate objective is to achieve Lhe highest possible efficiency, then the entire power stage should be built as a hybrid umt. This would reduce parasitic inductances and resistances and allow for externally driven synchronous rectifiers to be used without concern for chc overall circuit complexity.

5. The major disadvantage of the two-terminal synchronous rectifier is that it is inherently less efficient than an externally driven synchronous rectifier with the implementation used.

6. No-load operation with selected synchronous rectification configurations is possible.

6. ACKNOWLEDGMENTS

The work described in this paper was performed by the Jet propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

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