A Magnetic Solid-State Storage Technology: Vertical Bloch Line Storage

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No storage technology is known to exist today which simultaneously offers high storage density, nonvolatility, and a solid-state form factor. For example, common random access memories are solid-state, but are volatile and typically offer modest density. Alternatively, mainstream magnetic disk and magnetic tape systems offer high storage density and nonvolatility, but are fundamentally not solid-state.

A number of applications exist which would be suited well with high-performance solid-state technology. NASA, for example, is beginning to baseline solid-state recorders for upcoming space missions, such as the Cassini mission to Saturn. Solid-state storage is seen to offer advantages of lifetime, data access, and data management, for example, over tape storage, in which tape passage, whether for supporting on-board processing, accessing fragmented data records, or recording or reading data, becomes a life-limiting consumable. Second, rapidly accessible and indefatigable solid-state storage would be extremely useful for reducing data flow bottlenecks by providing local high-density storage within each node in multiprocessor computers. Third, portable laptop and palmtop computers serve as high-volume applications which would be served well by robust, high-density, solid-state storage modules. It is the existence of these types of applications which serves to motivate the investigation of high density, nonvolatile, and solid-state storage technology with no material fatigue, no cyclability limits, and favorable cost performance. These features also serve to motivate the investigation of Vertical Bloch Line (VBL) storage technology.

VBL storage technology is a block access storage technology, as shown schematically in Figure 1. The storage area is created from arrays of magnetic domain walls which are formed using arrays of magnetic domains in magnetic garnets. Bit cells are also defined, for example, by

creating a periodic magnetic field induced by the fringing fields from magnetized bars of hard magnetic material. As shown in Figure 2, the magnetic domain width, S_w, and the lithographic feature size, L_f, define the storage density limits for VBL technology. At present, a VBL chip is envisioned which would be fabricated using a thin-film lithography process which includes three ion implantation steps, four conducting metal layers with insulators, and two magnetic material layers. While deposition and patterning are required, no diffusion is required.

Electronic access to the data, for writing and readback, occurs in a VBL chip at the ends of the magnetic domain arrays. Write and read gates are placed at the ends of the magnetic domain arrays. Data input and output are performed using a current-access major line supplied by a magnetic bubble nucleator and a magnetoresistive output detector, respectively. In VBL technology, the presence or absence of pairs of VBLs are used to store information. VBL pairs are used as the datum since pairs are always induced topologically, and since a VBL pair is stabilized through a balance between exchange and magnetostatic energies. To support data access, VBL bits are propagated around the magnetic domains gyrotropically using a pulsed field from an integrated conductor.

Planned performance goals for VBL technology include storage capacities of 256 Mbits per chip; volumetric storage densities of 2 Gbits/cm^3 and 300 Gbit/kg in high density packaging; and power consumption levels of 10 mW per Mbit/sec for input/output, and 90 mW per active chip during bit propagation. The key issues being addressed at this time include demonstration of all critical functions in a single chip at a single operating point, and measurement of chip operating margins and error rates.

Figure 1. A schematic areal layout of a VBL chip.
Figure 2. VBL technology storage density calculations.

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A VBL Memory Architecture

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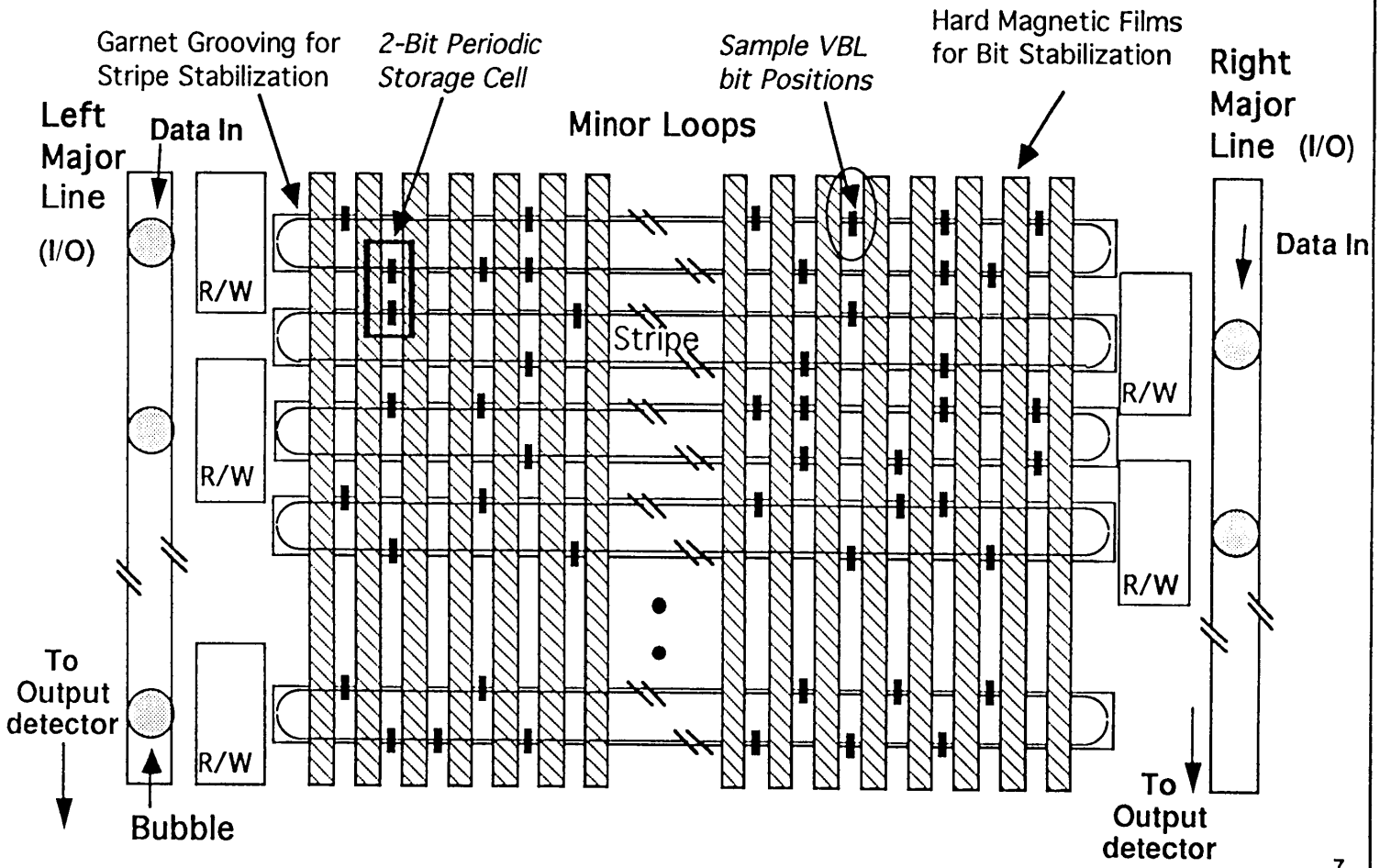

Fig 1

VBL Memory
Storage Density Performance

	Lf = 1 μm	Lf = 0.5 μm	Lf = 0.1 μm
Sw = 5 μm	10 Mbits/cm2	20 Mbits/cm2	100 Mbits/cm2
Sw = 2 μm	25 Mbits/cm2	50 Mbits/cm2	250 Mbits/cm2
Sw = 1 μm	50 Mbits/cm2	100 Mbits/cm2	500 Mbits/cm2
Sw = 0.5 μm	100 Mbits/cm2	200 Mbits/cm2	1,000 Mbits/cm2
Sw = 0.25 μm	200 Mbits/cm2	400 Mbits/cm2	2,000 Mbits/cm2

VBL Memory storage density is proportional to:

$$\frac{0.5}{(Sw) \times (Lf)}$$

Stripe:

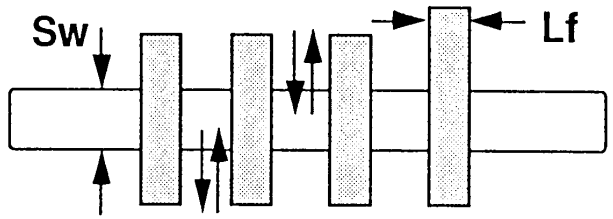

Fig 2