Design of a Low-Light-Level image Sensor with On-Chip Sigma-Delta Analog-to-Digital Conversion

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ABSTRACT

The design and projected performance of a low-light-level active-pixel-sensor (APS) chip with semi-parallel analog-to-digital (A/D) conversion is presented. The individual elements have been fabricated and tested using MOSIS* 2 pm CMOS technology, although the integrated system has not yet been fabricated, The imager consists of a 128x128 array of active pixels at a 50 μm pitch. Each column of pixels shares a 10-bit A/D converter based on first-order oversampled sigma-delta (Σ-Δ) modulation, The 10-bit outputs of each converter are multiplexed and read out through a single set of outputs. A semi-parallel architecture is chosen 10 achieve 30 fran~cs/second operation even at low light levels. The sensor is designed for less than 12 e⁻ rms noise performance.

1. INTRODUCTION

On-chip analog-to-digital (A/D) conversion can be used to improve sensor performance by minimizing read out noise introduced in transmitting analog signals off the focal plane. A focal-plane A/D converter has to be robust, Iow-power and compact. The architecture chosen to implement f6cal-plane A/D conversion for Iowlight-level imaging is a semi-parallel approach using first-order sigma-delta modulation and an array of active pixel sensors (Fig. 1).

The semi-parallel architecture was chosen as a trade-off between a serial system with a single A/D converter and a completely parallel system with an A/D converter for each pixel. A major disadvantage of the serial system is that it requires high operating speeds since conversion of each pixel must be done sequentially. This in turn introduces resolution problems due to the limited accuracy attainable at high conversion rates. On the other hand, a completely parallel system reduces the required operating speed but requires too much area to be included in each pixel. With a semi-parallel architecture, where an entire column of pixels shares a single A/D converter, the area available for each converter is limited mostly by the pixel pitch, and the number of conversions is proportional to the number of rows rather than the total number of pixels,
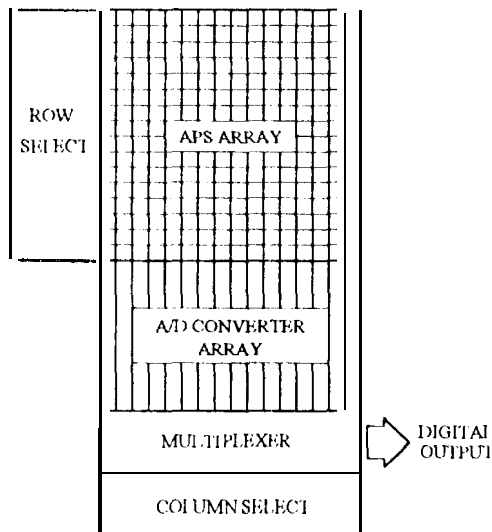
A/D conversion based on oversampled sigma-delta (Σ-Δ) modulation was selected since it has been proven to be well suited for VLSI applications where high conversion rate is not a requirement[1]. Due to the averaging nature of sigma-delta modulation, it is more robust against threshold variations and inadvertent comparator triggering than single-slopddual-slope methods and requires less component accuracy than successive approximation methods. It also uses less power and real estate than flash A/D converters. A semi-parallel architecture with an array of A/D converters reduces the conversion rate of each converter sufficiently to allow the use of sigma-delta modulation. Sigma-delta modulation is suitable for VLSI circuits since it is easier to achieve high oversampling ratios than to produce precise analog components in order to reduce component mismatch,

Figure 1: Semi-parallel architecture for focal plane A/D conversion.

in this design, q_n is averaged over 1024 samples by counting the number of" 1 "s using a 10-bit ripple counter. The block diagram for this system is shown in Fig. 3.
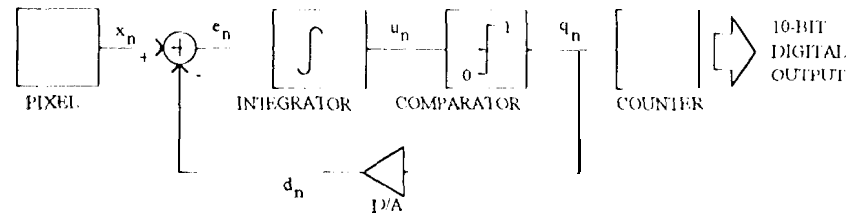

Figure 3: Block diagram of A/D converter.

2.2 Quantization noise in sigma-delta modulation

Quantization noise in sigma-delta modulation depends on the order of the modulator as well as the type of filter used to decimate the signal. in [1], the rms noise in the signal band in a first-order sigma-delta modulator with a busy input is expressed as

$$n_0 = e_{rms} \frac{\pi}{\sqrt{3}} (OSR)^{-3/2} \tag{2,2}$$

where OSR is the oversampling ratio defined as the ratio between the sampling frequency and the Nyquist frequency of the input signal. This derivation assumes that the quantization noise can be represented by an additive white noise source with equal probability of lying in the range $\pm \frac{\Delta}{2}$, and rms value $e_{rms} = \frac{\Delta}{\sqrt{12}}$. The average signal-to-noise ratio is then predicted as

$$\frac{A}{n_0} = \frac{6}{\pi} (OSR)^{3/2} \tag{2.3}$$

which improves by 1.S bits for each doubling of the oversampling ratio. When the output signal is averaged over each Nyquist interval, the noise in the signal band is

$$n_0 = \sqrt{2} e_{rms} (OSR)^{-1}$$

and the average signal-to-noise ratio is

$$\frac{\Delta}{n_0} = \sqrt{6} (OSR) \tag{2,4}$$

which corresponds 10 approximately 9.5 bits of accuracy for an oversampling ratio of 1024. Although a constant input dots not satisfy the assumptions made in the derivation in [1], it has been shown in [5] that the results may still hold.

Quantization noise in a tirsl-order sigma-delta modulator with a constant input is also highly dependent on the input level [1]. Analysis of such pattern noise can be found in references [1], [5] and [6].

3. DESIGN

3.1 Architecture

The chip consists of an imaging area, an array of A/D converters with multiplexed outputs, and control circuits for row and column selection as shown in Fig. 1. The imaging area is a 128x128 array of active pixel sensors which is scanned row by row. The row-control circuits decode the 7-bit row-address and provide the clock signals needed by each row of pixels. Each column of pixels shares a single A/D converter and the array of converters operate in parallel to convert a row of pixel outputs, Each A/D converter consists of a first-order oversampled sigma-delta modulator w'hose output is averaged by a 10-bit counter. The counter outputs are latched at the end of each conversion period and read out while the next row is being converted. The column control circuit decodes the 7-bit column address for the readout operation.

The integrator has two input branches, one 10 add the signal and the other to subtract the fall scale, P-type MOSFET switches arc used since they show less leakage than N-type switches, MOS capacitors which arc controlled by complementary clock signals arc included in the signal path to reduce switch feed-through, The switched-capacitors C_{sig} and C_{ref}, and the integrating capacitor C_{int} should bc large to minimize kTC noise but the size is limited mainly by the ability of the source-follolver to drive them at the oversampling rate and the available area under each column of pixels. Therefore, all the capacitors arc designed to bc poly1-poly2 capacitors of 1pF

The control signals ϕ_1 and ϕ_2 arc two non-overlapping clocks that read the two signal levels of the pixel output. Clock ϕ_v is synchronous with ϕ_2, and is generated from the output of the comparator so that it's on only when the comparator output is " 1". During each cycle, the amplitude of the modulated signal (A V_{sig}) is integrated across C_{int} in addition, when the comparator output is "1", the maximum signal swing (ΔV_{max}) is subtracted from the integrator output. A reset switch is included across the feedback capacitor to reset the integrator at the beginning of each pixel conversion, If it is assumed that the op amp and the switches arc ideal, the difference equation describing this operation for the n-th cycle can be written as

$$V_{out_n} = V_{out_{n-}} \mathbf{1} + \frac{C_{sig}}{C_{int}} \Delta V_{sig_n} - \frac{C_{ref}}{C_{int}} V_{q_{n-1}}$$

where V_q is O when q is "O" and V_q is ΔV_{max} when q is "1",
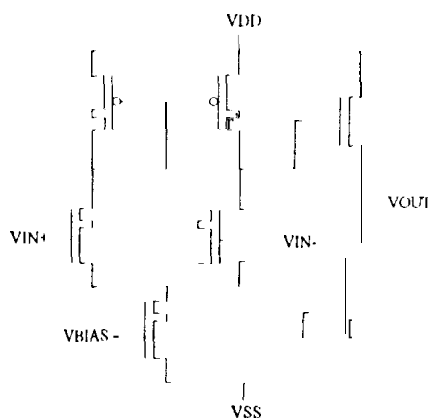

Figure 7: Op amp circuit

The op amp is implemented with self-cascoding transistors (SCFETs) [7] as shown in Fig, 7 in order to increase the gain of the input differential stage. The second stage consists of a source-follower to ensure single-pcrlc frequency response without the addition of a compensation capacitor.

The quantizer is a strobed comparator (Fig.8) whose inputs arc the integrator output and the reference level correc.spending to the full scale of the input. When the inputs are ready for comparison, the strobe signal is turned on, and the output is latched after it is allowed to settle. When the comparison is completed, the strobe signal is turned off to make the comparator idle and thus reduce power consumption.

The latched output of the comparator is used to generate the clock signal ϕ_v and its complement for the next integration cycle as shown in Figs, 6 and 9. It is also used to generate the two non-overlapping clocks required as inputs to the counter.
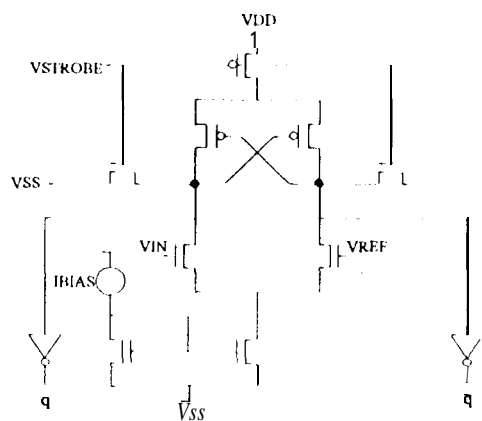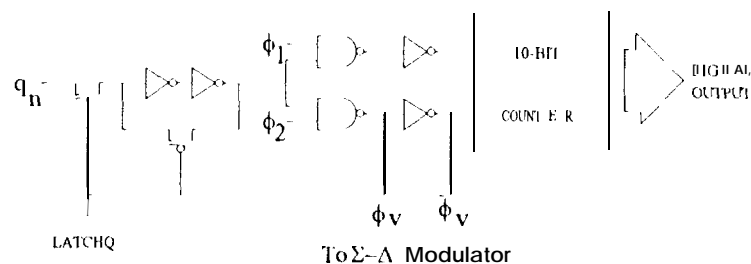

Figure 8: Strobed comparator circuit

Fig. 9: Logic circuit for feedback control and counter inputs

noise in each branch of the switched-capacitors can be expressed in input referred noise electrons as

$$\langle n_{sc} \rangle = \frac{1}{S} \sqrt{\frac{kT}{C}}$$

(4,3)

where S is the sensitivity of the APS unit cell given in equation (3.1), k is Boltzman's constant, and T is temperature. Table 1 summarizes these contributions in input referred rms noise electrons, The largest noise component is op amp white noise due to the large bandwidth needed for the high oversampling ratio. However, oversampling reduces the white noise and kTC noise components by the. square root of the number of samples taken.

4.3 Effects of op amp non-idealities

The transfer function of the integrator in the sigma-delta modulator with ideal components can be expressed as

$$H(z) = \frac{C_1}{C_2} \frac{z^{-1/2}}{1 - z^{-1}}$$

(4.4)

where C_1 and C_2 are the capacitors in the forward and feedback paths respectively. However, non-idealities of circuit components modify this expression and the actual transfer function includes a combination of these effects. The effects of finite op amp gain, limited op amp bandwidth and non-zero switch resistance are summarized in table 2

Table 2: Effects of op amp non-idealities

NON-IDEALITY	TRANSFER FUNCTION	EFFECT
Ideal transfer function	$H(z) = \frac{C_1}{C_2} \frac{z^{-1/2}}{1 - z^{-1}}$	Ideal behavior —
-Finite op amp gain	$H(z) = \frac{C_1}{C_2} \frac{(1 - 1/A - AC_1/C_2) z^{-1/2}}{1 - (1 - C_1/C_2 - 1/A)z^{-1}}$	Non-1 inearity
Limited op amp bandwidth	$H(z) = \frac{C_1}{C_2} \frac{z^{-1/2}\left[(1-\varepsilon) + z^{-1}\varepsilon\left(\frac{1}{C_1/C_2 + 1}\right)\right]}{1 - z^{-1}}$ where $\varepsilon = e^{-BT_s}$	Limits oversampling rate —
Non-zero switch resistance	$H(z) = \frac{C_1}{C_2} \frac{z^{-1/2}\left[1 - 2e^{-T_s/4R_{on}C_1}\right]}{1 - z^{-1}}$	Negligible effect

The most important of these is these effects is finite op amp gain since it affects the poles of the transfer function. It introduces a non-linearity due to damped integration as a result of the attenuation in the feed-back path. This effect was simulated for op amp gains of 300 and 3000, using the modified recursive relation

$$u_n = \alpha u_{n-1} - \beta(x_n - q_{n-1})$$

(4.5)

where a depends on the op amp gain and takes on a value less than 1, The simulation was carried out for constant inputs from 0 to full scale in integer multiples of the least significant bit (which is 1/1024th of full scale). The simulation involved integration over 1024 cycles and the output was defined as the number of " 1 "s in that output stream, The error plotted in
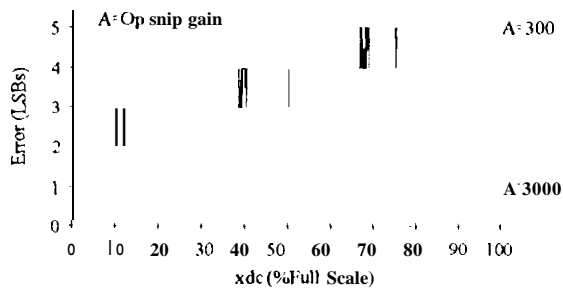
Figure 11: Effect of finite op amp gain vs. d.c. input

Fig. 11 is expressed as the difference between the output with damped integration and the output of the ideal integrator that has no damping. By choosing an op amp gain at least as high as the oversampling ratio, the effect of Finite gain can be limited to less than 3 dB [1].

The effects of limited op amp bandwidth and non-zero switch resistance are not as crucial as the effect of op amp gain since they change only the zeros of the transfer function and not the poles which affect stability of the sigma-delta modulator,

S. CONCLUSIONS

The design of a focal-plane A/D converter based on first order sigma-delta modulation has been presented. The predicted performance of the system in terms of speed of operation and noise is currently limited by the op amp. Improvements for future designs include an optimized op amp design and improved sensitivity of the active-pixel-sensor for better noise performance. Current research includes testing discrete sigma-delta modulator circuits, active-pixel-sensor designs and a 28x28 APS array which have been fabricated through the MOSIS foundry service. Future work will include improvements of the current design and integration into a full sensor.

6. ACKNOWLEDGMENTS

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* MOSIS is the MOS Implementation Service provided by DARPA and managed by USC's information Sciences Institute. The service provides quick turnaround, low cost foundry access to CMOS processing,