The Design and Implementation of NASA's Advanced Flight Computing Module

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1. Introduction

Driven by the economic reality of a declining fiscal budget and the favorable atmosphere for international collaboration and cost-sharing, NASA's deep space exploration program is moving away from the (several) billion dollar flagship missions, towards a series of small low-cost missions driven by focused science objectives as well as advanced technology validation. By launching several missions a year, rather than once a decade, the new approach will lead to the more cost-effective exploration of space by enabling the more frequent re-use of both hardware and software resources, as well as the faster insertion of new technology. The following programs are currently under development or under study:

Mars Exploration Program. A series of missions to the red planet include: the Mars Pathfinder mission in 1996 which will demonstrate a low-cost entry, descent and landing approach using parachutes and air-bags. It also carries a small 7 kg robotic vehicle called the microrover which will perform a number of technology experiments. This will be followed by a series of Mars Orbitters and landers that will then allow for the global exploration of Mars.

The Discovery Program, Starting in 1996, the Discovery program represents a series of low-cost scientific missions with a cost cap of 150 M$ and two launches every two years. Currently, over a dozen Discovery missions are under study.

The Pluto Fast Flyby Mission. With a project start planned in 1997 and a launch in 2001, the mission to planet Pluto and its moon Charon is currently under study at JPL.

in common to all of the above missions is the strong demand for the reduction in the system mass, volume, and power. It is within this context that NASA is currently funding the Advanced Flight Computing program at JPL, described in the following section.

2. NASA's Advanced Flight Computing Program

The Advanced Flight Computing (pre)program at JPL started in fiscal year 1993 with a small seed effort designated for planning purposes. During this period, JPL hosted several workshops with industry and academia, for the purpose of identifying the key enabling flight computing technologies for future small and low-cost planetary missions. The number one priority was given to the accelerated insertion of advanced packaging technology such as Multichip Modules (MCM) and 3D die stacking. Other technologies of high priority included: low-power and low-voltage VLSI technology; standardization of interfaces based on commercial practice; fault-tolerant embedded computing; software re-use, etc.

2.1 MESUR Network Case Study

During this same year of planning, the Mars Environmental Survey (MESUR) project[1] sponsored a study to determine whether the total mass of the spacecraft electronics of the 1996 Mars Pathfinder lander can be reduced by a factor of three, using advanced technology. As shown in Figure 1, the study showed in detail how the mass was reduced from a total of 42 kg to less than 11 kg. Moreover, this mass reduction had a further ripple effect to reduce the total spacecraft mass from 450 kg to 250kg. These results helped further focus the AFC program which began in FY 94. The key packaging technology that was extensively applied consisted of Multichip Modules, 3D die stacks for memory only, and 3D Multichip Module stacking.

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[1] The Mars Environmental Survey (MESUR) project has been renamed the Mars Pathfinder project. At that time, the MESUR Network program envisioned the distribution of up to 16 science stations on Mars.

2.2 AFC Program Outline

The AFC program was defined as a three year effort which started in FY 94 with a budget of 750K$ and a lot of enthusiasm. The planned budget for the following two years was 1.2 M$ in FY95, and 1.6M$ in FY96. The funding profile also included a space flight demo in FY96. The program proposes the development of three MCM building block modules that will then be slacked into a 3D MCM configuration. The first MCM to be built in FY 94 is the Flight Computer MCM. The other two MCMS arc the Mass Memory MCM using 3D die stacks, and the programmable I/O MCM for science payload as well as spacecraft engineering interface. The three module MCM stack is depicted in Figure 2. The focus of this paper is on the first MCM, that is the Night Computer module.

3. Flight Computer MCM

Before we describe the flight computer MCM in detail, it is important to emphasize that one of the main objectives of the AFC program was to work very closely with industry in a teaming arrangement that would be of mutual interest. This t taming arrangement was established with TRW Corporation using JPL's Technology Affiliates Program (TAP). The collaboration consists of a well planned and coordinated effort funded jointly by the AFC program and TRW's IRAD MCM IRAD program, and without the exchange of funds. The net effect is that both institutions receive the benefit of the sum total of the two int ernal research programs.

3.1 Flight Computer Architecture

As a result of this teaming arrangement, and as a result of numerous joint technical discussions, a flight computer architecture was finalized by April 1st 1994. As shown in Figure 3, the flight computer MCM was defined to consist of the following four partitions:

1. Core CPU set, which consists of the RH-32 RISC CPU and two Memory Management Units (MMU). The RH-32 chip set also includes the FPU and the System Control Unit (SCU).
2. Local Memory, which consists of 2.5 MB of SRAM slacked in a 3D configuration.
3. Non Volatile Memory, using EEPROM for system boot, operating system support and programmable logic configuration.
4. Field Programmable Logic, consists of 4 Xilinx 3090 FPGAs that implement the memory decode, interrupt control, timers, and other auxiliary flight computer support logic.

To demonstrate the flight computer h4CM in a spacecraft configuration, the plan called for the design to be open or compatible with any inter-moclulc interface. We have chosen to demonstrate the module on a VME board, since this configuration is supported by the JPL Flight System Testbed and is used by the Mars Pathfinder Attitude and information Management Subsystem (AIMS). The current plan is to also support the VxWorks real-lime operating system, and a C programming language development environment.

3.2 Flight Compute r MCM Technology

From the very start of the AFC program, the choice of the packaging technology was of crucial importance and was one of the essential deliverables. Both MCM technology and 3D memory technology were to be combined within the first module. The choice of nCHIP MCM technology was made after a lengthy study of several different technologies and MCM vendors. The following issues were instrumental in reaching this decision:

1. Based on reliability test results obtained from NASA's RELTECH program, the nCHIP MCM technology was evaluated as a robust process that can sustain a space environment.
2. The nCHIP MCM technology based on a Si substrate, Si02 dielectric and Al metal allows for high degrees of interconnect complexity in two signal layers.
3. The usc of the decoupling capacitor between the power and the ground plane allowed for the reduction in the total number of components, and the more cost effective usc of MCM real-estate.
4. nCHIP was willing to commit to a very aggressive schedule that would deliver two functional MCMS to JPL and TRW by November 1994.

Given the number of flight computer components that are integrated into the MCM a total substrate size of approximately 2 by 4 inches was chosen.

3,3 **Flight Computer** Packaging Technology

The package chosen for the nCHIP substrate is the 438 pin ·AlN package from Coors. Even though this package is more expensive than alternative alumina packages, the choice of AIN was made to better match the thermal properties of Si. Since we are dealing with a relatively large MCM substrate, any approach to further reduce the potential build-up of thermal or other stress, was taken into account. The total mass of the package with substrate and dic is less than 100 grams (89 grams), which represents more than an order of magnitude reduction in mass relative to more traditional SMT space qualified technology. Moreover, the volume of the single MCM flight computer module is lcss than 1.5 cubic inches, which is extremely attractive for most of the upcoming NASA planetary missions.

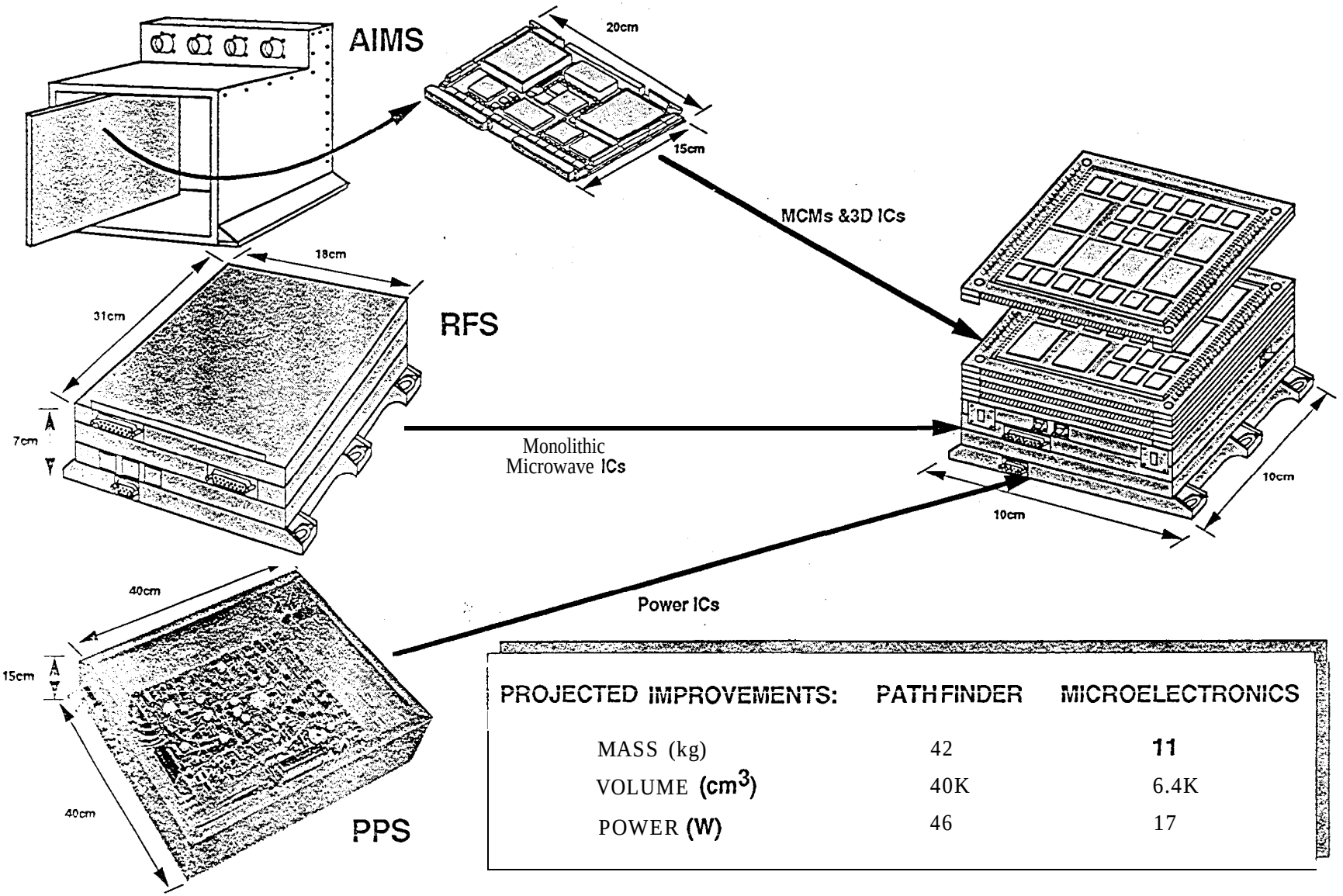
4. Summary

This paper describes a working flight computer Multichip Module developed jointly by JPL and TRW under their respective research programs in a collaborative fashion. The MCM is fabricated by nCH IP and is packaged within a 2 by 4 inch Al package from Coors. This flight computer module is one of three modules under development by NASA's Advanced Flight Computer (AFC) program. Further development of the Mass Memory and the Programmable 1/0 MCM modules will follow. The three building block modules will then bc stacked into a 3D MCM configuration. The mass and volume of the flight computer MCM achieved at 89 grams and 1.5 cubic inches respectively, represent a major enabling technology for future deep space as well as commercial remote sensing applications.

AFC INTEGRATED MICROELECTRONICS APPROACH

MARS PATHFINDER

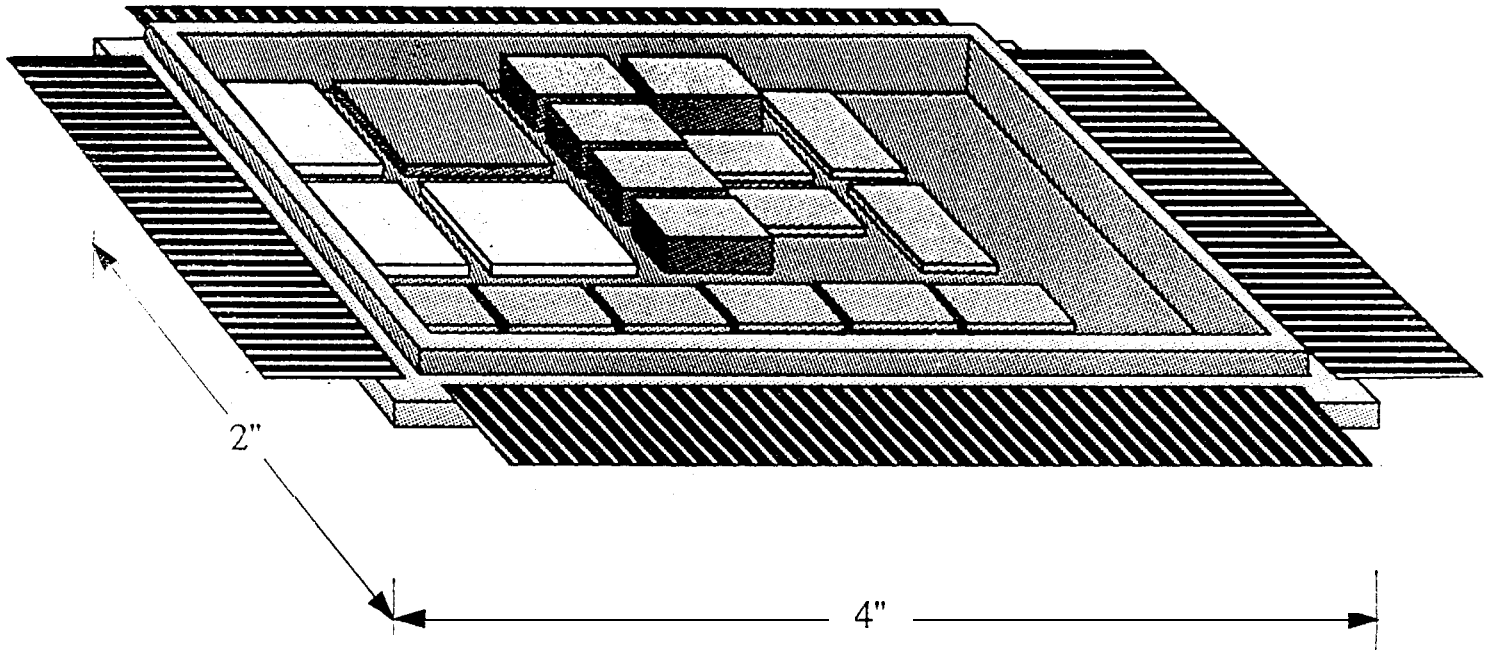
AFC MICROELECTRONICS



PROJECTED IMPROVEMENTS:	PATHFINDER	MICROELECTRONICS
MASS (kg)	42	11
VOLUME (cm^3)	40K	6.4K
POWER (W)	46	17

JPL

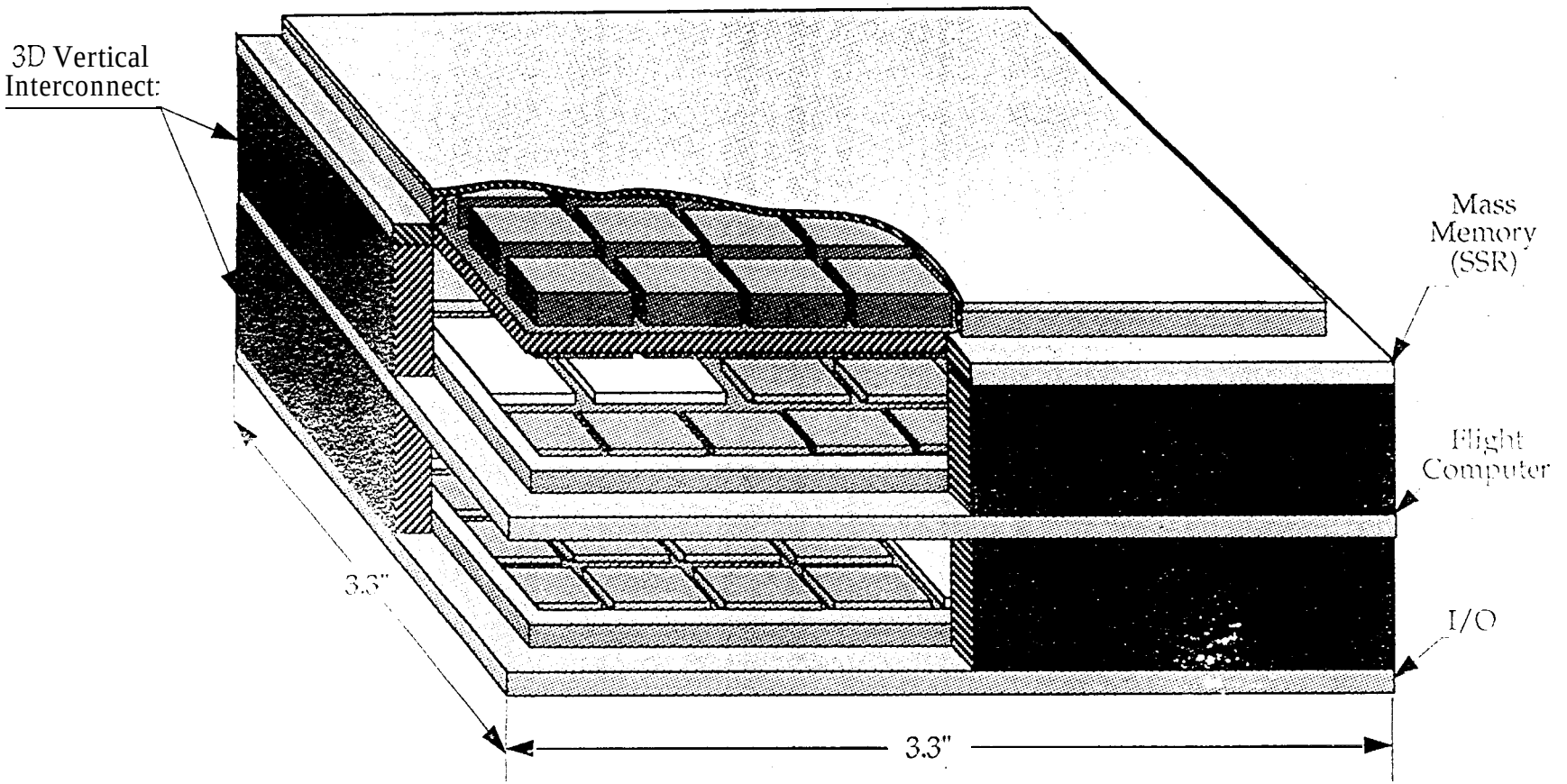
AFC Development Model



CPU
FPU
MMU
SRAM
EEPROM
XILINX

Performance	Packaging
RH-32 RISC CPU Set	MCM Substrate: Si
2.5 MB SRAM Using 3D Stacks	Vendor: nCHIP
512 KB EEPROM	Die Interconnect: Wire-bond
4 Xilinx 3090 FPGA	Package: AlN from Coors
Mass = 100 grams Volume = 1.5 cubic inches Power = 12 watts at 20 MHz (peak)	Pin Count: 438

AFC 3D MCM Stack for Integrated S/C Electronics



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