INTEGRATED BACK-TO-BACK BARRIER-N-N+ VARACTOR DIODE TRIPLER USING A SPLIT-WAVEGUIDE BLOCK

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ABSTRACT

The back-to-back barrier-N-N^+ (bbBNN) varactor is a nonlinear device being developed for frequency multiplier applications above 100 GHz. Its symmetrical C-V characteristic, low series resistance and suitability to planarization make it ideal choice for high frequency, low power, odd harmonic generation.

In this paper, development of an integrated planar multiplier device and its the performance as a 220 GHz tripler is presented. A new split-

waveguide block design has been used to provide the proper embedding impedances to the device. The performance over 200-240 GHz has been measured and the integrated bbBNN device is shown to provide as much as 734 microwatt output power. A flange-to-flange tripling efficiency of 7'% has been obtained. This is believed to be the highest conversion efficiency yet reported for all planar tripler at this frequency. The performance is expected to be improved further with minor changes to the device and circuit parameters.

1. INTRODUCTION

The submillimeter-wave range of the spectrum holds enormous promise for spectral line studies of the interstellar medium, distant galaxies, solar system and earth remote sensing. To achieve the high sensitivity and spectral resolution requirements of observatory and exploratory space missions, submillimeter-wave heterodyne radiometers are being developed [1 ,2]. One of the least developed technologies for submillimeter-wave heterodyne radiometry is the local oscillator source. Candidate technologies include harmonic generators, such as frequency multipliers pumped by millimeter-wave fundamental sources. Although the whisker contacted Schottky varactor diodes have proven very effective, there remains great interest in developing mechanically robust, planar device technologies which are capable of operating well into the submillimeter wavelength range and have the potential to deliver sufficient amounts of power [3]. To minimize the risk of failure, a planar device technology is preferred for space applications. The goal of our work is to demonstrate that planar devices can replace whisker contacted devices without degrading performance.

One such candidate for THz frequency space applications is the planar back-to-back barrier-n-n$^+$(bbBNN) varactor diode [4,5,6,7]. The sharp C-V characteristic of this device allows for high multiplication efficiency at low input power levels. This is an advantage, particularly at THz frequencies, where the available input power is quite low. In addition, its symmetric C-V characteristic offers significant benefits for odd harmonic multiplier applications since the idler circuits at the even harmonics are not needed and loss at higher even harmonic frequencies is zero in the ideal case. So, a tripler circuit for this does not require a second harmonic termination. This device has a comparatively low series resistance and high cut-off frequency. It has low substrate parasitic as all non-essential semiconductor materials can be removed using a backside processing technique [8]. The structure has no ohmic contacts, thereby reducing a substantial parasitic series resistance. The device also exhibits very low leakage current. The dynamic cut-off frequency for a given device area can be increased to a higher value by the multiple barrier approach, which helps to reduce the device capacitances and to generate higher powers by distributing the pump power over several stacked devices. Although measurements on discrete planar bbBNN devices have been carried out earlier in a crossed waveguide mount [7], handling and mounting of the small discrete chips were very difficult. This motivated us to develop the technique to integrate RF microstrip filter circuitry with the planar bbBNN device [9].

Waveguide mounts can provide appropriate embedding impedances at the input and output frequencies to couple power in and out of a nonlinear device. in order to accommodate the necessary waveguide flanges and backshort tuning mechanisms, frequency multipliers commonly utilize a crossed waveguide design, Ease of fabrication and assembly, wide tunability of fundamental and harmonic embedding impedances and low loss are the

desirable aspects of the multifrequency, multiwaveguide mount designs. To avoid the fabrication complexity of the crossed waveguide block and to facilitate easy mounting of planar integrated devices, a split-waveguide block has been proposed recently [10], The present experiment has been carried out using this spiit-waveguide block.

The outline of the remaining portion of this paper is as follows: Section II describes the multiplier device, fabrication of the planar integrated device and its characterization. Section III presents the theoretical nonlinear simulation results of the device used in this experiment. Section IV gives the 220 GHz waveguide mount description of the tripler. The procedure and results of the tripler measurement are presented in section V and finally conclusions are given in section VI.

II INTEGRATED **bbBNN DEVICE**

The integrated bbBNN device used in this experiment was developed at the Microdevices Laboratory of JPL. Fig.1 shows the schematic diagram of a planar bbBNN varactor structure, integrated with a microstrip filter on a quartz substrate, The schematic also shows that the final circuit structure has only a small semiconductor mesa region. The cross-sectional view of the active area of the device is shown in Fig.2. The thinned wafer from the top surface down consists of, (i) a GaAs cap layer, (ii) a $Al_{0.45}Ga_{0.55}As$ barrier, (ii) a GaAs spacer followed by silicon planar doping, (iv) a moderately doped GaAs layer and (v) a highly doped GaAs layer. The layer thicknesses, compositions, number of barriers, device geometry and doping densities can be independently tailored to optimize performance for the desired operation frequency range. This

heterojunction barrier device does not require any DC bias as the operating point of the device is controlled by the sheet doping. Combinations of depletion layer dopings and planar doping sheets allow tailoring of the capacitance versus voltage characteristic. The maximum capacitance is obtained at zero bias, when both sides of the diode are in accumulation. When a bias is applied to this structure, one side of the barrier is depleted and the other side is accumulated. The resulting capacitance is the series combination of the barrier region and the two semiconductor regions, with most of the capacitance change occurring on one side of the barrier. Since the structure consists of two back-to-back diodes, the capacitance versus voltage characteristic is symmetric about zero bias. The minimum capacitance occurs when one diode is in accumulation and the other is fully depleted. The minimal parasitic series resistance introduced by the favorable geometry does not degrade with the skin effect, The highly doped GaAs region provides a low resistance path between the Schottky contacts.

a) Fabrication of integrated bbBNN varactor

The process we describe was designed so as to integrate the planar device with the microstrip filter circuitry and to eliminate all the GaAs on the final circuit structure except for the small active GaAs mesa region. It has been demonstrated that, pre-fabricated and thinned GaAs substrate devices can be transplanted on to quartz using UV cured optical cement [11]. However, this process leaves highly doped GaAs around the devices and under the distributed circuit elements, which can be detrimental to the RF performance. Again, conventional multiplier diode isolation techniques have a number of draw backs. Isolation implants are commonly used, but the removal of masking materials from

the wafer often present difficulties. An alternative technique for isolating active devices is to perform a mesa etch, but connection of the contacts to the top of the mesa is achieved generally using a planarization process. Our experiments have shown that, planarization process damages the thin barrier layer of the BNN wafer. Metal coverage may also be a problem. Air bridging can be used with mesa isolation, but this also exposes the top of the semiconductor material to a larger number of process steps.

The integration process presented here uses a backside processing technique [8] in which the front of the wafer is exposed to the minimum amount of processing possible. The salient process steps are shown in Fig.3 and summarized below. The GaAs wafer structure consists of a (i) a **2** nm thick GaAs cap layer, (ii) a 20 nm $Al_{0.45}Ga_{0.55}As$ barrier, (ii) a 3 nm GaAs spacer followed by 4x1012 cm-2 silicon planar doping, (iv) a 120 nm thick moderately doped GaAs layer (doping level = $1x10^{17}$ cm^{-3}) (v) a 1300 nm thick highly doped GaAs layer (doping level = $5x1\ 0^{18}$ cm^{-3}) and (vi) a 600 nm thick $Al_{0.45}Ga_{0.55}As$ etch stop layer grown by MBE on a 508 pm thick semi-insulating GaAs substrate.

To begin the process, Schottky contacts are defined by lift-off of e-beam evaporated Ti/Pt/Au. The wafer is then passivated with 1200Å of ECR deposited silicon nitride. Using reactive ion etching, windows in the nitride are opened over the metal contact pads away from the active area of the device. The wafer is then bonded face down to a 0.152 mm thick quartz substrate with a thin layer (approximately 5-10 µm) of commercially available UV curing optical adhesive (Norland type 61). The windows in the nitride allow the glue to adhere directly to the metal pads, which helps to prevent metal peeling during later probe testing and wire bonding of the devices. The quartz mounted wafer is first mechanically lapped to about 100 µm. The semiconductor substrate is further

thinned in a selective etch that removes the remaining bulk GaAs, stopping on the AlGaAs etch stop layer, Mesas are patterned from the backside of the wafer using an IR mask aligner. A dry etch containing BCl_3, Cl_2 and Ar removes all the non-essential semiconductor material surrounding the active area, thus isolating the devices and exposing the metal contact pads. After removal of the mesa photo resist, the backside is passivated with a second layer of silicon nitride and contact windows are opened by photolithography and reactive ion etching. The backside metal contact pads and subsequently the microstrip filter circuitry are defined using Cr/Au evaporation and lift-off techniques. Final filter structure has 1 pm thick gold to reduce skin effects.

Fig.4(a) shows the photograph of a completed and diced integrated hammerhead filter structure. Fig. 4(b) and Fig.4(c) shows close-up views of the device portion of the integrated filter from two sides of the quartz substrate. Fig, 4(b) shows the view from the filter side of the quartz. The backside of the device active mesa can be seen at the center of the photograph. Fig. 4(c) **shows** the close-up view of the device through the 0.152 mm thick transparent quartz substrate. Two 1 μm wide fingers at the center of this photograph define the Schottky contact area across the mesa top surface, and connect the device to the contact pads.

b) DC characterization of integrated devices

The integrated devices used in this experiment have a 8 μm^2 device area. The width of the GaAs mesa is 4 μm and the two metal contact fingers are 2 μm wide, separated by a 1.4 μm gap. The design parameters of the devices are evaluated using the approach of [12]. These are as follows:

maximum capacitance, C_{max} = 23 fF, C_{max}/C_{min} = 4.0, series resistance, R_s = 11 Ω, breakdown voltage, V_{br} = 22.3 V, dynamic cut-off frequency, f_{cd} =1.9 THz. DC characterization of the diodes, performed both before and after the diodes are mounted into the waveguide mount, are similar. Fig.5(a) and 5(b) show the current-voltage (I-V) and 1 MHz capacitance-voltage (C-V) characteristics of an 8 μm^2 device integrated with RF microstrip filter circuitry. From these measurements, a C_{max} = 24 fF, a C_{max}/C_{min} = 2.7 and a breakdown voltage of 6.5 volts are obtained. The disparity between the modeled and measured breakdown may be due to avalanching and edge effects.

III. THEORETICAL TRIPLER PERFORMANCE

Theoretically a varactor tripler is most effective when the diode is impedance matched at the fundamental and output frequencies and a lossless current flow is permitted at the second harmonic idler frequency. bbBNN varactors generates only odd harmonics due to its symmetric C-V characteristic and thereby does not need any second harmonic termination. The mount design thus becomes simpler, The efficiency of the tripler is dependent on the diode parameters, embedding impedances and input power levels. The bbBNN devices are operated at the zero bias voltage, the symmetry point of the C-V characteristic.

The performance of the bbBNN device used in this paper has been theoretically evaluated using a modified version of the large signal analysis program [13], which performs a full non-linear analysis of the Schottky barrier diode, having a frequency dependent series resistance and arbitrary C-V and I-V characteristics. For the present work, the program has been modified to

handle themeasured C-V and I-V characteristics of the bbBNN varactors, witha frequency dependent series resistance, The analysis uses the device C-V and I-V characteristics shown in Fig.5. The realistic evaluation is obtained by carrying out the large signal analysis under the pumped conditions, In this nonlinear device circuit simulation, frequencies other than input and output are short circuited, The input and output embedding impedances are optimized to find the best output efficiency.

Since the series resistance of the device is important in device performance, the calculations are carried out for a range of series resistances with a corresponding range of cut-off frequencies. Fig.6 presents the theoretical diode tripling efficiency versus input power of the integrated bbBNN varactor used in this experiment plotted for series resistance values of 10Ω, 15Ω and 20Ω. Higher device series resistances degrade the performance significantly.

Another output of the large signal analysis **used to optimize the device is the embedding impedance required to maximize the performance.** Fig. 7 shows the imaginary part versus real part optimum embedding impedance plots parameterized by input power. Impedances are plotted for different series resistance of the device. Optimized embedding impedance curves for the fundamental frequency (73.3 GHz) are presented in Fig.7(a) and those for the third harmonic frequency (220 GHz) are shown in Fig.7(b) respectively. The input power is varied from O to 40 mW. At low input power, the real part of the impedances are the same as the diode series resistance and the imaginary part of the impedances are 90 Ω at the input frequency and 30 Ω at the output frequency, corresponding to the maximum capacitance at zero bias. The device capacitance decreases as the input power increases, thereby increasing the imaginary embedding impedance. The minimum capacitance of 9 fF corresponds to 219 Ω at the input frequency and 80 Q at the output frequency. Therefore, for

optimum performance, the device needs real impedances in the range from 10-28 Ω at the input frequency and 10-33 Ω at the output frequency. The imaginary impedances needed are in the range from 90-185 Ω for the input circuit and from 30-75 Ω for the output circuit,

IV. MOUNT DESCRIPTION

A split-waveguide mount [1 O] has been used to provide the proper input and output embedding impedances to the integrated bbBNN device. This mount has been specially designed for planar devices integrated with filter tuning circuitry on a quartz substrate. Fig.8 shows a photograph of the lower half of the 220 GHz tripler mount. Two halves of the block are mirror images of each other and input and output rectangular waveguides are split along the E-field. The input power is coupled to the quartz microstrip RF' filter through a WR-12 E-plane arm. The bbBNN device is positioned at the center of the broadwall of a half height WR-4 waveguide (0.28 mm x 1.09 mm). A channel waveguide transformer [14] couples the output waveguide to standard WR-4 through an E-plane arm. The distances of the input and output E-plane waveguides from the microstrip filter are approximately $\lambda_{g,fundamental}/2$ and $\lambda_{g,third\text{-}harmonic}/2$ respectively. The mount has four sliding backshorts, two at the input side and two at the output side. The backshorts provide both a series and parallel stub at the input and output and help to achieve the maximum coupling. The filter channel is 0.36 mm wide and 0,31 mm high and it extends across and beyond the output tuner waveguide. This allows DC and RF grounding at the end of a microstrip filter instead of at the waveguide wall. The bias voltage can be applied to the

device through the bottom of the lower half of the block, via a SMA coaxial connector and a bias filter.

Fig.9 shows the schematic diagram of the filter section of the 220 GHz tripler mount. The integrated RF filter and the bias filter (Fig.9) help to achieve the signal separation. These microstrip hammerhead filters are fabricated on 0.33 mm wide and 0.152 mm thick fused quartz substrates, The bias filter and the RF filter are the three section hammerhead filters, similar to those presented in [15]. Fine tuning of the filter response was accomplished using the finite difference time domain (FDTD) method [16]. The bias filter rejects the 60-80 GHz input power. The RF filter passes the input frequency, but rejects the tripled output power, The filter on the far side of the output tuner waveguide presents a short circuit at the waveguide wall at the third harmonic frequency and presents a reactive termination, via a side stub, at the fundamental frequency.

Iv. RF PERFORMANCE

The tripler performance is measured using the technique described in [17]. Gunn oscillators are used as pump sources for the 66-80 GHz range of input frequencies, The device was biased at O volts during the measurements. The flange-to-flange efficiency of the bbBNN device with the C-V and I-V characteristics of Fig.5 is measured. The input power is monitored by an Anritsu power meter calibrated to give the power at the input flange. Input backshorts are tuned at each input power level to couple the maximum input power to the integrated device. The reflected power is monitored using a directional coupler coupled to a second power meter. The third harmonic output power is measured at the output flange of the waveguide mount using a third

power meter. Output series and parallel non-contacting backshorts are tuned at every frequency and power levels to achieve the maximum output power.

The tripler measurements for the integrated device are carried out over the frequency range of 200-240 GHz. The best performance was achieved at an output frequency of 217.5 GHz. Fig.10(a) shows the measured flange-to-flange tripling efficiency versus input power for the integrated bbBNN varactor in the split-waveguide mount. The flange-to-flange efficiency of the tripler reaches its maximum value of **7%** at **8.8** mW **input** power and then begins to decrease as the pump power level is increased. Fig. 10(b) shows the tripled output power versus input power for this device. A maximum output power of **734** μW **was measured for 14.3** mW **input power.**

Fig. 11 presents the measurement results over the 200-240 GHz output frequency range. Plotted are the flange-to-flange tripling efficiency **versus output frequency** curves for 5 mW, 8.8 mW and 12 mW input power **levels. Input impedance matching is easily obtained for these measurements, by slightly varying the positions of** the **input tuners.** But output impedance matching is difficult and changes with slight variation of input frequency and power levels.

V. CONCLUSION

The performance of a monolithically integrated planar bbBNN varactor structure as a frequency tripler has been presented. A device development process has been described which integrates the device with a larger tuning circuit on a quartz substrate. This planar structure is easily scalable to submillimeter wave frequencies and allows for more flexibility in the circuit

design. The integration of the filter structure with the varator diode eases handling and reduces assembly and test costs ,

A flange-to-flange tripling efficiency of 7% and a maximum output power of 734 μW have been measured for a integrated bbBNN device. A new 220 GHz split-waveguide mount, designed for planar devices, has been used for these measurement. The devices measured in this study had C_{max}/C_{min} = 2,7. Theoretical studies indicate thal increasing the C_{max}/C_{min} ratio will give better efficiency [12]. The performance should further improve with minor modifications of device and circuit parameters.

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FIGURE CAPTIONS

Fig.1 Schematic of a planar bbBNN varactor integrated with the microstrip filter structure on a fused quartz substrate

Fig.2 Semiconductor layer structure of the bbBNN device

Fig.3 The fabrication process steps for the integrated, planar GaAs bbBNN varactor device.

(a) MBE growth, (b) Schottky metallization, (c) Surface passivation, (d) Dielectric window opening, (e) Mounting on quartz, (f) Lapping and etching, (g) Mesa definition and removal of unwanted semiconductor substrate portions, (h) Backside passivation, (i) Contact vias, (j) Backside metal contacts, (k) Filter metal patterning

Fig.4(a) The photograph of a completed and diced integrated hammerhead filter structure.

Fig.4(b) Close-up view of the device portion of the integrated filter from the filter side of the quartz.

Fig.4(c) Close-up view of the integrated device through quartz substrate,

Fig.5 Measured (a) C-V and (b) I-V characteristics of a 8 μm^2 integrated bbBNN varactor.

Fig.6 Theoretical diode tripling efficiency to 220 GHz versus input power plot parameterized by the series resistance of the integrated bbBNN device.

Fig.7 Theoretical optimum embedding impedances for the integrated bbBNN varactor tripler to 220 GHz as a function of input power with different series resistances. (a) at 73,3 GHz; (b) at 220 GHz.

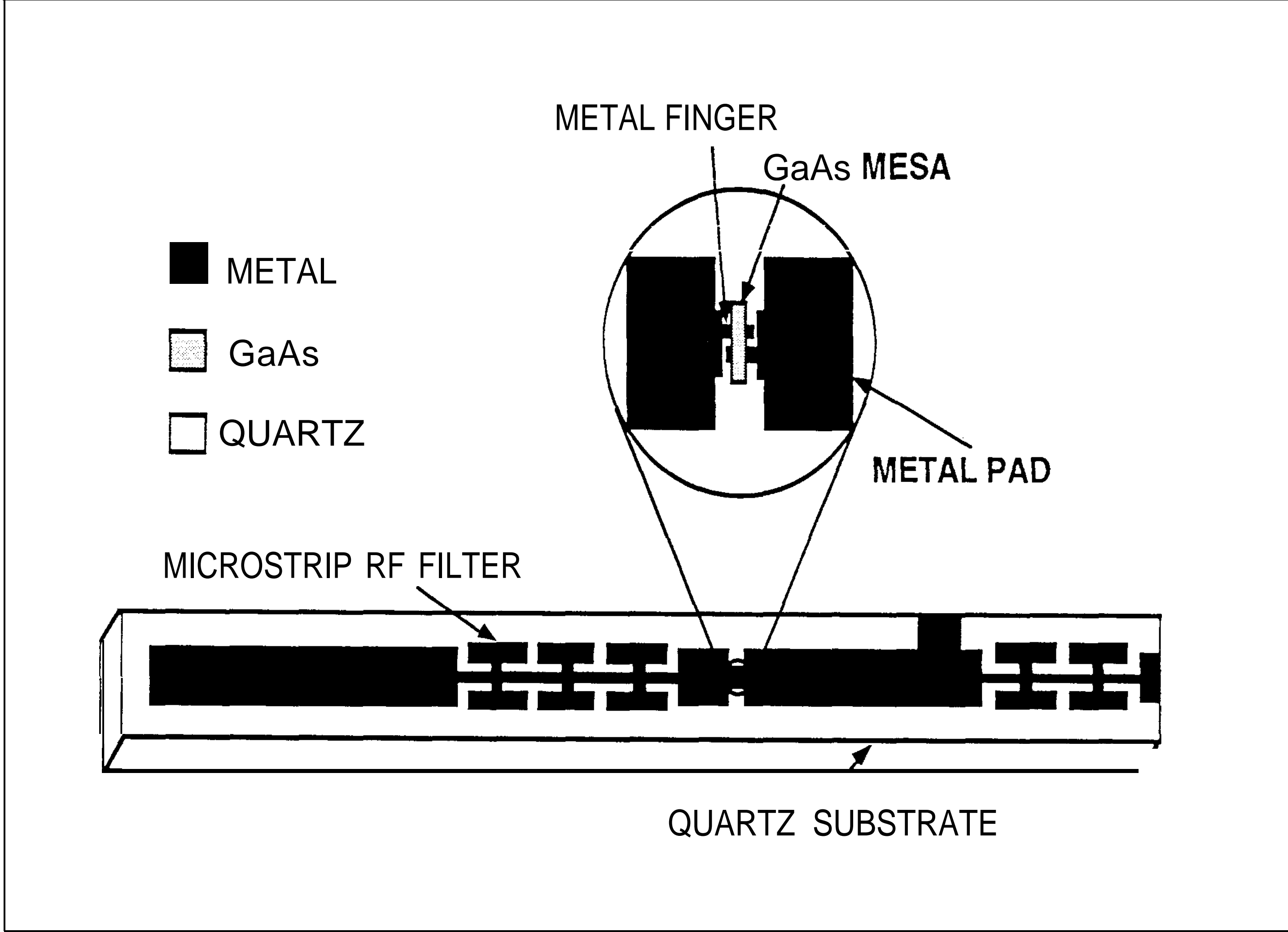
Fig.8 Photograph of the lower half of the 220 GHz split-waveguide tripler mount with the integrated bbBNN device.

Fig.9 Schematic diagram of the close-up view of the filter portion of the 220 GHz tripler mount.

Fig.10(a) **Measured flange-to-flange efficiency** versus input power plotted at 217,5 GHz.

Fig.10(b) Measured output power versus input power plotted at 217.5 GHz.

Fig.11 Measured flange-to-flange tripling efficiency versus output frequency power for 5 mW, 8.8 mW and 12 mW input power



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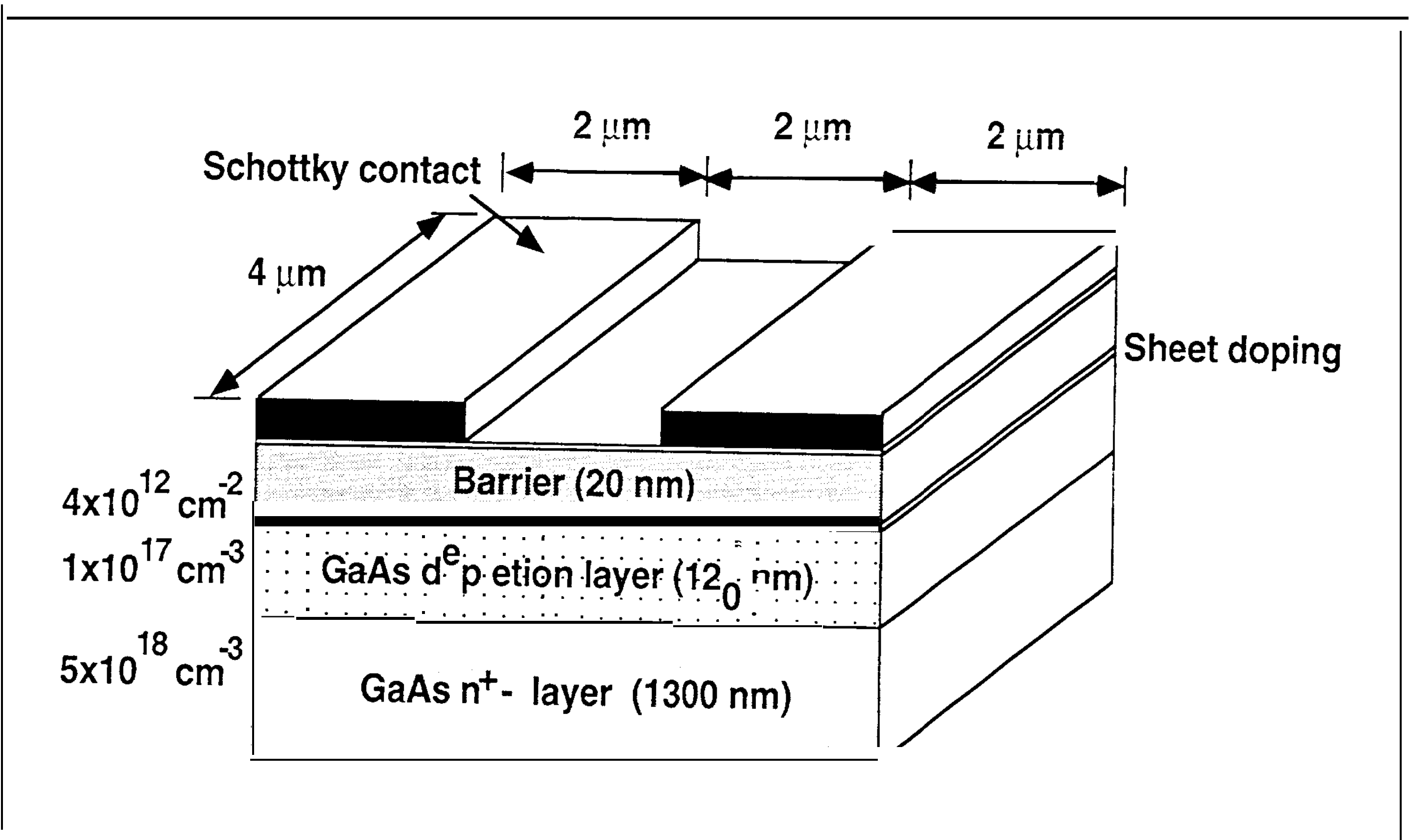

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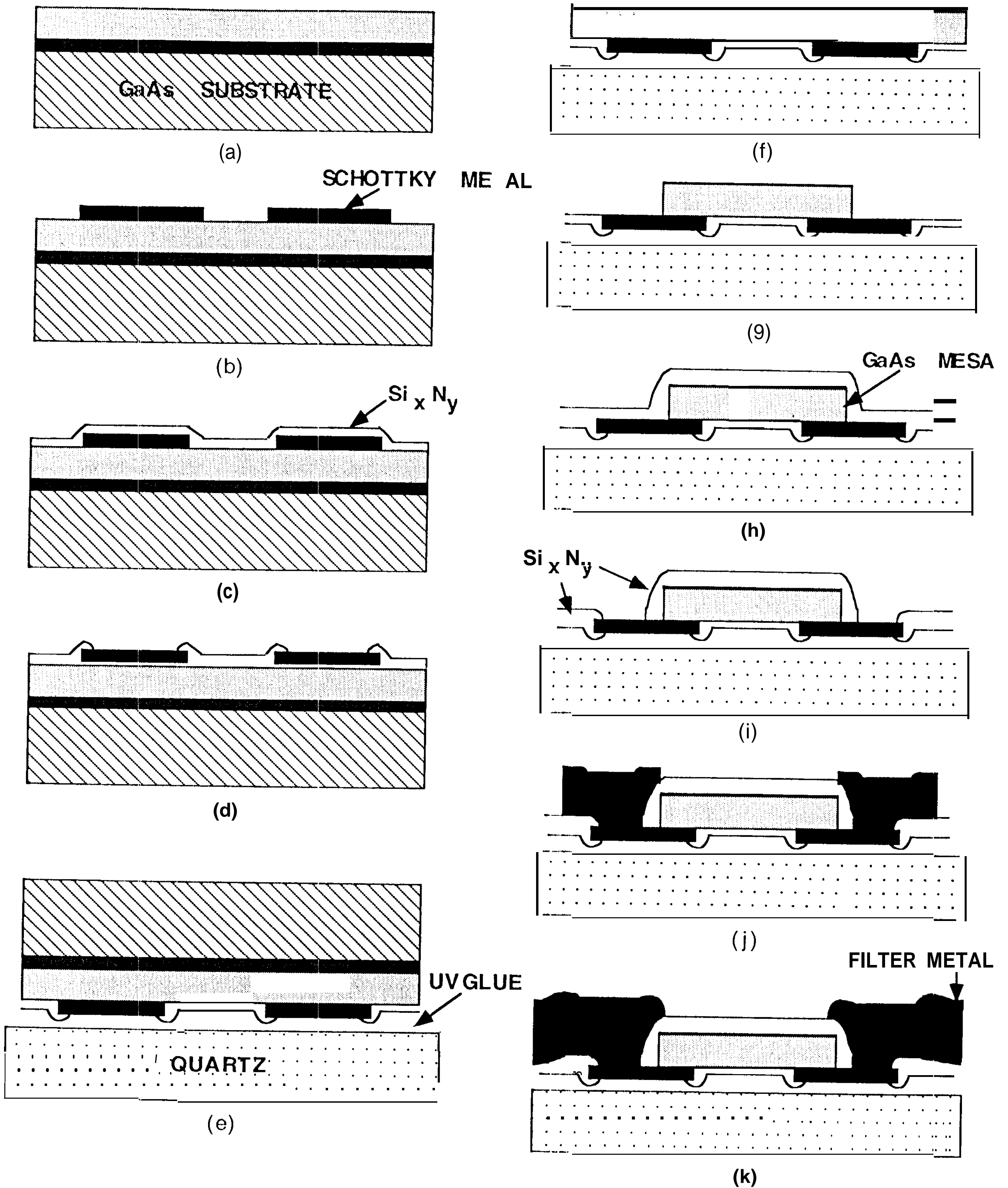

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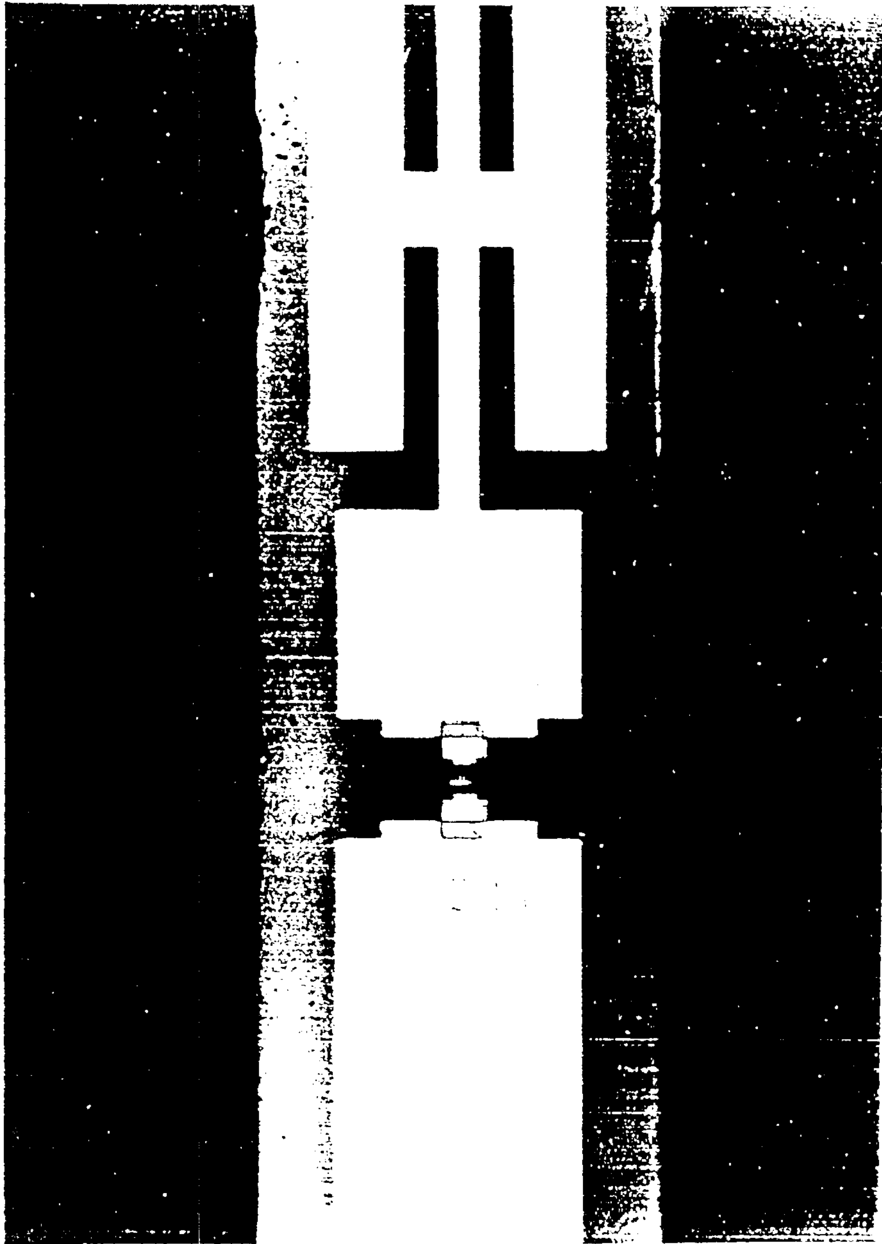
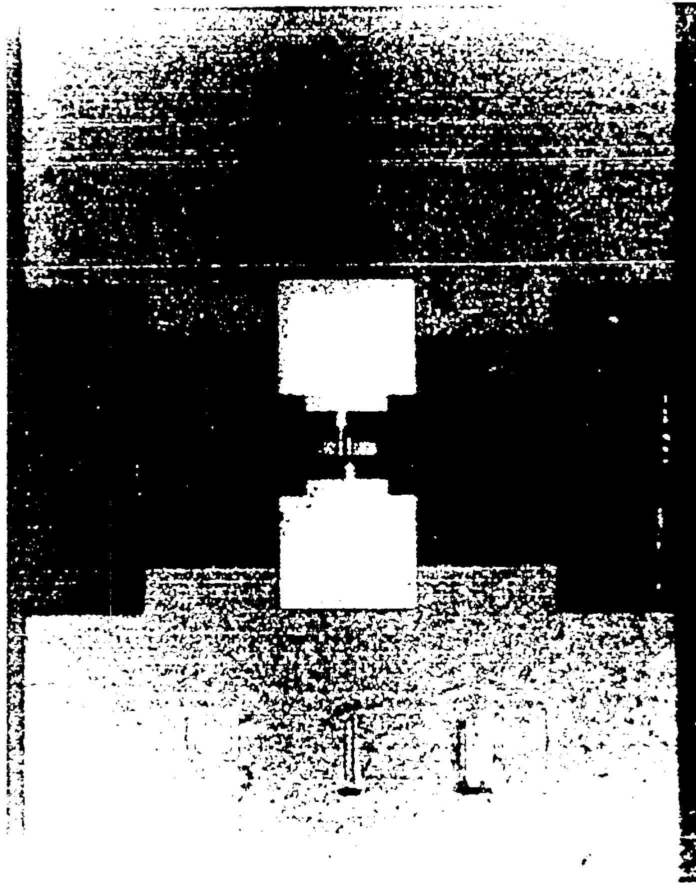
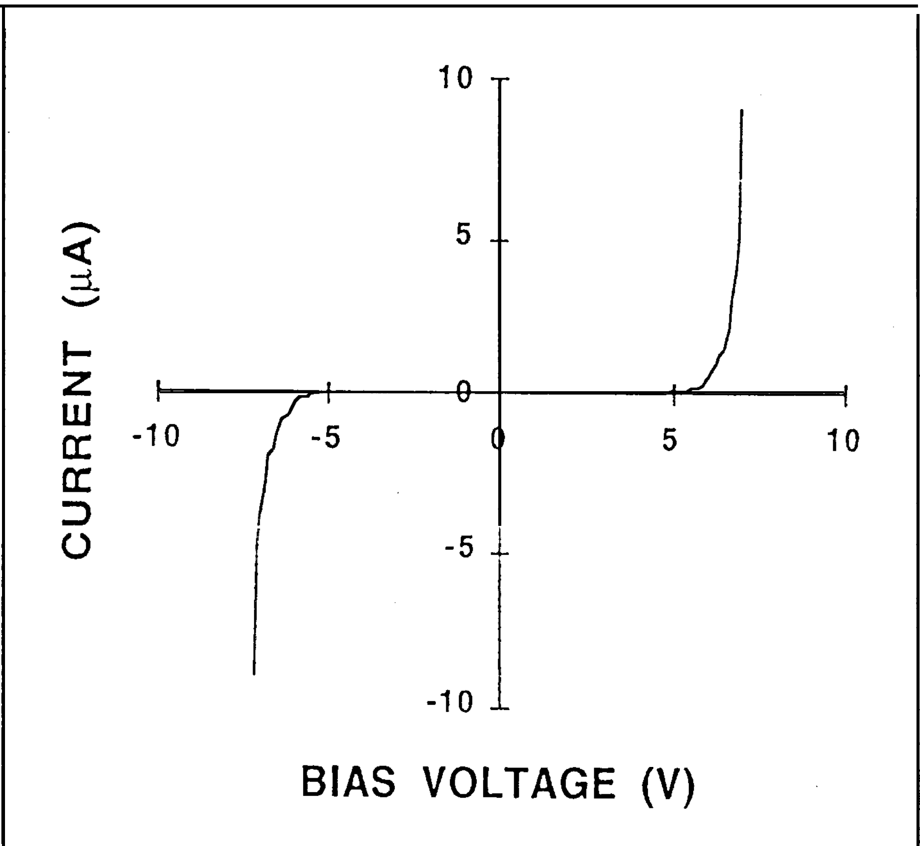


Fig 4a

Fig 4b





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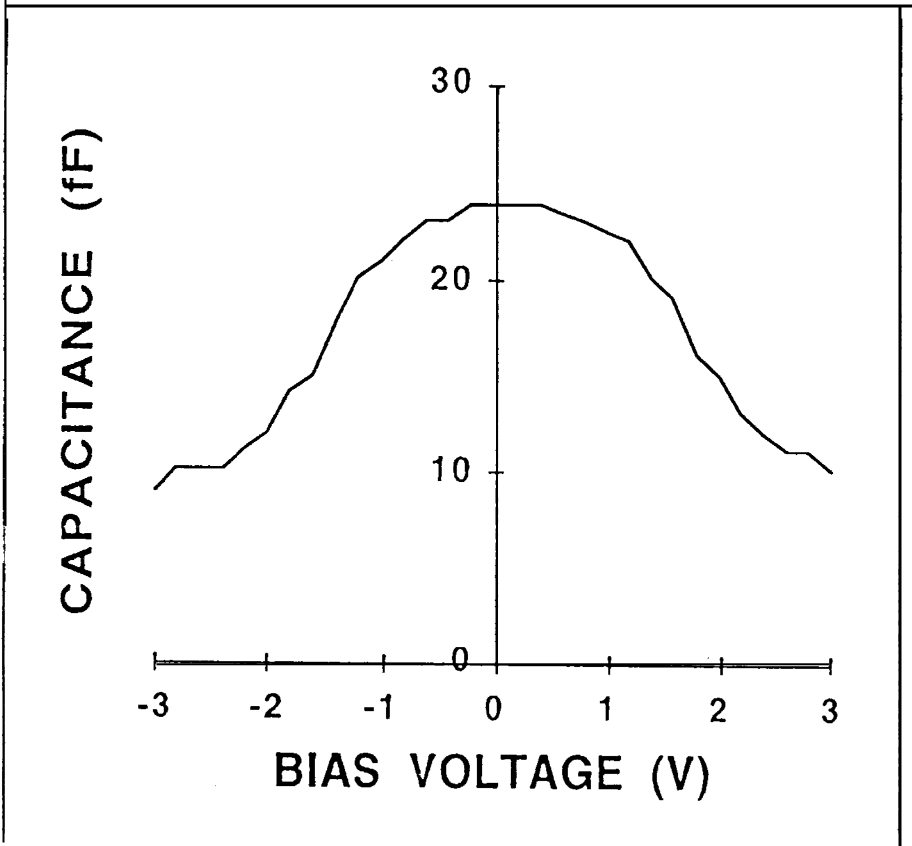

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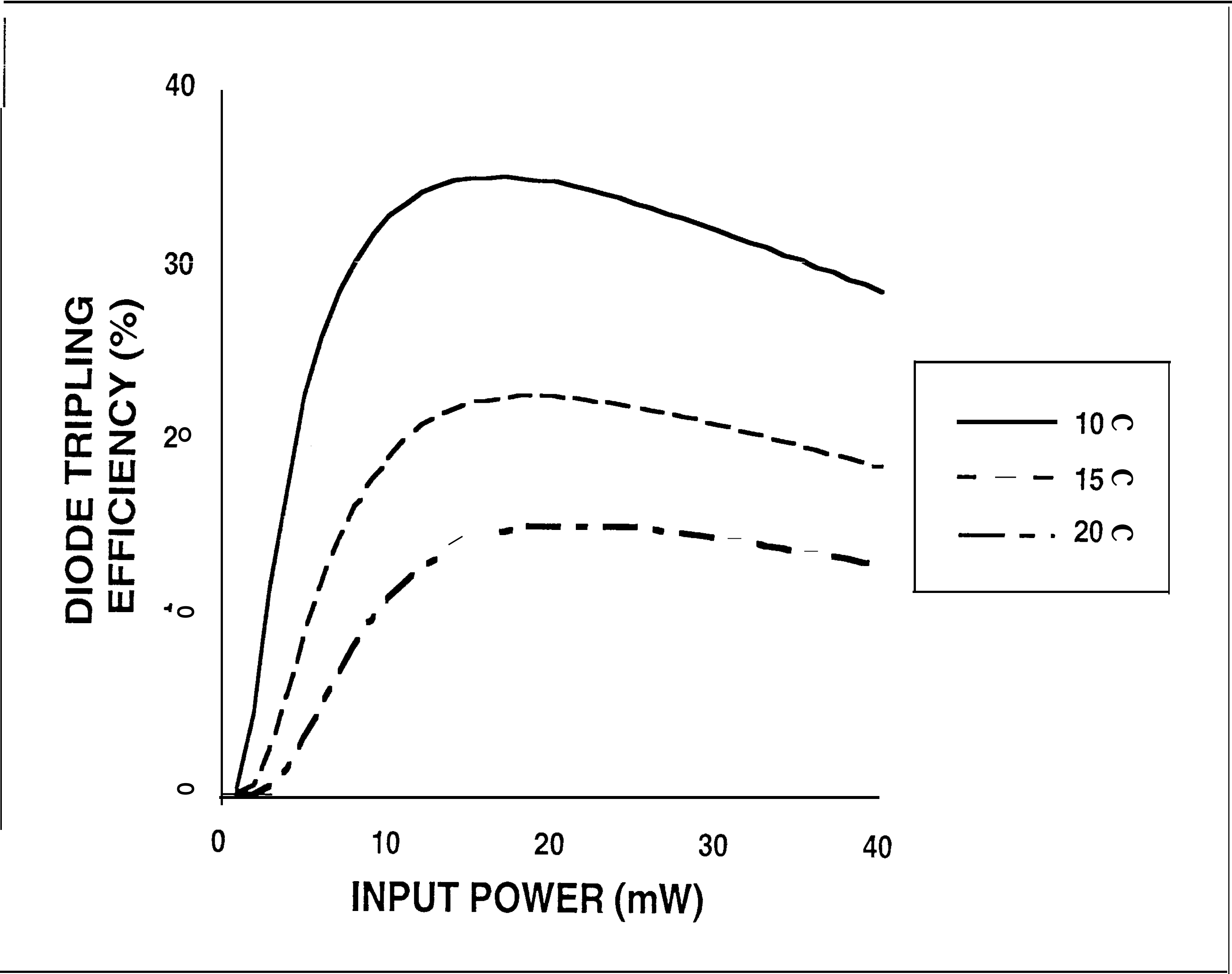

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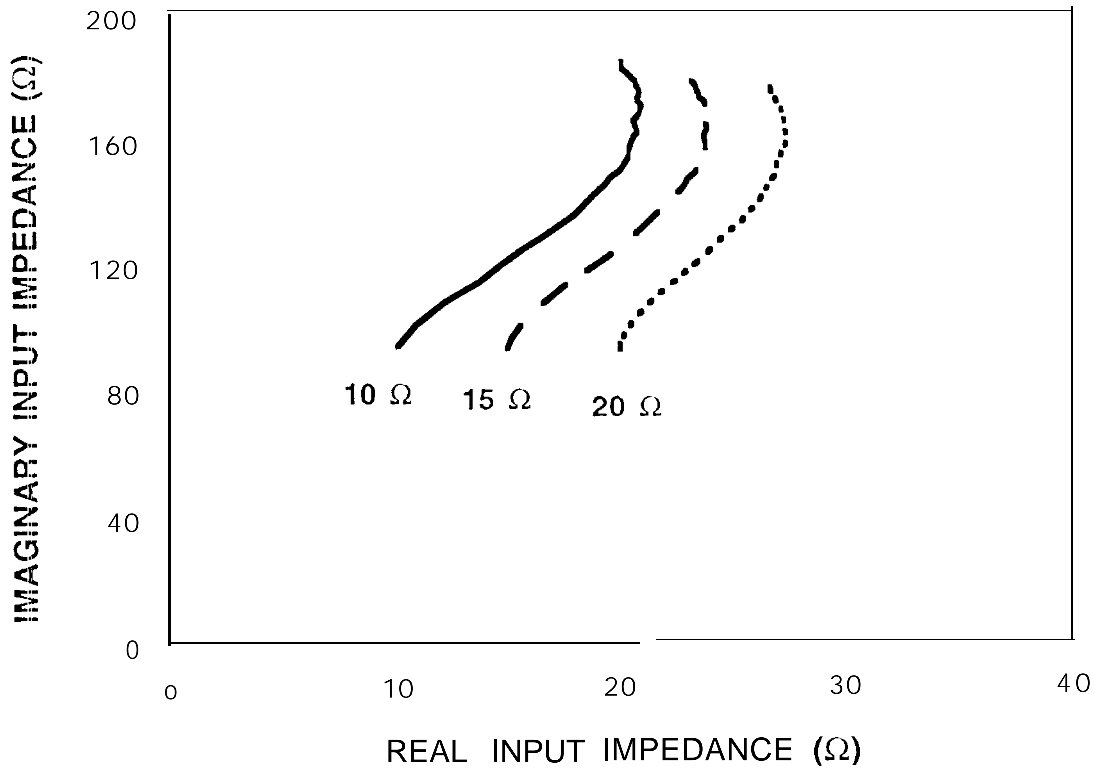

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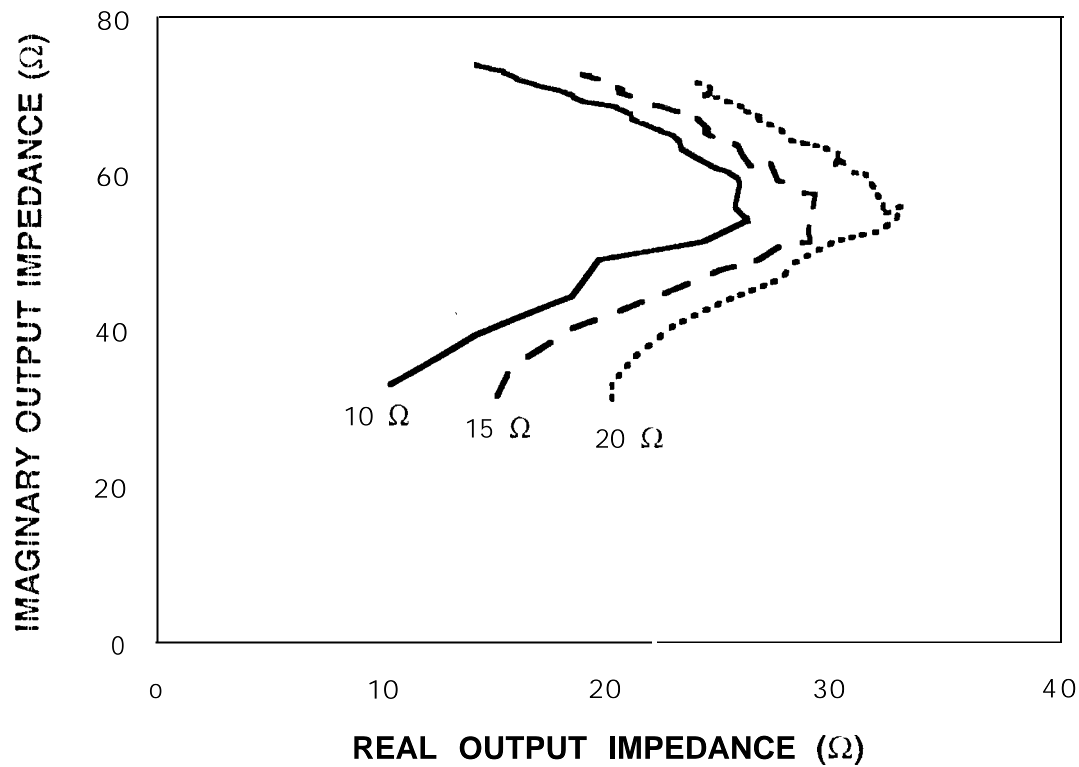

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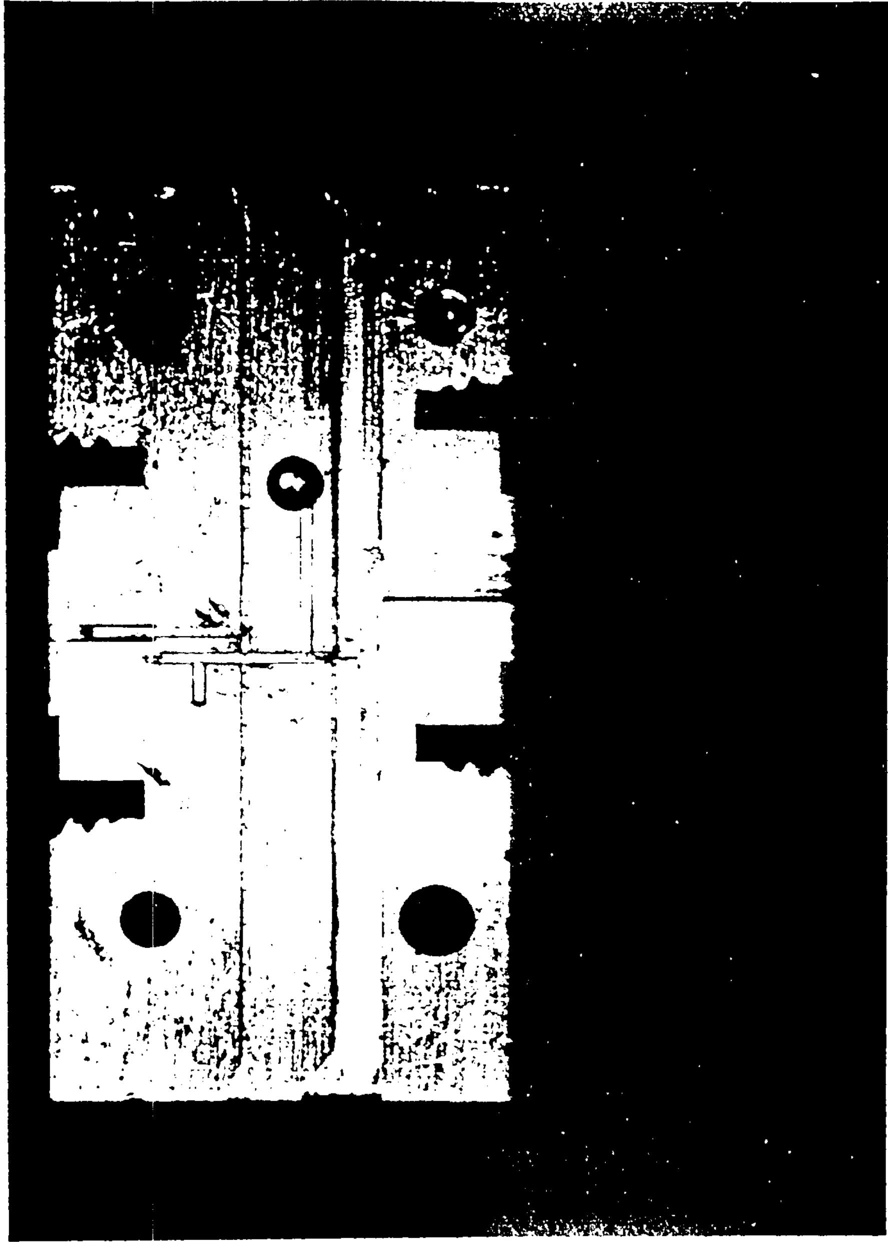

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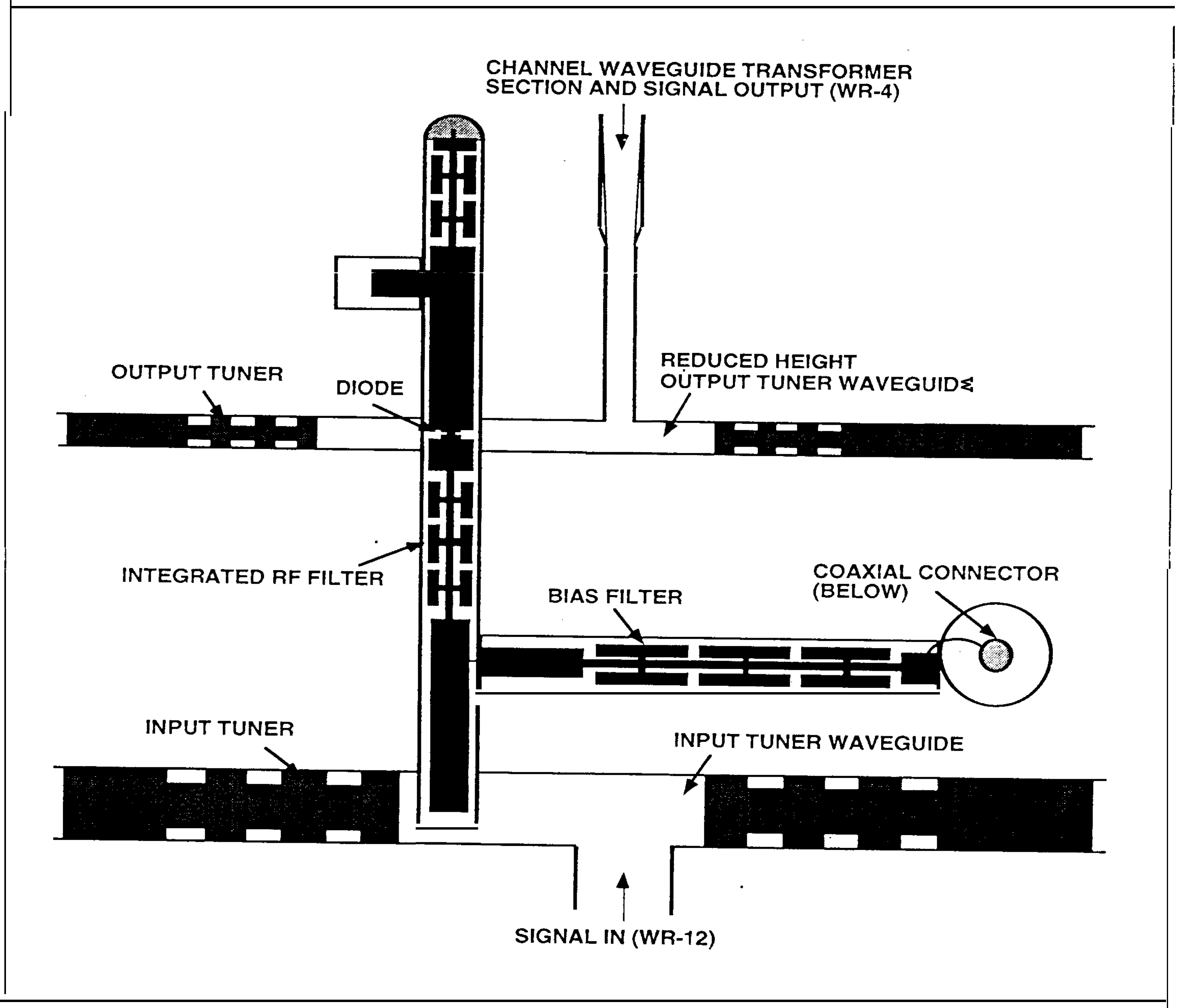
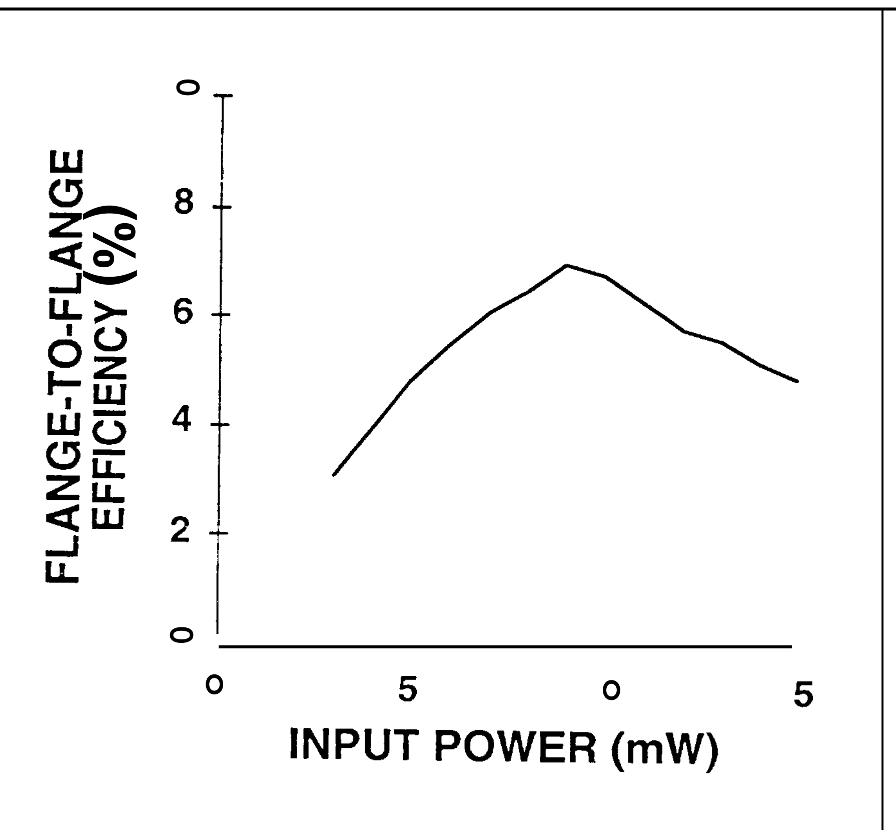


Fig-9



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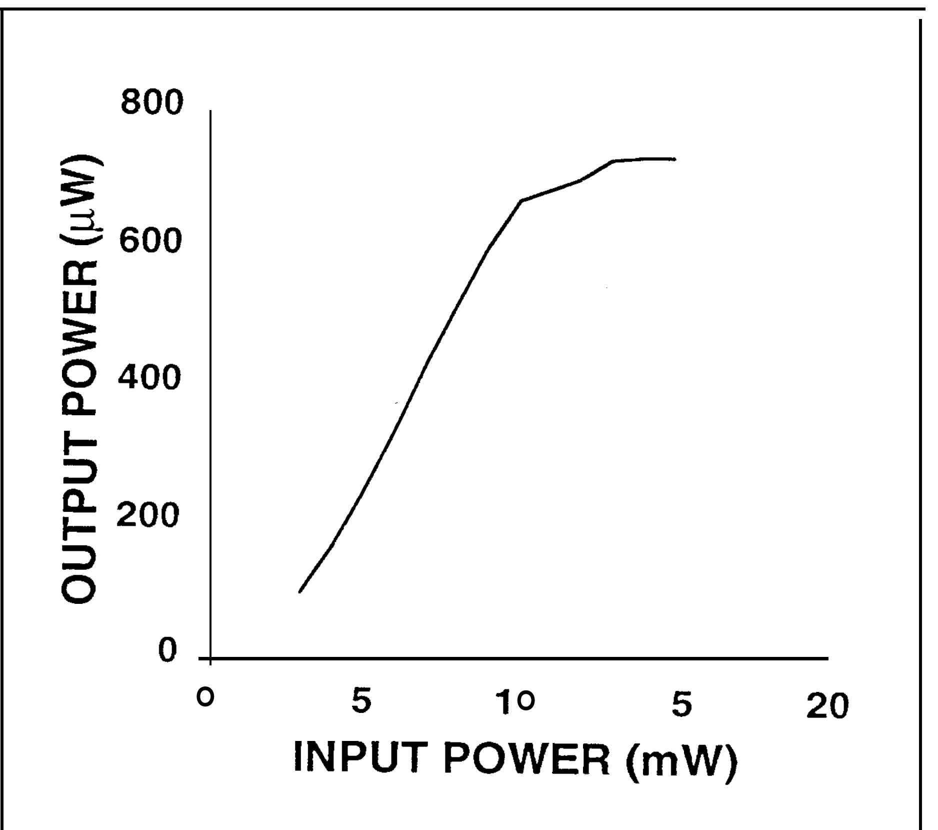

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Fig. 0

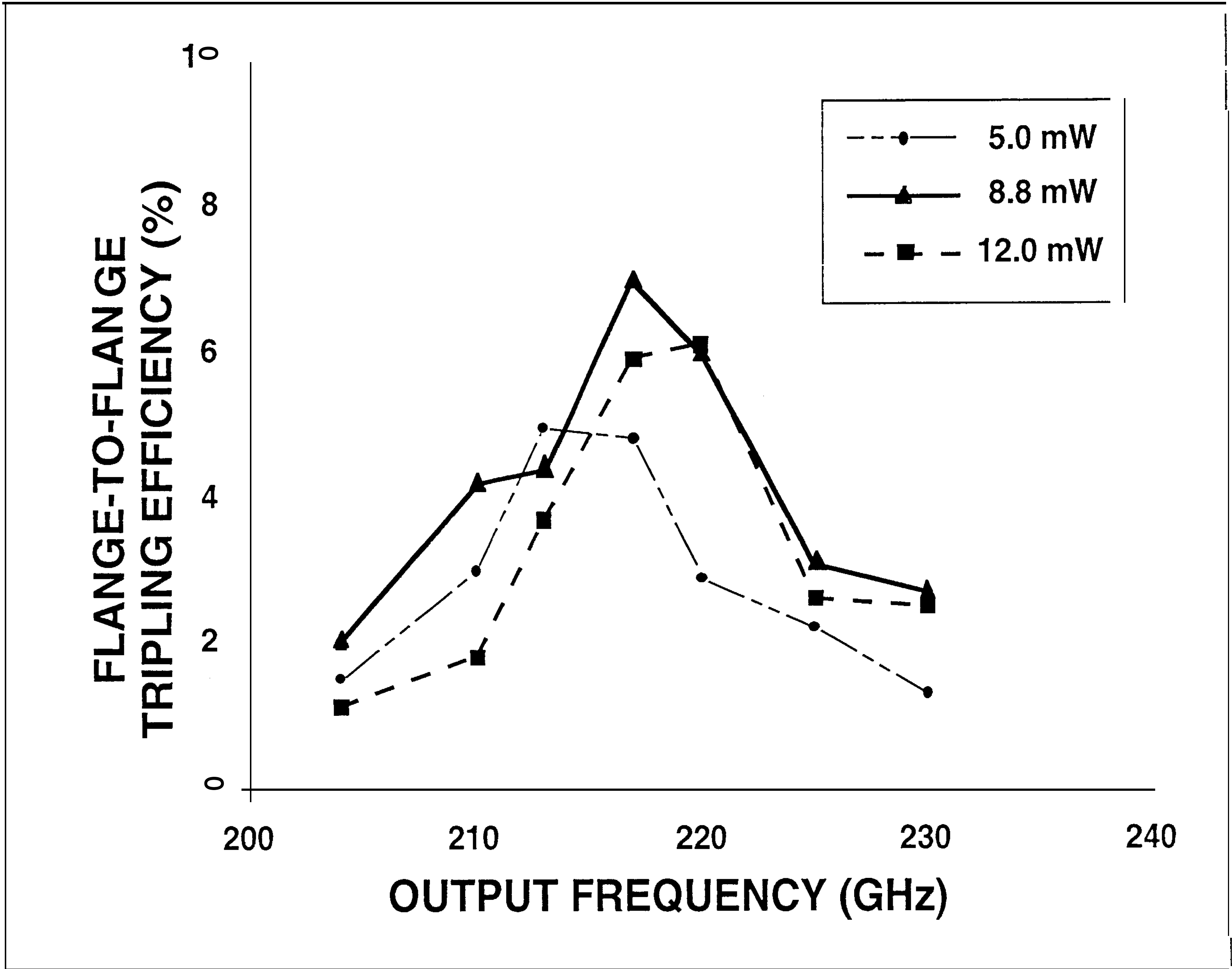

Fig. 1