THE INTERPLAY OF SURFACE MOUNT SOLDER JOINT QUALITY ANI) RELIABILITY OF LOW VOLUME SMAS

by

Reza Ghaffarian, Ph.D
Jet Propulsion Laboratory
California Institute of Technology

ABSTRACT

Spacecraft electronics as used in the NASA community, including the Jet Propulsion Laboratory (JPL), demand production of highly reliable assemblies in an Ultra-Low Volume (ULV) environment. At JPL, different aspects of Surface Mount Technology (SMT) including design, manufacturing, test, and deployment (aging) cycles arc being investigated, Extensive work has been done in these areas. Onc aspect is focused on identification of the critical manufacturing parameters, the effect of manufacturing defects on solder joint reli ability, and integration of Quality Assurance (QA) procedures into the design and manufacturing so that the critical parameters could bc bounded and controlled. In this paper, manufacturing defect types for leaded and leadless SMT assemblies arc compared, For leaded assemblies, solder joint quality of assemblies will bc cori elated with the solderability test results performed on lead remnants For Leadless Chip Carriers (1 .CCs), correlation between SMT solder joint manufacturing defects and damage propagation during thermal cycling, and the life of solder joints arc presented. The daisy chained assemblies were monitored for electrical continuity throughout the tests to detect "opens" using slight changes in resistance as an indicator. Assemblies were periodically inspected visually at 20-50X magnifications and also at higher magnification using a scanning electron microscope (SEM) to validate visual results.

SUMMARY

OBJECTIVES

NASA Headquarters has established an Electronic Packaging and Assembly Program to address the common needs of NASA programs, Onc of these programs is focused on the usc of SMT for high reliability, ULV spacecraft electronics as used in the NASA community. Four RTOPS (Research & Technology Objectives & Plans) have been conducted at NASA's Jet Propulsion Laboratory each dealing with an aspect of SMT. These RTOPS are interdependent and arc being conducted concurrently. Each RTOP concentrates its efforts on a particular aspect of the design, manufacturing, test, and deployment (aging) cycle. The primary objectives of the RTOPS arc as follows:

- Identify the critical parameters of SMT manufacture. Determine the methods and tools required to integrate QA procedures into the design and manufacturing processes so that the critical parameters can bc bounded and controlled.

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- Develop a thorough understanding of the creep-fatigue mechanisms underlying solder joint failures of surface mount electronic packaging systems. Develop generic, broadly applicable design guidelines, analysis methodologies, and data requirements.

- Develop an assembly level qualification test methodology for surface mount technology and apply this methodology to electronic packaging systems through the use of experimental design techniques and phased experimentation.

- Deliver the NASA Guidelines for SMT, developed from the knowledge gained from the JPL RTOPS, as well as the efforts of other NASA centers, industry knowledge centers, and industry partners.

References 1-7 document some of activities in these areas. In conjunction with the RTOPS, a survey and a series of Phase 1 and Phase 2 cooperative test programs involving all RTOPS arc being performed. Results of the survey and Phase 1 and Phase 2 test programs with emphasis on the Quality Assurance efforts arc presented.

SMT SURVEY

NASA centers involved with SMT were surveyed in 1993 (Reference 1). Onc section of the survey addresses QA issues for SMT hardware. The objectives of the SMT QA survey were to identify the critical parameters of the SMT manufacture and to determine the methods and tools presently used by industry to identify and control them. It was concluded that the leading causes of SMT rejects were solderability and solder paste deposition problems. Some operations did not have corrective action feedback loops to change a design or process even when data indicated a problem.

PHASE 1 TEST PROGRAM

The Phase 1 test involves use of a single ceramic component, 0.050" pitch, soldered to an epoxy-fiberglass FR-4 board (Reference 4). LCCs, J-lead cerquads, and gull wing cerquads were the SMT components. The JPL SMT Training" Facility assembled 20 and the Electronics Manufacturing Productivity Facility (EMPF) in Indianapolis, Indiana assembled 205 test boards.

Thermomechanical cycle testing (-55°C to 100"C, 45 minutes dwells and duration of 246 minutes) on Phase 1 assemblies having LCCS, began in August, 1993. All LCC assemblies have failed (open circuit). Twro-parameters Weibull equation was used to characterize failure distribution (Figure 1). Phase 1 testing of the J-leads was initiated in January, 1994, and now has reached more than 2,000 cycles with no failure. Testing of the gull wing cerquads started in July, and they have now (November 1995) accumulated more than 1,800 cycles with onc failure at 1,720 cycles.

All Phase 1 assemblies were inspected prior to thermal cycling, and have been, or will bc, periodically inspected as they arc cycled to electrical (solder joint) failure. Correlation between manufacturing defects, dimensional characteristics, inspection observations and life of the solder joint have been analyzed for the failed LCCS and is presented (Figure 2).

Since JPL and organizations surveyed are using visual inspection for acceptance/rejection of solder joints, wc also used this technique. To selectively validate observations we utilized other more powerful visual aids including SEM and cross-sectional microscopic evaluation. Crack initiation and propagation over time were documented using visual inspection and/or SEM (Reference 7).

Two methods were developed for ease of inspection data visualization and trends identification. In the first method (Reference 4), inspection data were displayed in an innovative graph representation that allows instant visualization of damage progress levels and correlation to pin locations, In the second method, shown in Figure 2, the damage that progressed over time was plotted for a group of leads that had the same category of manufacturing defect . These methods could be adapted for use with other type of data, and other graphical display methods for case of data visualization and trend recognition.

PHASE 2 TEST PROGRAM

Phase 2 used several different types of packages similar to phase 1 as well as capacitors and resistors on a polyimide board. The overall purpose of the Phase 2 testing is to perform statistically significant testing of surface mount assemblies to better understand the failure 'modes and inherent fatigue life of the solder interconnect, and to continue development of tailored qualification methods. Critical SMT manufacture parameters will be controlled to determine their effects and to further develop QA methodologies. Design of Experiment (DOE) test methodology is being utilized to meet these objectives. The DOE is a hybrid of full factorial and partial factorial approaches. The majority of environmental testing will consist of flight-like thermal cycling, i.e., thermal cycling within a vacuum environment.

Extensive planning and coordination were required to implement the DOE requirements in a manufacturing environment. A total of 33 test boards with over 3,000 components that included about 600 LCCs, J-leads, and fine pitch gull wings were assembled at Lockheed Martin, Sunnyvale, California One test vehicle was assembled at the JPL SMT Training Facility Center for electrical and thermal characterization and validation.

For ease of manufacturing flow, the boards were divided into six groups, each differing by at least one variable. Variables included tinning for J-leads and LCCS, reflow profile for the board assembly, and lead height for the fine pitch gull wings. Also, prior to assembly, J-leads and LCC packages were tinned manually by dipping in molten solder pot. There were no solder defects when the LCCS were tinned (4 times-- once for each side); however, occasional ceramic lid debonding did occur.

After solder paste application and package placement, thirty boards were mass reflowed using standard and three using a modified reflow profile. Modification of the profile was made by rapid cooling of the assembly just after solder solidification to produce a representative of a hand soldering condition.

Assemblies were visually inspected at JPL for solder joint manufacturing defect and onc or more defect codes assigned. For ease of visualization and trend identification, inspection data graphed in three-dimensional plots and commonly to rare defect type occurrences were identified for package types and assembly locations on PWB (Figure 3). In addition, gull wings of four test vehicles were reworked as a part of the DOE test plan even though they did not have defects. Two gull wings were reworked by removing and replacing the solder while the remaining six had the ten corner solder joints reworked, These assemblies are being subjected to thermal cycling exposure pcr DOE requirements to determine the effects of these variable on reliability.

Solderability behavior of remnant of gull wing leads were evaluated for comparison to manufacturing defect of gull wings. The dip-and-look qualitative test method was used at vendor site and a quantitative Multicore Universal Solderability Tester (MUST), that measures wetting force, was used at JPL. Vendor tested about twenty and JPL tested approximately 500 strips of leads. Leads were held in place by a plastic strip in bundles of41 and 64 leads representing a side of 164 and 256 gull wing packages, respectively. Results of visual inspection, dip-and-look, and MUST print-out data were compared for 164 and 256 gull win packages (Table 2).

PHASE 1 TEST RESULTS

LCC SOLDER JOINT MANUFACTURING DEFECTS

Table 1 lists summary defects observed for LCC assemblies during the manufacturing inspections prior to thermal cycling. This Table also includes defect codes used for Phase 1 testing that include other packages, e.g. code 29 for gull wing, as well as those generally used for crack propagation mapping (codes 13 to 20).

As the Table shows, no dewetting or non-wetting was observed. Defects such as icicles, solder bridging, inclusion, void, and light stress defects were extremely rare. The next most commonly occurring significant manufacturing defects were associated with the improper control of solder paste amount, including observations of excess and lumpy solder

TABLE 1. Defect Codes and Types for Identification of Solder Joint Quality

Defect Code/Type	68 Lcc	28 LCC	20 LCC
1 NO MFG DEFECT	138	107	32
2 SOLDER BALLS	23	33	0
3 DEWETTING	0	0	0
4 NON-WETTING	0	2	0
5 INCLUSION	0	5	0
6 VOID	3	0	0
7 ICICLES	7	2	0
8 INSUFFICIENT SOLDER	401	64	46
9 EXCESS SOLDER	0	3	11
10 NO FILLET	0	0	0
11 LEAD OVERHANG	0	1	0
12 CONTAMINATION (ON SOLDER)	477	30	0
13 LIGHT STRESS	0	0	0
14 MODERATE STRESS	0	0	0
15 HEAVY STRESS	0	0	0
16 POSSIBLE CRACK	0	1	0
17 CRACK@ 25% FEATURE LENGTH		0	0
18 CRACK@ 50%	0	0	0
19 CRACK @75%	0	0	0
20 CRACK @100%	0	0	0
Total assemblies'	**24**	**73**	**8**
Total Joints	1632	2044	**160**

Defect Code/Type	68 Lcc	28 Lcc	20 Lcc
21 SOLDER BRIDGE	0	6	0
22 GRAINY SOLDER	1429	1866	90
23 LUMPY SOLDER	9	66	4
24 STRETCH MARKS	10	131	3
25 BOARD CONTAMINATION	623	364	20
26 INSUFFICIENT TINNING	0	2	0
27 LEAD SOLDERED 10 BODY	0	0	0
28 LEAD TOO HIGH	0	0	0
29 TOE DOWN	0	0	0
30 LEAD DEFORMED	0	0	0
31 DAMAGED JOINT	0	0	0
32 CONTAMINATION (IN SOLDER)	0	0	0
33 HEEL NO FILLET	0	0	0
34 OPEN	0	0	0
35 LUMP SOLDER ON LEAD	0	0	0
36 CYCLING PEEL OF}	0	0	0
99 NO CYCLESTRESS DEFECT	0	0	0

* Note: Some of the assemblies fabricated were not inspected and thermally cycled

joints. Solder joints with excess solder were few while the number of joints with insufficient solder were very high. Solder and board contamination commonly occurred, The grainy solder (defect 22) was the single most frequently observed defect with a percentage of rnorc than the total percentages of solders with other defect types.

CYCLES TO FAILURE AND WEIBULL DISTRIBUTION

Figure 1 shows cycles to failure for 68-, 28-, and 20-pin LCC assemblies. Failures were detected by Anatech® and verified by visual inspection. The failure distribution percentiles were approximated using median plotting position, Fi (i-0.3)/((n+0.4). As expected, there was a large spread in cycles to failure because of variance in solder joint volume, quality and location. The first failure for the 68-pin LCCS was detected at 53 cycles while the last sample failed after 139 with 93 average cycles. 28-pin LCCS failed at much higher cycles in the range of 352 to 908 with 660 average cycles. The 20-pin cycles to failure were in the same range as for those of 28-pins and failed within 573 to 863 averaging 674 cycles.

If only Distance from Neutral Points (DNPs) are considered, the 20-pin LCCS should have failed at higher cycles, Cycles to failure is directly proportional to DNP. However, cycles to failure also inversely depends on the effective solder fillet height. Solder fillet height for 20- and 28-pin LCCs were .021 and .033 inches respectively, which is lower for 20-pin resulting in higher shear strain for the same CTE mismatch displacement. The difference in part size could have been off-set by the difference in the fillet height.

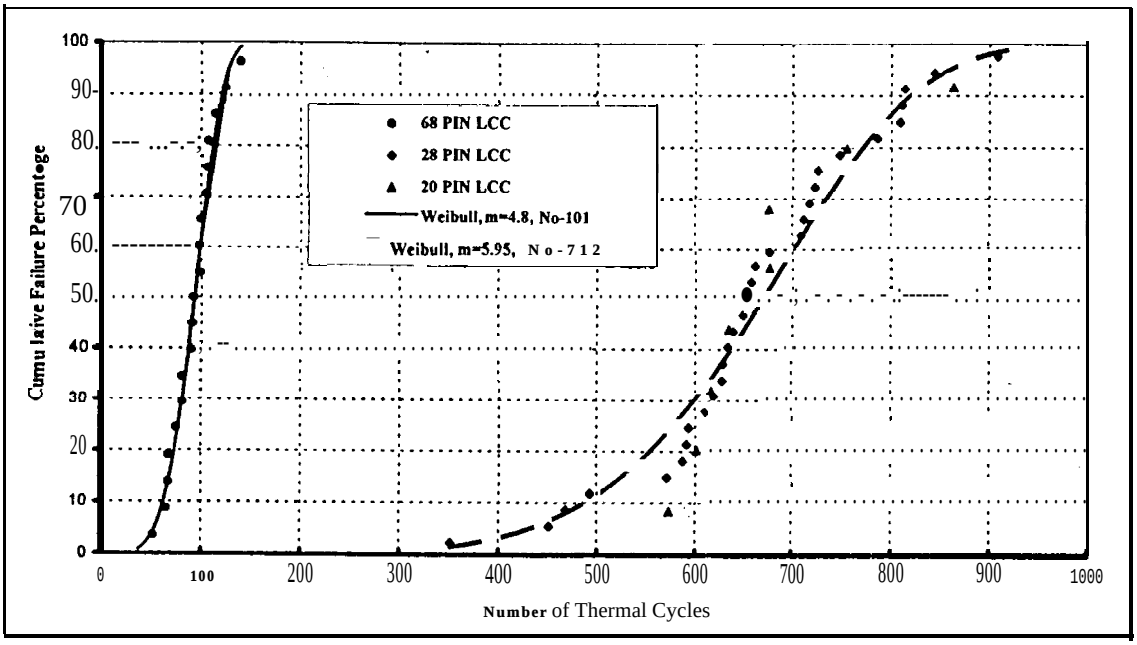


FIGURE 1. Cumulative Failure Distribution Plots for LCC Assemblies

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull cumulative failure distribution was used to tit 68- and 28- pin LCCS' cycles to failure data. The Weibull graphs are plotted in Figure 1 as solid and dash lines for 68- and 28-pins, respectively, For 68-pin LCCS, the scale and shape parameters were 101 cycles and 4.8, respectively. These were 712 cycles and 5.95 for the 28-pin LCCs. Both data sets showed excellent linear correlation in log-log plots with a coefficient of correlation of at least 0.97.

MANUFACTURING DEFECTS AND RELIABILITY CORRELATION

Effects of manufacturing defects on solder joint reliability were determined using visual inspection data of LCC assemblies. The crack propagation was mapped over time for solder joints with a manufacturing defect categories including grainy and insufficient solder joints. Analysis of damage growth enable one to quantitatively define the criticality of each defect category, and based on the results, provide general or specific guidelines for the rejection of manufacturing defects.

Figures 2 show an approach that tracks damage growth of individual solder joints and graphs damage accumulation for solder joints with specific manufacturing defect categories. For 68-pin LCC, two types of defect categories were included in one plot, there were 930 grainy and 180 insufficient solder joints with 100 having both defects. It is clear from these and similar plots for 20-pin LCCS (Reference 7), that the solder joints with a higher defect category showed earlier signs of damage growth as well as accounting for higher failed joint percentages. Similar plots were generated for other LCCs.

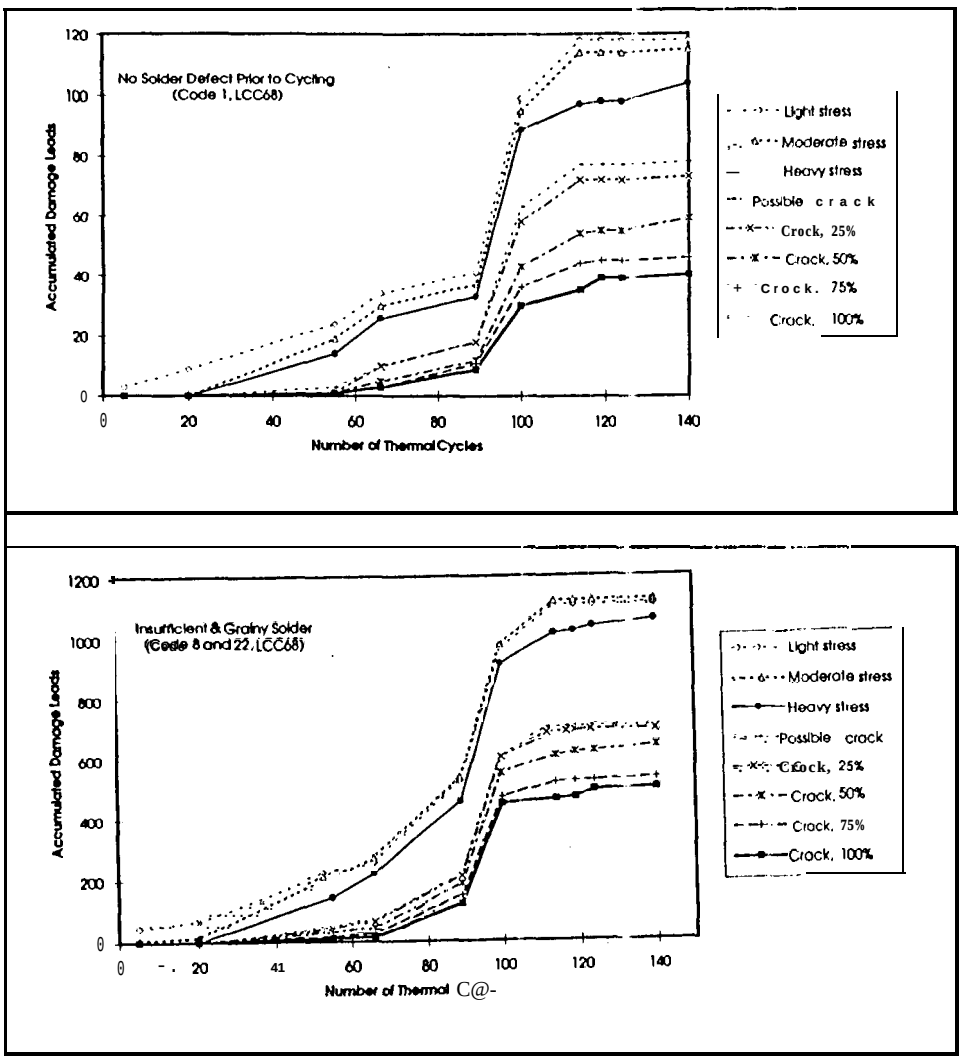


FIGURE 2. Accumulation of Damages for 68-Pin LCC Solder Joints With and Without Manufacturing Defects

PHASE 2 TEST PROGRAM

SOLDER JOINT MANUFACTURING DEFECTS

Assemblies were visually inspected at 10-50X magnification for solder joint quality at JPL and one or rnorc defect codes were assigned to a joint (defect codes of Table 1). The total number of defects for the three main categories, i.e., gull wing, J-leads, and LCCs included:

- 73,211 inspection points for gull wing leads with 16,118 leads showing no signs of defects and the rest showing defects
- 17,243 inspection points for LCC terminations with 7,991 showing no signs of defects and the rest showing defects
- 13,843 inspection points for J-leads with 4,271 showing no signs of defects and the rest showing defects

It should be noted that the total of inspection points arc generally much higher than the total of solder joint leads/terrnination inspcctcd, since often a lead shows more than onc inspection point (defect type). To visualize data, these were presented in 3 dimensional plots (Figures 3). To generate the z axis percentage, the total of number of a defect type was divided by the total of the inspection points for that package. For example, for 256 lead gull wings, the total number of lead overhangs were 449. This number was divided by 24,481, the total number of inspection points for this assembly to obtain the defect percentage. Some of the general observation are as follows:

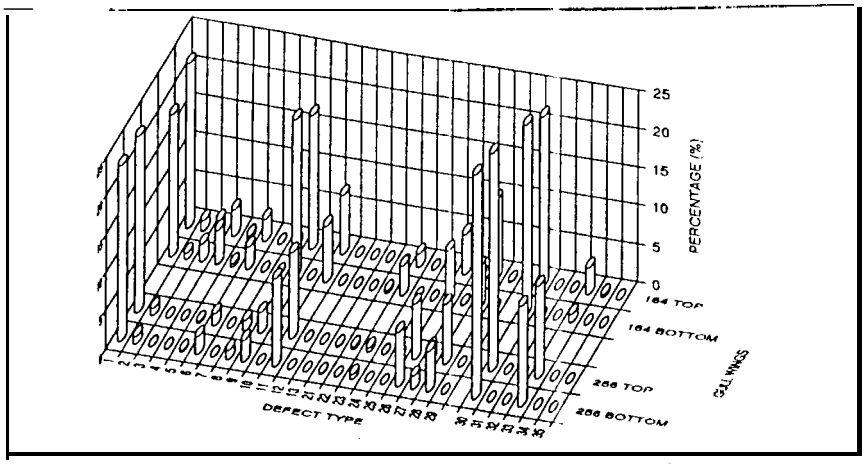
Some of the general observation arc as follows:

- Leaded packages showed higher defects than LCC type packages. Fine pitch gull wings showed higher defects than J-leads. The higher values for gull wings are partially attributed to the leads not being straight to start with
- Lead deformed defect for gull wings, lead overhang for J-leads, and grainy solder for LCCS were the major contributors of defects
- The defect distribution and number for 164 and 256 gull wing packages were independent of location
- Gull wings with 164 leads showed about six times higher number of leads with excess solder than the 256 lead gull wings. This is in agreement with solderability test results performed on these leads (Table 2)
- The 28 J-leads that were located in the center of the printed wiring board showed much higher grainy solder than those J-leads at corner areas. This is possibly duc to temperature non-uniformity with temperatures reaching higher values at the center during the reflow process

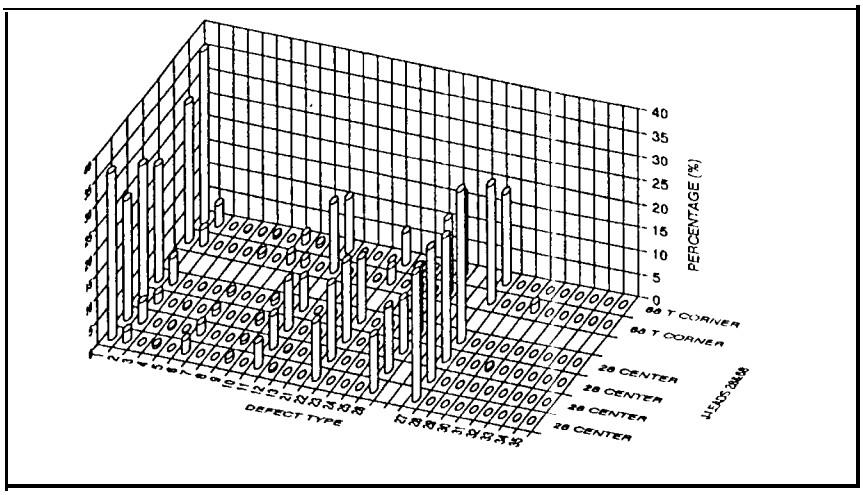
Similar to Phase I Quality Assurance approach, the phase 2 assemblies will be periodically inspcctcd as they are cycled to electrical (solder joint) failure. Correlations between manufacturing defects, dimensional characteristics, inspection observations and the life of the solder joint in different cycling environments (atmosphere and vacuum) and cycling temperature ranges will be analyzed and will be presented in a future paper.

INSPECTION CORRELATION TO SOLDERABILITY RESULTS

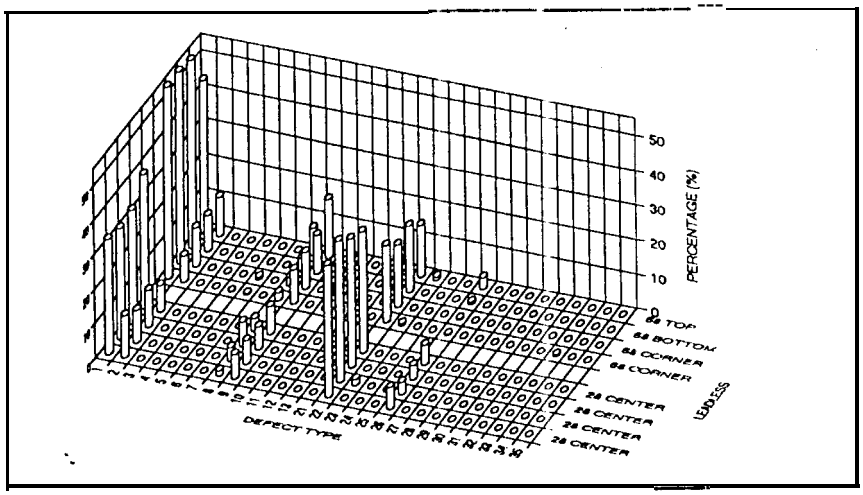
Table 2 lists dip-and-look, MUST print out test data and solder joint inspection results. Values for dip-and-Iook arc approximate area percentages of non-coverage solder areas. F, r, and S parameters arc those read from MUST print-outs. These parameters arc automatically calculated based on the wetting section of the curve, i.e., time to begin wetting to time to maximum wetting force.



Fine Pitch Gull Wings at Top and Bottom Near the Edge of PWB Assembly



J-Lead at the Center and Top Corner of PWB Assembly



Leadless Chip Carrier at Center and Other Locations of PWB Assembly

FIGURE 3. Defect Percentages for Part Types and Location on the P WB Assembly

The plot portion approximates to an exponential, that is the force f at any time t is considered to be a function of the maximum force F_{max} and the time constant **S.**

$$f = F_{max} (1 - \exp(-t/S))$$

The 'Wetting speed" changes with time and is a function of the time constant S, The force f, changes from the maximum negative wetting force to the maximum positive force. S is measured in seconds, when **t=S, f =** 0.632 F_{max} F_{max} and **S** can be calculated from the force/time curve. The MUST wetting balance takes force readings every 0.1 seconds, and the best fit of data to a straight line of log-log of this equation. The value F_{max} and S arc calculated from the regression line together with the coefficient of correlation r, which express how closely the observations fit a straight line,

Based on the dip-and-look test results, all of the 164 and most of the 256 gull wing leads failed solderability testing (non-coverage area more than 5%). Results of solder joint assembly inspection contradict the dip-and-look test results for the 164 gull wing leads whereas they agree with results of the of 256 leads, It should be noted that the 164 leads had a tin coating layer whereas the 256 leads had a gold coating layer. It is possible that the test results were influenced by surface coating conditions. This needs to bc further explored,

The print out values of **r, S,** and **F** give some indication of solderability. The r indicates uniformity of wetting. If wetting characteristic of the lead, everywhere, then the value or should exceed 0.8 (dimensionless). **S, in** seconds gave some indication of the speed of wetting. A value of less than 1 second shows rapid wetting which considered to bc good. The total wetting force, **F,** depends on the perimeter of the specimen and when divided by the perimeter value in nun gives the wetting strength.

TABLE 2 Lead Solderability Test Results And Solder Joint Inspection

Serial Number	Time Constant (sec)	Correlation Coefficient	Wetting Balance Force (grams)	"Dip & Look" non-coverage	Dip & Look Pass/ Fail	Visual Inspection
164 GW	**S**	**r**	**F**	(%)		
6	0.407	0.951	0.734	25	Fail	OK
9	0.258	0.966	1.060	10	Fail	OK
32	0.269	0.970	0.579	10	Fail	dewet,nonwet
36	0.569	0.876	0.367	20	Fail	OK
62	0.334	0.964	0.541	25	Fail	No inspection
68	0.543	0.855	0.509	35	Fail	OK
69	0.797	0.741	0.906	30	Fail	dewet
79	0.881	0.933	0.538	15	Fail	dewet
256 GW						
1024	0.357	0.971	1.320	5	Pass	OK
1034	0.346	0.962	1.126	1	Pass	OK
1035	0.413	0.916	1.426	20	Fail	bridge
1037	0.410	0.866	1.518	30	Fail	open
1044	1.205	0.426	1.971	5	Pass	OK
1045	0.738	0.687	1.378	5	Pass	OK
1046	0.352	0.980	1.091	1	Pass	OK
1049	0.612	0.699	1.695	?	not cleaned	OK
1061	0.193	0.971	1.075	5	Pass	bridge

DISCUSSION

Ultra-low volume surface mount assemblies considered for space applications do not permit the proof of process potential as commercial or military production quantities. This fact mandates that Quality Assurance involvement be proactive and be included throughout the process of validation and proof of process build, and as well as problem detection by inspection. The QA engineer should be responsible for ensuring that manufacturing controls are in place and that critical steps are considered and understood for inspection. In this cooperative investigation, the QA role being proactive and concurrent resulted in better understanding of some of the critical parameters in solder joint reliability as well as more confidence in the methodology of visual inspection. In correlating visual inspection results to those of SEM and microsectioning, it has been demonstrated that once trained, QA personnel would indeed be able to detect solder joints with potential reliability problems.

At JPL, the conventional pass/fail criterion relies on visual inspection at 10x to 50x magnifications. For leaded parts, once cracking is observed, more than an one order of magnitude additional cycles are required before the failure whereas this is not the case for leadless assemblies. Crack initiation and propagation in the heel fillet of gull wing leads which arc considered to be kcy factors in solder joint failure mechanisms arc being closely monitored. One solder joint showed signs of heel fillet cracking at 50 cycles, but did not continue propagating significantly up to 1,000 thermal cycles. For leadless, however, cracks usually initiate inside the joint, at the corner underneath the part, and propagate outward. For a 68-pin LCC assembly, cracks were not observed until 47 cycles. Complete cracking and failure occurred after 71 cycles.

Microstructural changes observed during environmental exposure could also be used to determine aging history and estimate remaining life of solder joints. These include observation of phenomena such as solder ball spreading, the appearance of "crack healing", and minor to major surface roughening. These changes also depend on the initial properties of solder including solder composition, solidification rate, and interface joint metallurgy. Information obtained from crack propagation and microstructural changes is being incorporated into prediction guidelines for design and reliability and training materials for inspection and manufacturing personnel.

Another aspect of this investigation is to better understand the interplay of manufacturing defects and reliability, and to provide QA personnel with the necessary tools to increase their effectiveness in detection of solder joints with potential reliability problems. To establish such criteria, visual criteria such as signs of heavy stress or crack initiation and possibly in combination with thermal aging including signs of grainy due to grain growth and ball spreading need to be investigated, The approaches including the crack propagation mapping over time for solder joints with a defect category was aimed to identify a quantitative definition about the criticality of each defect category. Qualitative indicators could be used to reject solder joints that do not meet cycle requirements for a mission thermal environment.

It was hoped that the interpretation of results of solder damage progress would provide the required quantitative visual indicator. Plots for cycles to failure for LCCS, because of missing inspection data intervals and combining solder joints irrespective of lead location could be used only to come to conclusion that those defect categories investigated result in early failure and possibly cause reduction of the Weibull shape parameter (increase in coefficient of variation).

Elimination of the cause of such defect will decrease failure spread and therefore provide higher confidence in ' predicating reliability for a significantly lower rate of failure.

Currently inspection results for 28-pin LCC with nearly 1,000 solder joints arc being analyzed to determine if a more definite trend could be established. Results will be analyzed similarly to those presented here as well as considering corner and center joints separately. Similar techniques will also be used for leaded parts of SMT Phase 1 and Phase 2 test programs and data will be presented as they become available. Based on the results, QA will

provide general or specific guidelines for the acceptance/rejection of solder joints for a mission thermal environment.

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BIOGRAPHY

Dr. Reza Ghaffarian has more than fifteen years of industrial and academic experience in mechanical, materials, and manufacturing processes engineering. At JPL, He supports research and development activities in SMT for infusion in NASA's missions including projects in advanced electronics packaging, interconnection, and assembly. His responsibilities include technical coordination, Design of Experiment (DOE) statistical test vehicle implementation, manufacturing process, inspection methodology development, failure analysis, and environmental test data collection and analysis. Dr. Ghaffarian has authored or co-authored over 15 technical papers and numerous patentable innovations. Hc has also organized and chaired many technical sessions. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 all in Engineering from University of California at Los Angeles (UCLA).