

VLSI Design of Cellular Neural Networks with Annealing and Optical Input Capabilities

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ABSTRACT

A cellular neural network (CNN) is a locally connected, massively paralleled computing system with simple synaptic operators so that it is very suitable for VLSI implementation in real-time, high-speed applications. VLSI architecture of a continuous-time shift-invariant CNN with digitally-programmable operators and optical inputs is proposed. The circuits with annealing ability is included to achieve optima] solutions for many selected applications.

1. Introduction

Local interconnection and simple synaptic operators are the most attractive features of the CNN. Under the mild conditions [1], a CNN autonomously finds a stable solution for which the Lyapunov function of the network is locally minimized. The CNNs can be used in many computation-intensive applications such as image and signal processing. Moreover, the quadratic nature of the Lyapunov function allows us to map it into optimization problems [2]. Several structural variations of the continuous-time, shift-invariant, rectangular-grided network which was introduced by Chua and Yang [1, 3] in 1988, have been reported. Among them are discrete-time CNN and CNNs with nonlinear and delay-type templates [4].

VLSI implementation of discrete- or continuous- time CNNs have been studied by many researchers [5]-[9]. A continuous- time, rectangular-type CNN with $r=1$ is reported here. A CNN unit consists of a *core neuron* cell, *synaptic weights*, *input/output circuits*, and *digital interface*, as shown in Fig. 1. The digital interface includes control data buses and read data lines. Four control buses for weights a_1 , a_2 , and b_0 are 5-bit wide each. The data for synaptic weights are written into operator registers and the network outputs are fetched from the cell output latches. In addition to the basic structure of the network,

the annealing capability is included to accommodate the applications in which the optimal solutions of energy function are needed. The hardware annealing is performed by increasing the gain of the neuron from a pre-determined low value to a final critical high value.

11. CNN with annealing

The hardware annealing is operated by controlling the gain of the neuron, which is the same for all neurons throughout the whole network. After the state is initialized to $x=x(0)$, the initial gain at time $t=0$ can be set to an arbitrarily small, positive value such that $0 \leq g(0) \ll 1$. It then increases continuously for $0 < t \leq T_A$ to the nominal gain of 1. The maximum gain $g_{max}=1$ is maintained for $T_A < t \leq T$, during which the network is stabilized. When the hardware annealing is applied to a CNN by increasing the neuron gain $g(t)$, the transfer function can be described by $v_{yij}(t) = f(g(t)v_{xij}(t))$ or simply $y = f(gx)$. Note that the saturation level is still $y=+1$ or -1 and only the slope of $f(x)$ around $x=0$ varies. By using the normalized variables in a vector and matrix notation, the differential equation can be written as

$$C \frac{dx}{dt} = Ax - T_A x + b, \quad (1)$$

where $y = f(gx)$ and $b = Bu + I_b w$ for a constant vector $w = [1 \ 1]^T$. In (1), A and B are two-real N -by- N matrices determined by given cloning templates T_A and T_B , respectively. For the shift-invariant CNNs, they are real symmetric. Initially, the gain g is small so that the network can be linearized. For the piecewise linear function, the assumption is exact until some of neurons are saturated. In this case, $y = gx$ and (1) becomes

$$C \frac{dx}{dt} = Mgx + b, \quad (2)$$

where $M_g = gA - I_x$ for an N-by-N identity matrix I. The process of finding the optimal solutions takes place during the change of M_g from negative definite to indefinite matrix, as the annealing gain g increases.

III. VLSI Design

The first circuit is an unannealed CNN with fixed synaptic weights. To simplify the design, the current-mode approach [7] is used. The summation of weighted currents is simply done by a wired-ORing of all signals and the fixed weights can be accomplished by appropriate transistor sizing. A cell circuit consists of a constant input resistance negative-current conveyor followed by the piecewise-linear circuit. Figure 2 shows the schematic diagram of a simple current comparator using a cascade of two inverters. The input current I_y and reference current set by V_b are compared to produce an output voltage V_y^L . Figure 3 shows a detailed schematic diagram of a neuron cell. The synaptic weight is realized by $M_{11} - A_{4,1}$ for a_0 and $M_{15} - M_{16}$ for a_1 . Note that four copies of a current mirror are used to provide the weight for four neighboring cells. The feedback current, bias current, external input current, and those from the neighboring cells are summed at the input node, i.e., the drain terminal of $A_{4,1}$. Transistors $M_{29} - M_{30}$ provide a bias current which is set by the bias voltage V_{BI} . A simple current comparator circuit consisting of transistors $M_{23} - M_{28}$ produces the logic output $V_{yij}(L)$ which represents the sign of the neuron output.

An annealed CNN cell consists of a summing circuit, an analog multiplier, and a nonlinear function circuit. The synaptic weights are digitally programmable through binary-weighted current switches. For programmable-weight networks, the current-mode circuits also provide the simplicity over voltage-mode circuits because the number of cells is much smaller than the number of synapse weights for $r \geq 1$. The hardware annealing is performed by the pre-multiplication of the state v_{xij} by the gain control g before the nonlinear function $f(\cdot)$ takes place. Thus an analog multiplier is placed between the summing circuit and nonlinearity circuit as shown in Figure 4. Since g is positive, the two-quadrant multiplier is employed. The double-MOS differential resistor circuit [10] operating in triode region can be used as the analog multiplier. Current inverter can be used at the input stage of the multiplier to have a constant input impedance.

The complete schematic diagram of a neuron cell for an annealed CNN is shown in Figure 5. The nonlinear sigmoid function is accomplished by a simple transconductor consisting of a differential amplifier as indicated in Fig 5. The value of differential transconductance $g_m = (K I_0 (W/L))^{1/2}$ is relatively small in accommodating the normalized linear operating region $-1 \leq x \leq 1$ for the input range of $|x| \leq |x_{max}| \sim 10$. Here, I_0 is

the bias current and W/L is the geometric aspect ratio of the differential-pair transistors. Notice that the situation remains unchanged for increased I_0 because it also increases the saturated output levels. Therefore, a weak positive feedback is applied to increase the transconductance value without increasing the (w'/l) ratio of M_{17} and M_{18} . The transistors $M_{20} - M_{23}$ in saturation determine the feedback factor α , $0 \leq \alpha \leq 1$,

$$\alpha = \frac{(W/L)_{M21}}{(W/L)_{M20}} - \frac{(W/L)_{M23}}{(W/L)_{M22}} \quad (3)$$

Then, the transconductance at $V_1 - V_2 = 0$ becomes

$$g_m = \frac{g_m(\alpha=0)}{1-\alpha} \quad (4)$$

A binary-weighted current source array with the capability of four-quadrant multiplication is shown in Figure 6. By swapping the inputs I_1 and I_2 through the MSB bit, the polarity of the output I_W can be changed. The magnitude of the multiplication is done by $(n-1)$ LSB bits. Here, $n = 5$ and the sizes of transistors for weighting are chosen such that $|I_W| \leq (2 - 2^{-3})|I_{diff}|$, where $I_{diff} = I_1 - I_2$, in a step of $0.125 I_{diff}$. Because the current mirrors are used several times, it is important to match them as closely as possible through a careful layout design. The synapse weight for the self-feedback $A(i,j; i,j)$ must be a positive number greater than one. Thus, only four control bits are used for this synapse and, with the addition of constant factor of one, the range of output current is given by $I_d \leq I_W \leq (5 - 2^{-2})I_{diff}$ in a step of $0.25 I_{diff}$.

The proposed annealed VLSI CNN can include smart-pixel configurations. The incoming information is acquired by photo-sensitive diodes or transistors as reported in [11, 12].

IV. Simulation and Conclusion

SPICE simulation results of a variable-gain neuron for several annealing gain value are shown in Fig. 7. Figure 8 shows the SPICE simulation results of state and logic output voltages in a 4-by-4 CNN during four operation intervals. The cloning templates used are

$$T_A = \begin{bmatrix} 0 & -0.5 & 0 \\ -0.5 & 2 & -0.5 \\ 0 & -0.5 & 0 \end{bmatrix}, \text{ and } T_B = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad (5)$$

In each operation, the hardware annealing is applied for $0 \leq t \leq 4.5 \mu s$ with an initialization period $0.5 \mu s$ and $g_{min} = 0.005$. A CNN chip with 5×5 neural cells is designed and fabricated in a $2.0 \mu m$ CMOS technology through MOSIS Services. The die photo is shown in Fig. 9

A continuous-time CNN with annealing capability is designed. The circuits with digital-programmable synapses

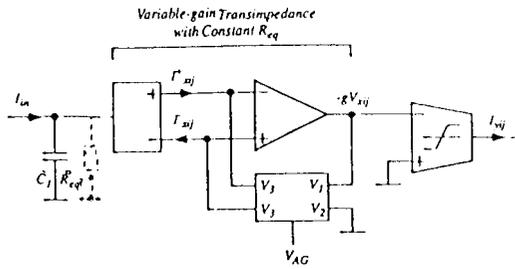


Figure 4: Variable-gain neuron cell for hardware annealing.

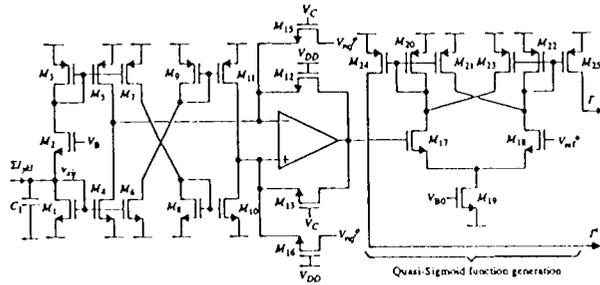


Figure 5: Complete schematic diagram of a variable-gain neuron cell.

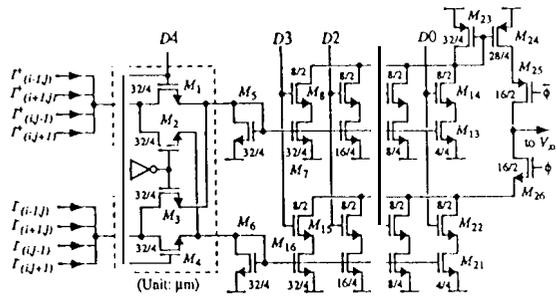


Figure 6: Circuit schematic of digitally-programmable synaptic weight.

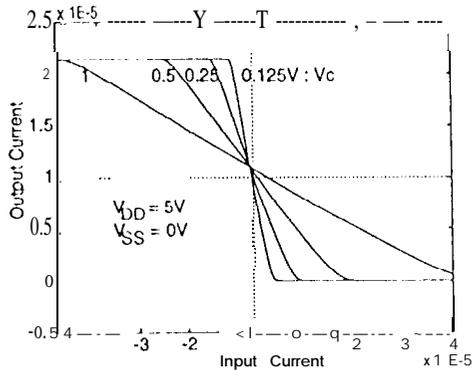
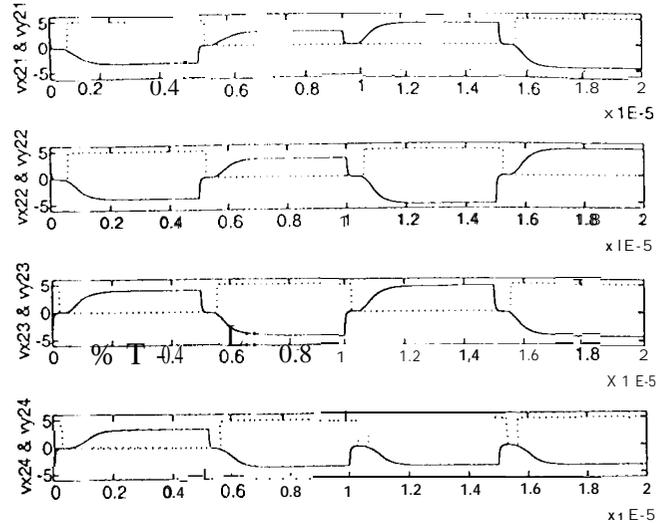


Figure 7: SPICE simulation results of variable-gain neuron for several annealing gain values.



initialization: 0.5 usec., operation: 4.5 usec.

Figure 8: Simulated state and logic output voltages of 4 cells in 2nd row. (solid lines: state voltages, dotted lines: logic output voltages)

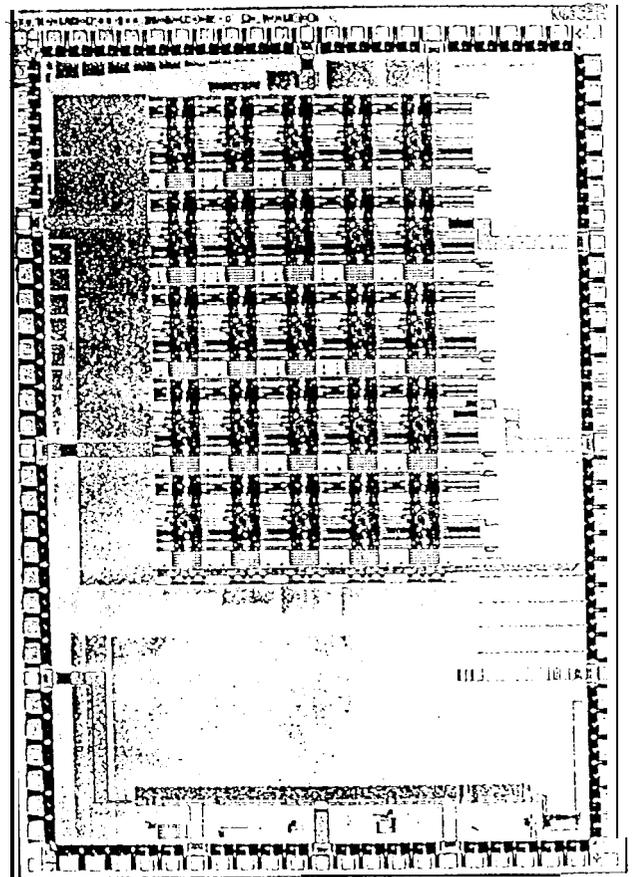


Figure 9: Die photo of the 5 x 5 CNN chip.

and flexible digital interface are included. Operation of CNN is verified by the SPICE simulation for different cloning templates.

Acknowledgement

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References

- [1] L. O. Chua, L. Yang, "Cellular neural network: Theory," *IEEE Trans. on Circuits and Systems (T- CA S)*, vol. 35, pp. 1257-1272, Oct. 1988.
- [2] A. Cichocki, R. Unbehauen, *Neural Network for Optimization and Signal Processing*, New York, NY; John Wiley & Sons, 1993.
- [3] L. O. Chua, L. Yang, "Cellular neural network: Applications," *IEEE Trans. on Circuits and Systems*, vol. 35, pp. 1273-1290, Oct. 1988.
- [4] T. Roska, J. Vandewalle, Eds., *Cellular Neural Networks*, West Sussex; John Wiley & Sons, 1993.
- [5] H. Halonen, V. Porra, I. Roska, L. O. Chua, "Programmable analog VLSI CNN chip with local digital logic," *Proc. IEEE Int '1. Symposium on Circuits and Systems*, pp. 1291-1294, 1991.
- [6] J. M. Cruz, L. O. Chua, "A CNN chip for connected component detection," *IEEE T-CAS*, vol. 38, pp. 812-817, July 1991.
- [7] A. Rodriguez-Vazquez, et al., "current-mode techniques for the implementation of continuous- and discrete-time cellular neural networks," *IEEE T-CAS II*, vol. 40, pp. 132-146, Mar. 1993.
- [8] J. E. Varrientos, E. Sanchez- Sinencio, J. Ramirez-Angulo, "A current-mode cellular neural network implementation," *IEEE T-CAS II*, vol. 40, pp. 147-155, Mar. 1993.
- [9] I. A. Baktir, M. A. Tan, "Analog CMOS implementation of cellular neural networks," *IEEE T-CAS II*, vol. 40, pp. 200-206, Mar. 1993.
- [10] M. Ismail, S. V. Smith, R. G. Beale, "A new MOSFET-C universal filter structure for VLSI," *IEEE Jour. of Solid-State Circuits*, vol. 23, pp. 183-194, Feb. 1988.
- [11] C. Mead, *Analog VLSI and Neural Systems*, Addison Wesley: Reading, MA, 1989.

- [12] S. Espejo, A. Rodríguez-Vázquez, R. Domínguez-Castro, J. L. Huertas, E. Sánchez-Sinencio, "Smart-pixel cellular neural networks in analog current-mode CMOS technology," *IEEE Jour. of Solid-State Circuits*, vol. 29, pp. 895-905, Aug. 1994.

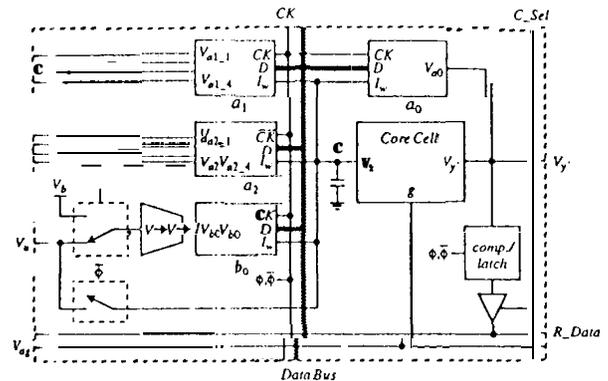


Figure 1: Block diagram of a CNN cell.

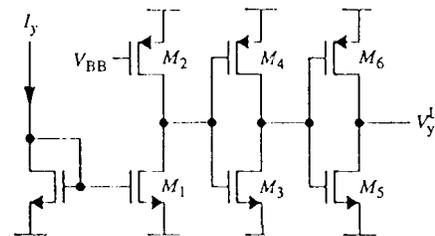


Figure 2: Current comparator for logic output of a cell.

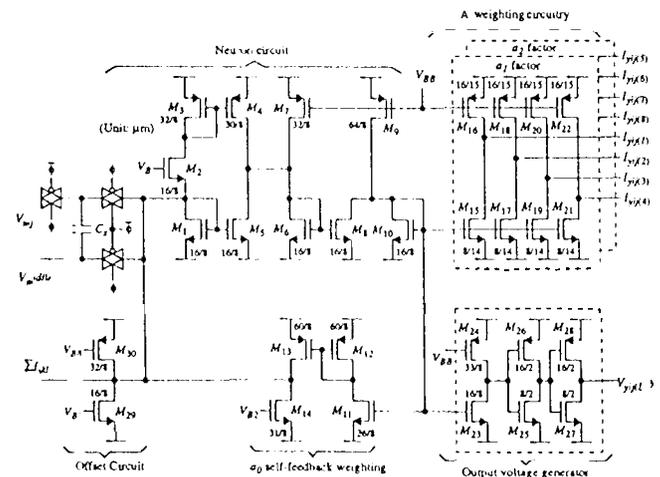


Figure 3: Circuit schematic of a fixed-weight CNN.

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COMMENTS: A continuous-time cellular neural network with annealing capabilities.

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