

Using Commercial Semiconductor Technologies in Space¹

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Introduction

The increase in capitalization cost of semiconductor fabrication facilities has gradually changed the economics of semiconductor production, [1] with the result that few manufacturers can afford to produce devices for special niche markets, such as radiation-hardened devices.^{††} This factor, coupled with the recent decline in the military semiconductor market, has increased the pressure to adapt unhardened commercial devices for space applications.

This paper discusses recent results from the Jet Propulsion Laboratory that provide insight into behavior of commercial devices in space environments, along with the types of controls and tests that are required to successfully use them in space applications. Three issues are particularly significant: enhanced damage in bipolar devices at low dose rate; the older problem of lot-to-lot variations in the radiation response, which is still critically important; and single-event hard errors, which are likely to increase in importance as digital devices are scaled to smaller dimensions.

Dose Rate Effects in Bipolar Technologies

The discovery that some bipolar device technologies exhibit more damage at low dose rates [2-4] greatly increases the difficulty of testing and qualifying these devices for space applications. The problem is most severe for special pnp devices used in many linear circuits, where damage can be 6-7 times greater at low dose rates than at high dose rates. [2] These pnp devices remain sensitive to dose rate at very low rates -- ≈ 0.002 to 0.005 rad(Si)/s -- which are impractical for routine testing, because of the extremely long test times required. Note that npn devices are generally not sensitive to dose rate effects below approximately 1 rad(Si)/s. Thus, circuits which use both types of components may exhibit different failure modes at low and high dose rates because of the different amount of relative damage that occurs in the two types of components at low dose rates.

^{††}The research in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

^{†††}A limited number of part types is available from hardened or radiation-tolerant lines, and it is preferable to use such devices for space applications because their radiation hardness is explicitly controlled. When commercial parts are used, the user must ensure that testing and control of the parts is sufficient to detect devices with marginal radiation capability.

As indicated by previous tests of voltage regulators, (.) enhanced damage can vary substantially between manufacturers of the same part type, and it is sometimes possible to select a specific manufacturer with less severe dose rate behavior. Figure 1 shows recent results for LM111 voltage comparators, which use substrate pnp input transistors, procured from three different vendors, and tested at two widely different dose rates. For two of the manufacturers, damage of the input transistors is about six times greater at low dose rates. Devices from the third manufacturer show only a small increase in damage at the lowest dose rate, even though the geometry of the input transistors of this vendor are identical to that of the vendor with the highest damage at low dose rates. Thus, in this instance it is possible to select a vendor with little dose rate dependence, and thereby avoid the need for costly testing at very low dose rates. However, tests at intermediate dose rates -- ≈ 0.02 - 0.05 rad(Si)/s -- would still be required during characterization tests in order to verify that dose rate effects are sufficiently low.

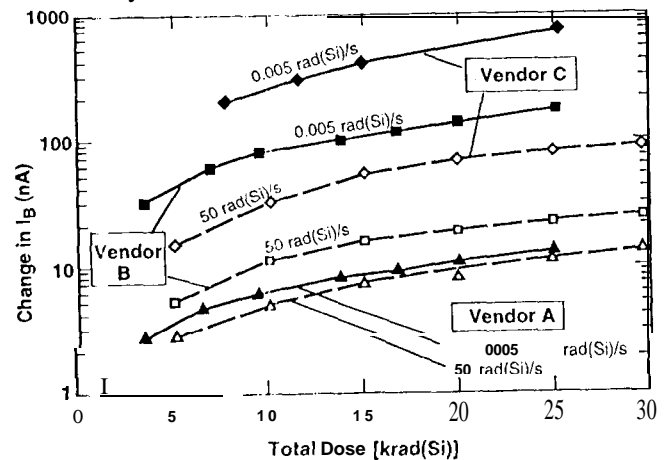


Figure 1 Total dose degradation of LM 111 comparators from three manufacturers at high and very low dose rates.

Although LM111 comparators produced by this manufacturer were relatively insensitive to total dose and exhibited only a slight dose rate effect, this was not true for OP42 op-amps produced by the same manufacturer. The OP42 uses a similar process that includes compatible JFETs along with the usual bipolar components. The manufacturer's data sheet includes representative data showing that its para-

meters are only slightly affected by total dose out to 1 Mrad(Si), based on many years of testing at high dose rate. However, tests at low dose rates produced an entirely different result. As shown in Figure 2, extremely large changes in input offset voltage occurred in this device at relatively low levels that were only apparent during low dose rate tests. Similar results were obtained for two different production lots, fabricated in 1988 and 1994. The degradation was so severe that the part was removed from applications in the Cassini spacecraft. Initial modeling of the device indicates that degradation of internal pnp transistors in the second stage are responsible for the large change in offset voltage. A more detailed analysis will be included in the full paper.

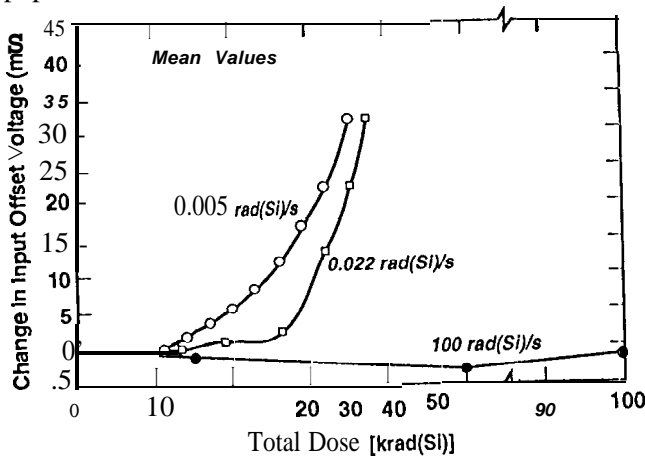


Figure 2. Offset voltage degradation of the OP42 op-amp at high and low dose rates. The large changes in offset voltage that occurred at low dose rates were not evident in tests under high dose rate conditions.

The difference in the behavior of pnp and npn devices at low dose rates makes it impossible to properly account for dose rate effects by applying a guardband factor to high dose rate data. The OP42 results show that different mechanisms can appear at low dose rates which are not at all evident at high dose rates. One way to deal with this problem is to require tests at two different dose rates, selecting the lower dose rate so that it is sufficiently high to allow tests to be completed in days or weeks instead of the extremely long time periods imposed by the very low dose rates discussed above. JPL has implemented this approach for several devices, using 0.02 rad(Si)/s for the lowest dose rate. Data for several device technologies will be provided in the full paper, along with a discussion of methods to select appropriate dose rates, and comparison of test results for data as low as 0.002 rad(Si)/s. Alternative approaches, such

as irradiation at elevated temperature, will also be discussed.

Scaled MOS Technologies

Highly scaled MOS devices are extremely competitive, and production lines are frequently upgraded to provide technical and cost advantages. These changes can affect their radiation response, and it is necessary to evaluate the radiation performance of these devices on a regular basis in order to ensure compliance with radiation requirements. For example, some manufacturers use on-chip voltage regulators to provide a lower operating voltage for internal circuitry. The internal voltage is usually not specified, and may be lowered for future design upgrades with smaller feature size

Device scaling can affect radiation behavior in several ways, including total dose sensitivity, which remains an important issue; SEU; latchup sensitivity; and the new problem of single-event hard errors.[5-8] The latter issue is particularly important because it may limit the effectiveness of system solutions, such as error-detection- and-correction, that are often used to correct single-event upset effects.

Total Dose Effects. Recent test data shows that field oxide leakage often dominates total dose degradation in advanced MOS devices, [9] and hence total dose hardness levels have not followed first-order scaling predictions based on gate oxide sensitivity. Even though gate oxide threshold voltage shifts are expected to decrease as gate oxide thicknesses are reduced, second-order effects become increasingly important, particularly for devices with reduced power supply voltage and reduced internal operating margins.[10] The increased sensitivity of scaled devices to threshold voltage will generally make them more sensitive to small variations in threshold voltage than older devices with 5 V power supplies, which have much larger operating margins.

An additional factor to be considered is the statistical variation of threshold voltage on devices from a single chip, which results primarily from statistical fluctuations in the number of dopant atoms. Figure 3 shows the spread in retention times for a 16 Mb DRAM; the distribution is consistent with a three-standard deviation range of 26 mV in threshold voltage of internal transistors, and agrees closely with predictions of the effect of doping atom fluctuations. [11]

The voltage fluctuation remains nearly constant after irradiation, further corroborating the assumption that internal threshold voltage variations are responsible for the spread in retention times.

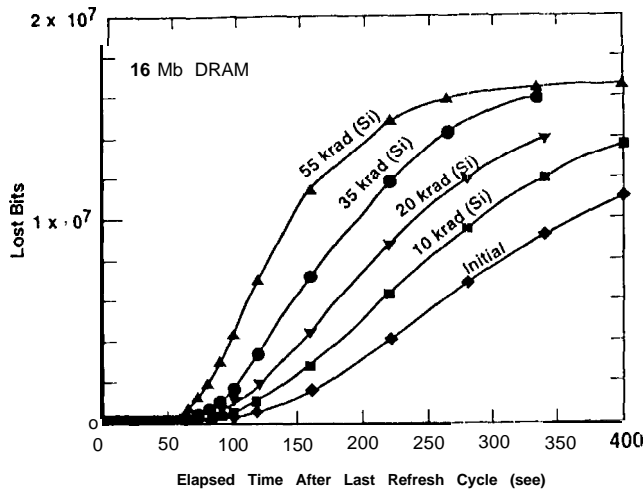


Figure 3. Lost bits vs. refresh delay for a 16 Mbit DRAM at various dose rates. The dispersion is due to threshold voltage variations of pass transistors within the DRAM array.

These variations will cause a small number of transistors within a large chip to fail at much lower total dose levels than average transistors on the chip, and can only be detected by implementing very thorough test methods. As shown in Figure 3, the effect is already apparent in the radiation response of devices with feature sizes in the 0.6 to 0.8 μ range, and will be more severe as devices are scaled further because of larger statistical fluctuations and reduced internal operating margins.

Hard Errors. Two types of single-event hard errors have been discovered, one involving microdose deposition from a single ion (or a small number of single ions) in the gate region, [5-7] and a second which appears to cause catastrophic gate failure, similar to gate rupture. [8] The second mechanism is particularly important because it causes catastrophic failure, not just a small increase in subthreshold leakage, and may affect devices other than storage arrays, such as random logic in microprocessors.

Initial results have shown that device scaling lowers the threshold for the onset of the second mechanism. Figure 4 shows the dependence of the failure threshold LET on gate oxide field strength for two devices from the same vendor with different oxide thickness. The process with the reduced oxide thickness is a "shrunk" version of the initial design that is electrically equivalent, and supersedes the original version. The slope is very close to the square root dependence that was established for gate rupture in power MOSFETs, and suggests that the threshold LET for this mechanism will continue to decrease as devices are scaled further, nearing the

iron threshold as devices are scaled to the third generation (2.5 V power supplies). 64 Mb DRAMs with a gate oxide thickness of 110 Å have recently been obtained by JPL that are representative of 3.3 V technology, and hard error results for these devices will be included in the final paper to provide additional data on the effects of scaling on the second type of hard error.

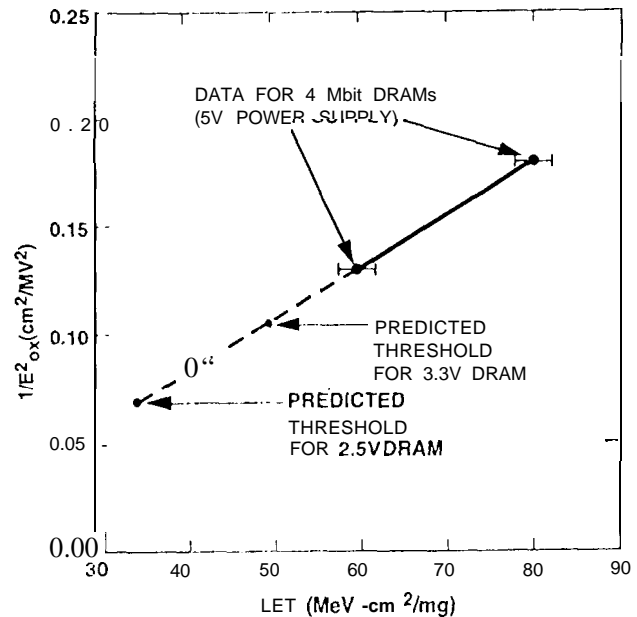


Figure 4. Dependence of threshold LET for gate rupture from heavy ions on scaled DRAM technologies.

Mixed-Signal Devices

Most spacecraft use analog-to-digital converters in key interface applications. Great strides have been made in the design of A/D converters, increasing their accuracy and precision. Two different technologies are available: (1) BiCMOS designs, which employ conventional architectures, and selectively use bipolar devices in key circuit areas to decrease offset voltage and simplify design of input amplifiers and comparators; and (2) full CMOS designs, some of which employ complex internal calibration and error correction methods to overcome the inherent limitations of CMOS devices in linear amplifiers. Both technologies generally have much higher voltage ratings than conventional digital CMOS circuits, which in turn requires thicker gate and field oxides. Because of the thicker oxides, these devices are generally far more sensitive to ionizing radiation than digital technologies, and anneal relatively quickly after irradiation. They are also sensitive to rebound effects.

Somewhat surprisingly, the dominant failure modes are generally not small deviations in the conversion accuracy, but global failure modes such as increase in leakage current, or changes in offset of internal amplifiers and reference circuits. Frequently the first indication of failure is that of stuck bits in the digital output stage. At high dose rates commercial devices typically fail between 3 and 10 krad(Si), but often recover after initial irradiation within a few hours. However, rebound effects may cause them to have a different response at low dose rates. For CMOS devices standard rebound testing using high-temperature annealing is satisfactory, [12] but this approach has not been verified for BiCMOS devices, which may be affected differently because of the interplay between bipolar and CMOS devices. Dose rate effects in bipolar devices may also limit the applicability of accelerated temperature for rebound testing of BiCMOS devices.

These types of A/D converters exhibit different failure mechanisms when they are irradiated at low dose rate. Specific failure modes depend on the specific device architecture. Internal reference voltages are typically one of the key parameters, even though buried zener references are generally used. Figure 5 shows the change in reference voltage for three different comparator technologies. Changes in the two BiCMOS devices are sufficient to cause them to fail specifications at levels below 10 krad(Si). Although the CMOS converter exhibits much larger changes, the internal calibration scheme partially compensates for the degradation. This will be discussed more fully in the complete paper, along with comparisons of tests at high and low dose rates for these devices.

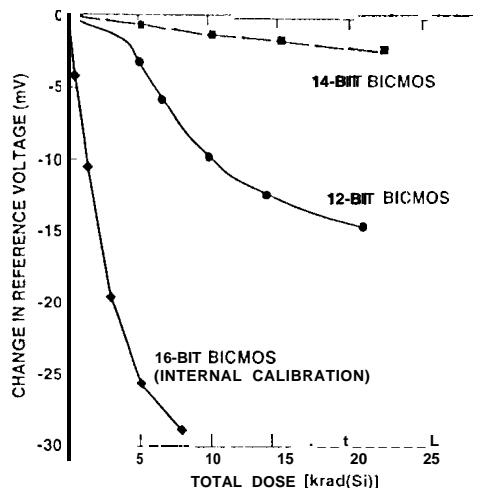


Figure 5. Changes in reference voltage after total dose degradation for three different A/D converter technologies

Discussion

The wide range of device functions and increased performance of commercial devices provides advantages in designs that are sensitive to weight and power, particularly in small spacecraft. However, device complexity and new radiation problems that are exacerbated by device scaling make it more difficult to verify that commercial designs will work satisfactorily in space. Careful attention must be given to device failure modes and test methods, as well as variations in the response of devices produced at different time periods. Increased emphasis is needed on low dose rate testing in order to establish a better technical framework for hardness assurance and qualification of these technologies, as well as on new effects such as single-event hard errors that must be accounted for when new technologies are applied in space

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