Communication interface for SAMS

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Abstract

This paper describes the architecture and current implementation of a STD Bus accelerometer /LonTalk communication interface. The interface is a part of the Shuttle Space Acceleration Measurement System (SAMS), a data acquisition unit. The goal of this development was to design and build a flexible interface between flight instruments and the analog input of an existing conventional recording unit. The control and recording unit is designed as a set of boards on a STD Bus. The digital control interface communicates with the control and recording unit through an ALTERA Flexible Logic Element Matrix (FLEX) device.

The ALTERA FLEX device has been chosen to implement STD Bus/ LonTalk communication interface because:

- FLEX devices have very high density logic integration, which saves system weight and space.
- FLEX devices have very low power consumption, which is critical for flight equipment design.
- MAX+ PLUSH software allows a very short development cycle.

Introduction

As part of a NASA microgravity accelerometer program we have developed a Digital Communication Interface (DCI) STD module that is functionally transparent to the Space Acceleration Measurement System(SAMS) control and recording unit. 'l'he compatibility is such that once our DCI module is installed, no subsequent modification to the hardware of the SAMS is necessary . Our DC1 module facilitates a variety of instruments that can be provided with communication and power (5 or +/- 15volts).

The instruments can communicate with the SAMS through the DCI unit (point-to-point communications) as well as with each other (direct peer-to- peer communication). The SAMS unit can accommodate a 2 Kbytes/sec data collection rate. Neither SAMS nor DCI units have to be either modified or requalified when a new instrument or new communication arrangement is introduced.

The DCI shuttle interface is the first space qualified unit that incorporates the peer-to-peer communicating microcontrollers that can be used to build a "smart" sensor networks. The advantages of the network are: modular approach to design and development, ease of last minute changes. potential for last minute substitutions. Communication microcontrollers may be coupled to existing instrument computers or even to the analog outputs of instruments.

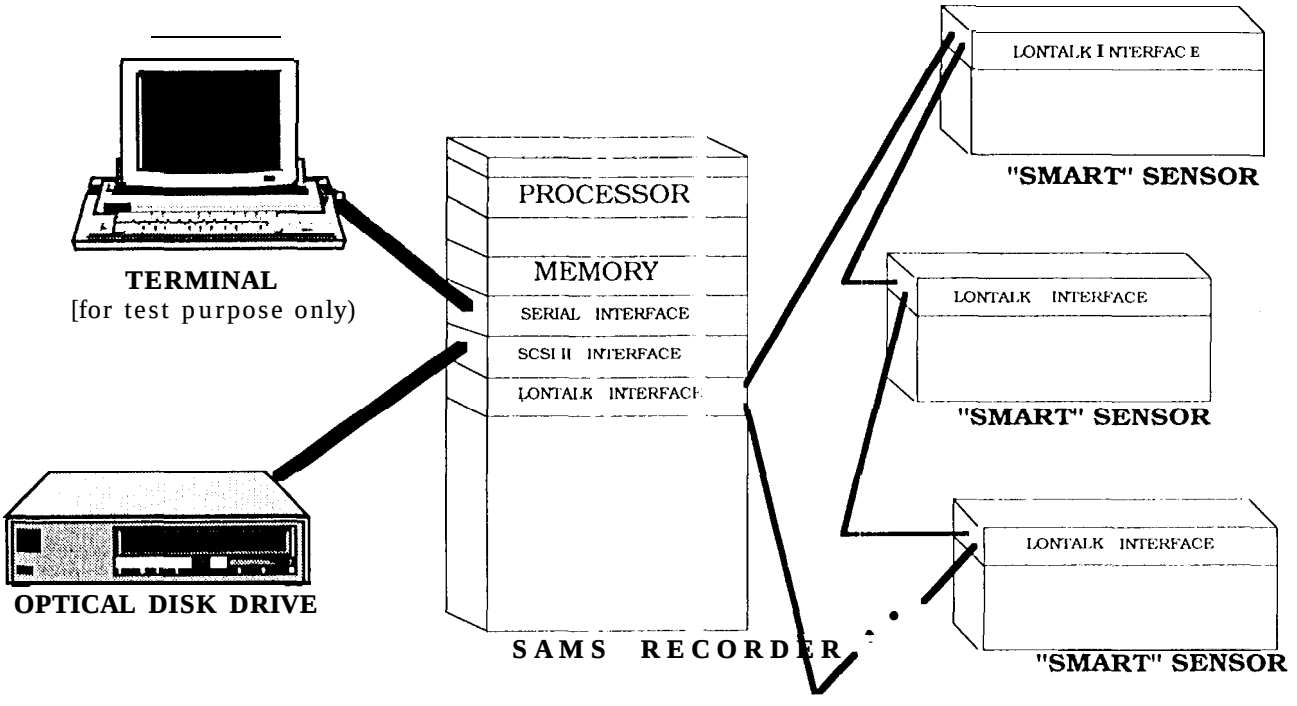


Fig. 1 SAMS System

SAMS System

As shown in Figure 1, the SAMS system consists of a recorder and several "smart" sensor nodes. The recorder is a STD card cage with:

- processor board
- memory board
- SCSI 11 interface board, hooked up to an external storage device(for example, an optical disk drive)
- . serial interface board, which provides for connection to a terminal for test and diagnostics (for example, RS-232)
- LonTalk interface board (1X1), which provides for connection of up to 32 different "smart" sensor nodes.

The "smart" sensor node consists of

- sensor
- signal conditioning{<
- A/D converter
- communication processor, which supports LonTalk protocol
- transceiver.

"Smart" sensor nodes arc capable of self-calibration, digital conditioning, compensation, linearization, measurement reliability, and health monitoring.

This concept was chosen to achieve flexibility, performance, low cost, and low mass.

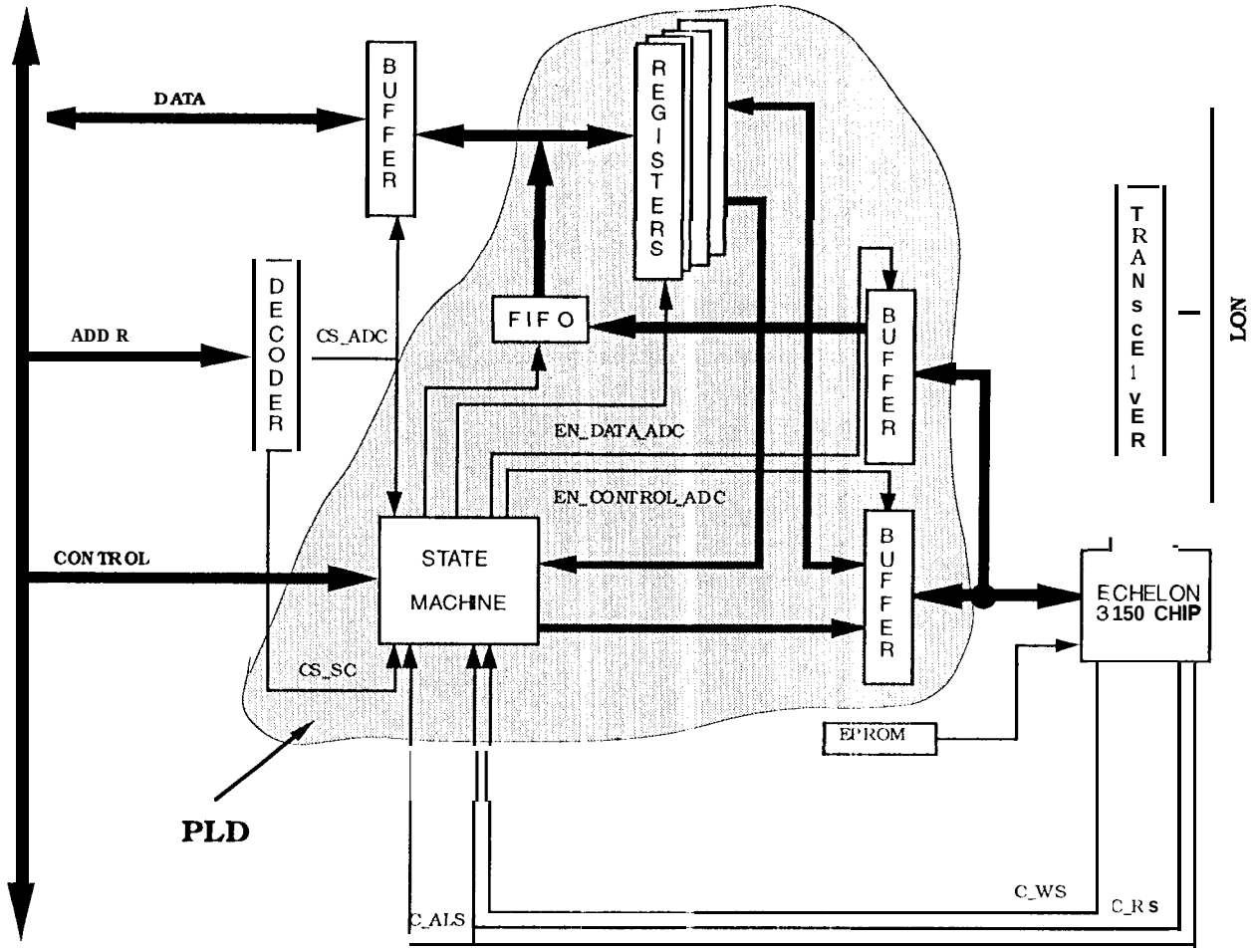


Fig. 2 DCI Board

DCI Board

As shown in Figure 2 the DCI has several major elements:

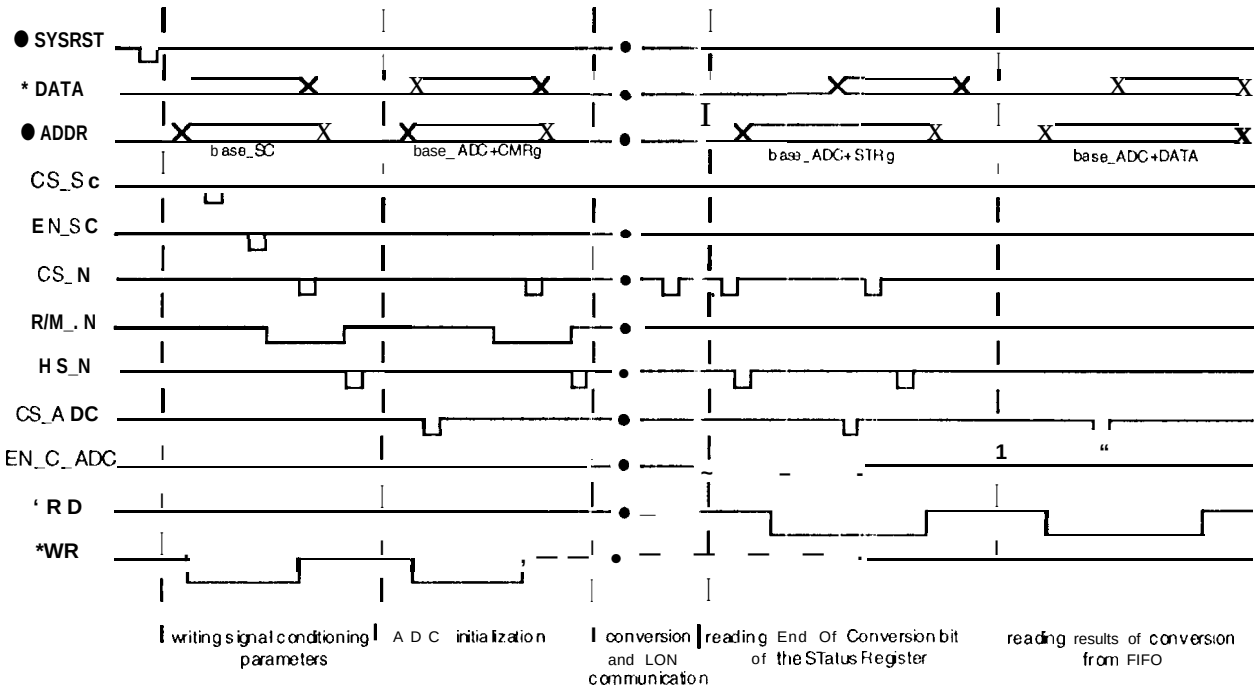
- LonTalk interface
  - processor (Echelon 3150)
  - EPROM
  - transceiver
- STD side
  - data buffer
  - address decoder
- PLD (ALTERA FLEX **EPF81 1 88)**
  - FIFO
  - state machine
  - set of buffers and registers

The 8 x 8 FIFO is used to store four sixteen-bit words. Several status registers are used to provide STD and LonTalk communication protocols. The STD and Echelon 3150 data lines are hi-directional, so input/output buffers are provided. The Echelon 3150 connects to application-specific external hardware via eleven 1/0 pins, configured in this described application as MUX131JS.

The program control on STD bus is provided by the host CPU which can be either 8088 or 8085 microprocessors. Maximum clock rates are 8 MHz and 6 MHz respectively. One average instruction needs 10 CPU clocks. An average write command is executed by 10 instructions which take approximately 40 µsec and an average read command is executed by 25 instructions which take approximately 100 µsec.

In the described application , the Echelon 3150 is configured to use 90 ns memory (EPROM in Fig. 2). Communication media for LonTalk is twisted pair, which provide a 1.25 Mbps channel. The Echelon 3150 operates over a 10 MHz clock.

Analysis of the STD bus/ LonTalk interface timing diagram (Fig.3) shows that the ALTERA FLEX device is a good candidate for implementing a major part of this interface.



* **Bold -** STD **Bus signals**

Fig.3

Conclusion

The ALTERA FLEX family also provides some features which arc very important for this specific application. These are:

- very high density logic integration, which saves system weight and space
- very low power consumption, which is critical for flight equipment
- MAX+PLUS software tools, which allows a very short development cycle

The ALTERA FLEX device EPF81 188 MC240 was chosen to implement this design, Approximately 30% of the available part space was used.

Acknowledgment

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