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Edge Processing and Formation for High- T_c SNS Josephson Junctions and Circuits* J.B. BARNER, A.W. KLEINSASSER (AN) K.A. DELIN, Jet Propulsion Laboratory, California Institute of Technology, Center for Space Microelectronics, Pasadena, CA 91109, USA, B.D. HUNT, Westinghouse STC, Pittsburgh, PA 15235—We are investigating a variety of tapered-edge formation processes in $YBa_2Cu_3O_{7.8}$ (YBCO) and insulating oxide thin films, such as Sr_2AlTaO_6 or $SrTiO_3$, for use in all-epitaxial SNS devices and circuits. A critical part of any edge formation process is the ability to grow epitaxial layers afterwards. Hence, the edge must be shallow to permit epitaxial growth of subsequent oxide films and it must be free of processing residues. We have introduced a number of process variations to give the desired results and improve upon the standard photoresist ion-milling mask technique. Devices fabricated with and without groundplanes and utilizing normal layers of Co- and Pr-doped YBCO display RSJ-like behavior. Comparison of devices fabricated with the different processes and their dependence on process variation will be presented.

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LTS Junctions, HTS Junctions

