

Section 4

Device Responses and Effects



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outline

Introduction and Review of Device Structures

Total Dose Effects

Displacement Damage

Transient Ionization Effects

Single-Event Effects

Latchup from Transient Ionization and Heavy Ions

Introduction to the Commercial Device Problem

Introduction

This section of the short course discusses radiation effects in semiconductor devices. This is a broad topic, and it is not possible to cover all aspects in a course of this length. The approach that will be used is to briefly review basic mechanisms and device responses, and to go into more detail for new topics, or topics such as latchup that have not been covered in as much detail in previous short courses. This assumes that most course participants are generally familiar with radiation effects in devices.

The five topics to be covered in the oral presentation are as follows:

Introduction

Total Dose Effects

Transient Ionization Effects

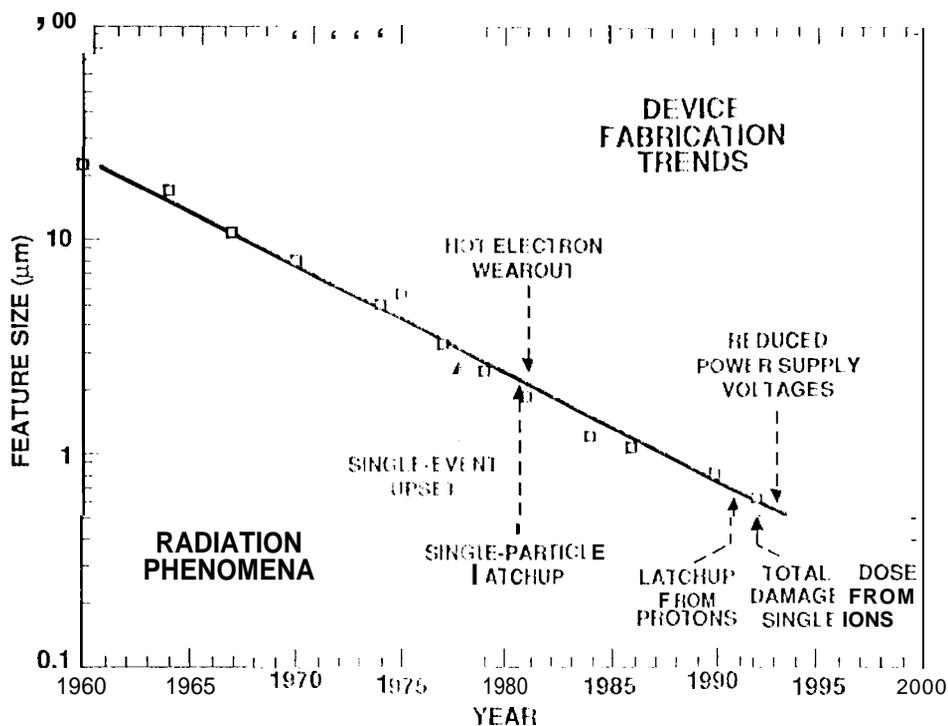
Single-Event Effects

Latchup

Introduction to the Commercial Device Problem

A sixth topic, neutron damage, is included in the notes for completeness, but was not covered in the oral presentation because of time constraints.

FEATURE SIZE TRENDS IN MICROELECTRONICS

*Feature Size Trends*

The radiation response of integrated circuit technologies has been heavily influenced by changes in technology, particularly in space environments. This figure shows the time and approximate feature size where various single-particle effects have become significant. Note particularly proton-induced latchup and two new permanent damage effects, microdose damage and gate rupture.

The data in this figure show when these phenomena were first discovered (generally in commercial technologies). Feature size alone does not determine susceptibility to these effects because of the importance of processing and layout details. However, the figure demonstrates how new effects evolve as device technology changes. New low-voltage technologies are expected to be even more sensitive to SEE phenomena.

Key Technical Issues

Charge Generation and Trapping in Insulators

- **Affects Both Bipolar and MOS "1 technologies**
- **Complicated Dependence on Bias Conditions and Device Structure**
- **Time Dependent**

Transient Charges or Photocurrents from Heavy Ions or Gamma Pulses

- **Upset Effects**
- **Latchup**
- **Destructive Effects**

Parasitic Elements Are Important for both Phenomena

- **MOS Structures in Bipolar Devices**
- **Bipolar Structures in MOS Devices**

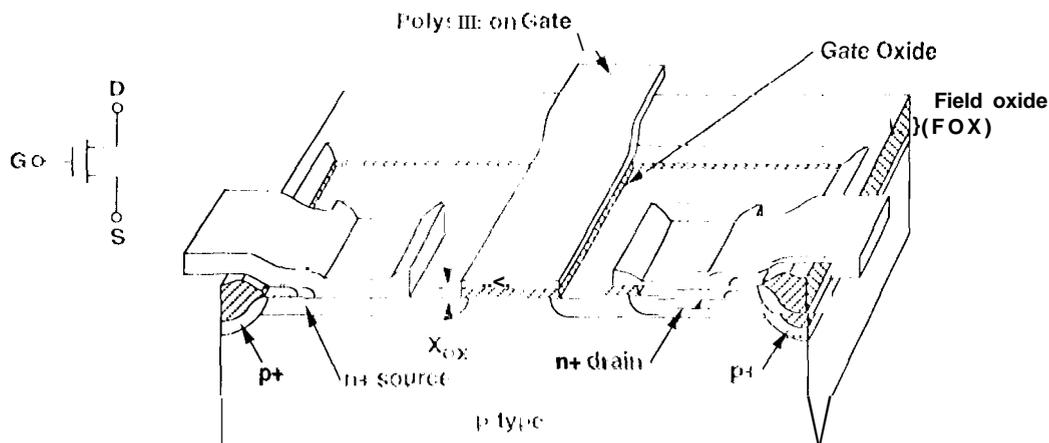
Key Technical Issues

Two basic radiation effects phenomena have proved to be particularly challenging as device technology has evolved: (1) charge trapping at the interface between silicon dioxide and silicon, which is present in most semiconductor technologies; and (2,) transient charge pulses or photocurrents generated by heavy ions and short-duration pulses of gamma radiation.

In order to understand these effects, it is necessary to examine some of the physical details of modern semiconductor devices. In many cases, the primary radiation effects problem occurs because of parasitic structures that are not directly related to the basic device performance. For example, charge trapping in the oxides at the surface of bipolar devices are the cause of ionization damage, and recent results have shown that the damage depends directly on dose rate for some technologies. A parallel example for MOS devices is the importance of parasitic bipolar structures in single-event upset and latchup. In general these parasitic structures are not well controlled in commercial processes, and this creates a great deal of uncertainty in evaluating the radiation response of commercial devices.

Radiation-hardened technologies are designed to take these effects into account, and generally specify maximum parametric changes or upset rates (details vary with the circuit technology and process). Developing "hardened circuit technology" requires a great deal of effort by manufacturers only in initially designing the process, but also in establishing process controls and hardness assurance techniques to make sure that the radiation response stays within prescribed limits.

Structure of an NMOS Transistor



- Operation depends on *majority* carrier flow from drain to source
- Gate oxide is directly related to device performance
- Parasitic field oxide is much thicker, and only loosely controlled

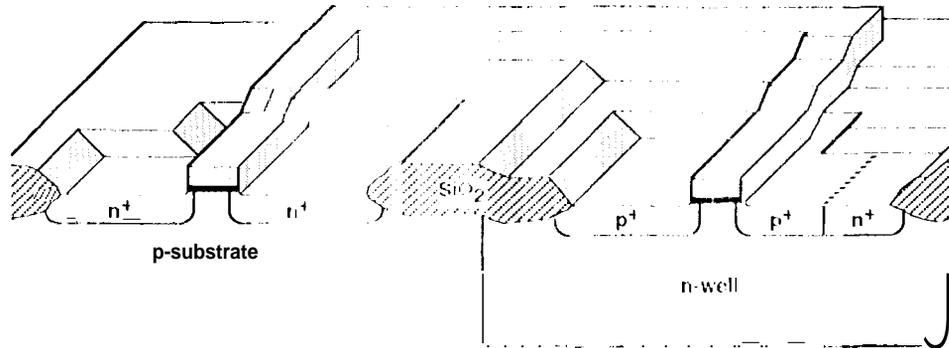
Structure of an NMOS Transistor

This figure shows an outline of an NMOS transistor. The basic operation depends on the flow of majority carriers from source to drain, moving in a lateral direction. The flow of carriers within this region depends on the voltage applied to the gate, which produces a field-induced junction in the bulk region under the gate. When a low gate voltage is applied, the field-induced junction depletes the bulk region under the gate, creating a high-resistance region between source and drain. For higher gate voltages, a conducting channel is produced, increasing the conductivity between the source and drain regions. The gate voltage for which the channel first begins to conduct is called the gate threshold voltage, V_T .

The gate threshold voltage is affected by trapped charge at the surface. As discussed later, this can be affected by ionizing radiation, which will then cause a change in V_T . Gate oxides in modern devices are 80-200 Å, which reduces their sensitivity to radiation damage compared to older technologies.

In addition to the gate oxide, most MOS transistors use a field oxide to provide isolation. The field oxide is much thicker than the gate oxide, 4500 to 8000 Å. Ionizing radiation can cause inversion in field oxides, resulting in very high leakage current. This is a very important failure mechanism in modern commercial devices. Hardened device technologies use special processing techniques to reduce gate threshold shifts in field oxides. They may also use special processing to improve the radiation hardness of gate oxides.

Topology of NMOS and PMOS Transistors in CMOS

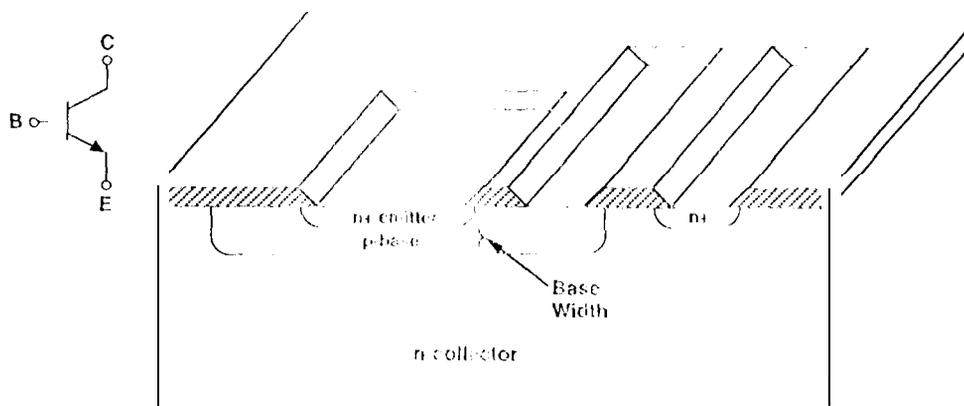


Topology of NMOS and PMOS Transistors in CMOS

This diagram shows the fabrication of NMOS and PMOS transistors in a junction-isolated CMOS circuit. NMOS devices are fabricated directly in the p-substrate, while PMOS transistors are fabricated in n-wells that are diffused into the substrate early in the processing sequence.

The circuit operation depends on reverse bias junction isolation between the well and substrate. This isolation technique is very important for transient radiation phenomena because photocurrents are produced within the depletion junction of the n-well/substrate junction that can have a large influence on device responses. As discussed later, this type of isolation also produces a parasitic p-n-p structure that can cause latchup. Other forms of isolation can be used that **1,111,** or eliminate the effects of parasitic p-n junctions in MOS devices, and such approaches are often used in hardened technologies.

Structure of a B polar Transistor



- Operation depends on *minority* carrier transport through base region
- Oxides are used only as barriers during processing steps

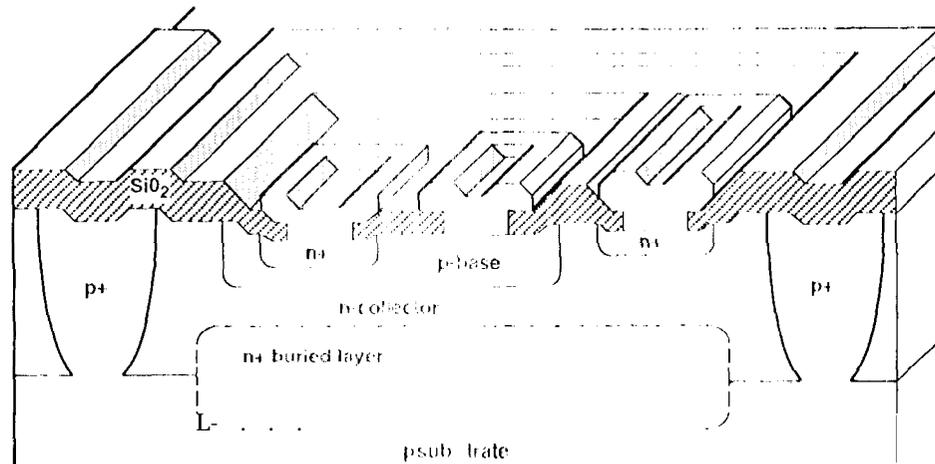
Structure of a Bipolar Transistor

This diagram shows the basic structure of a bipolar transistor. Operation depends on the transport of *minority* carriers injected from the emitter-base junction through the narrow base region, to the collector. The magnitude of the collector current depends on the base current (provided by external circuitry). The ratio of collector current to base current is the common-emitter current gain, β_{FE} , and it is the **fundamental parameter** that is usually used to describe transistors.

Note that because transistor operation depends on minority current flow through the base, transistors are far more sensitive to displacement effects from protons and neutrons than MOS transistors. Devices with wide base regions (lower values of unity-gain frequency response, f_T) are more sensitive to displacement effects.

Just as parasitic p-n junctions were important for some types of radiation effects in MOS devices, parasitic oxide structure in bipolar devices can have a large influence on the radiation response of bipolar devices. The oxides used in bipolar devices are less well controlled than oxides in MOS devices and are only necessary to provide barriers during **processing steps**. These oxides are typically very thick, and may be grown in several successive processing steps.

Topology of a Junction-Isolated Bipolar Transistor



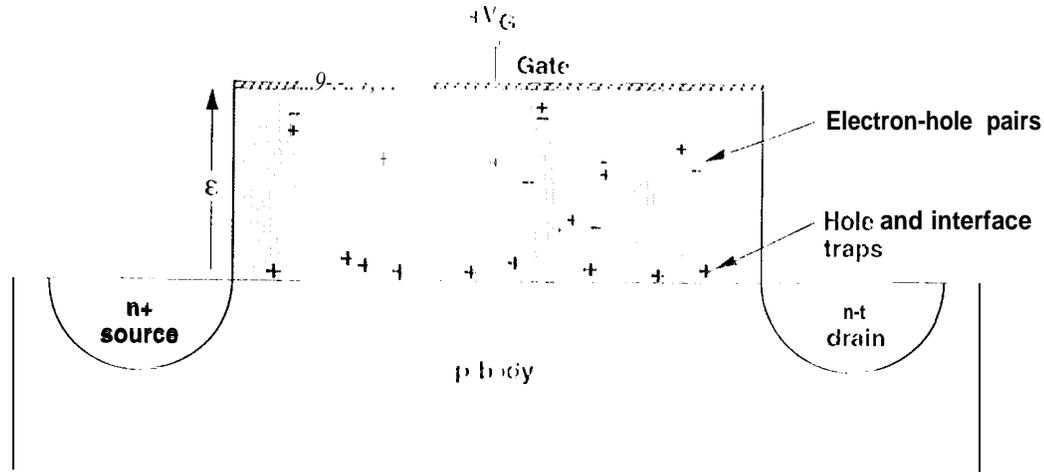
Junction-Isolated Bipolar Transistor

This diagram shows the topology of a junction-isolated bipolar transistor. Note the added complexity compared to the basic structure in the previous figure. Junction isolation is done early in the processing flow by selectively diffusing p+ regions around "islands" in the epitaxial n-layer that initially exists over the entire wafer. The p-dopant diffuses through to the substrate, creating isolated n regions in the wafer that eventually become the collector of npn transistors. Just as in CMOS, operation of these devices depends on the reverse bias of a parasitic junction, in this case from the n-collector to the substrate.

The isolation junction creates a parasitic pnp transistor, formed by the base, collector, and substrate, which can be turned on by transient photocurrents. Generally the large area precludes turn-on of this transistor by heavy ions, but this may no longer be true for highly scaled devices. Four-region structures are also present in junction-isolated bipolar devices that can result in latchup.

This form of junction isolation requires a large spacing between different collector islands because of the depletion width of the two reverse-biased junctions. (The depletion regions cannot touch, or the structure will break down because of punch through). High-density bipolar devices usually use a different approach for lateral isolation, such as oxide sidewall or trench isolation, in order to reduce the collector-collector spacing. However, they usually retain junction isolation in the vertical direction.

Charge Trapping in Silicon Dioxide



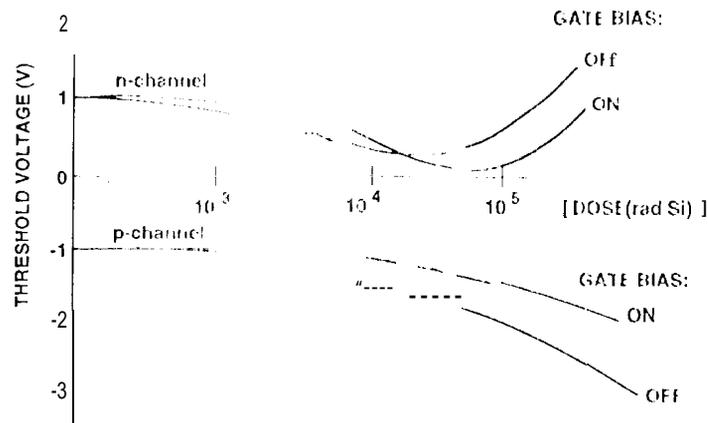
- Ionization produces electron-hole pairs in oxide
- Holes migrate to interface
- Hole transport depends on electric field

Charge Generation

Ionizing radiation produces electron-hole pairs in insulators and semiconductors. This figure shows charge within the very high resistance gate of an MOS transistor. The electrons have high mobility, and are quickly swept out to either the gate electrode or the interface. Holes have much lower mobility, but will migrate to either the gate or the interface in time periods of milliseconds to seconds. Their transport time depends on the gate oxide thickness and the applied field. Some of the holes will recombine within the gate oxide. A fraction of the holes that reach the silicon-silicon dioxide interface will be trapped. Interface traps can also be created which affect devices in different ways than hole traps.

Although this example involves an MOS transistor, the same basic process applies to any silicon/silicon dioxide interface, including the oxides in bipolar transistors.

THRESHOLD VOLTAGE VS. TOTAL [IC)SE. FOR N-AND P-CHANNEL MOS TRANSISTORS



Delta V_T for n- and p-Channel MOSFETs

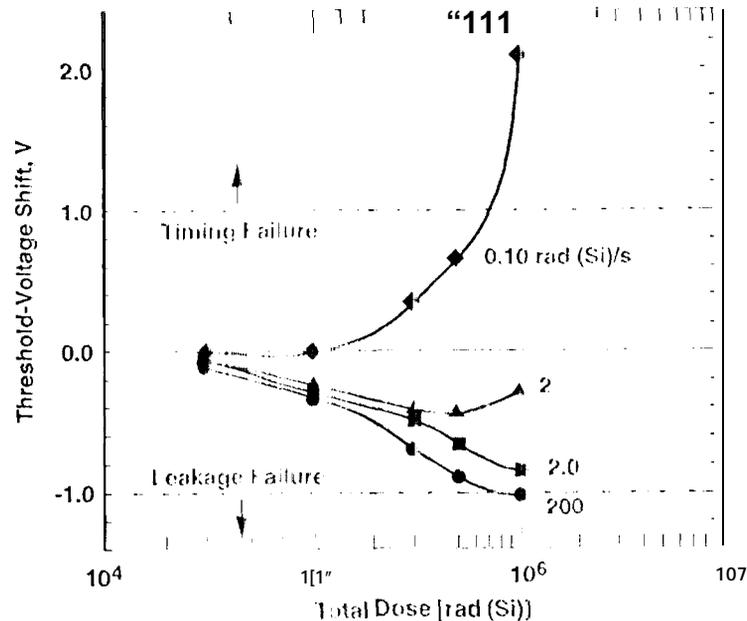
This figure shows the change in threshold voltage for n- and p-channel MOSFETs when they are exposed to ionizing radiation. At low total dose levels, the threshold voltage of n-channel MOSFETs decreases with increasing levels of radiation, and at sufficiently high levels the change in threshold voltage may be large enough to cause enhancement-mode (normally off) devices to conduct. This is caused by the buildup of trapped holes at the silicon-silicon dioxide interface. At higher radiation levels, interface traps are formed that effectively work in the opposite direction (at high currents), causing the change in threshold voltage to reverse sign in n-channel devices.

An additional complication arises because the hole traps and interface traps **have** different time dependencies. The most important difference is that hole traps **generally** anneal with time, even at room temperature. This can cause *apparent* dose rate effects in MOS devices, because most of the holes will recover at very low dose rates, leaving only the interface traps. Testing approaches have been developed to deal with this problem for MOS technologies.

For p-channel MOSFETs, hole traps cause the threshold voltage to shift in the direction that further depletes the channel (effectively the opposite direction from n-channel devices). Interface traps have the same effect in PMOS, so that even though both hole and interface traps are important, it is not possible to get the change in sign that occurs in NMOS devices.

Hardened MOS devices are available with much lower gate threshold voltage changes than the values shown in this figure. Note that device hardening must take both interface and hole traps into account.

Threshold Shift at Various Dose Rates for an NMOS Transistor



Rebound

The previous figure showed how hole and interface traps affect threshold voltage. This figure shows an example of a device where hole and interface traps compete, causing test results to depend strongly on test conditions. Although not shown here, test results depend on bias conditions (i.e. gate voltage) during and after irradiation, as well as on dose rate.

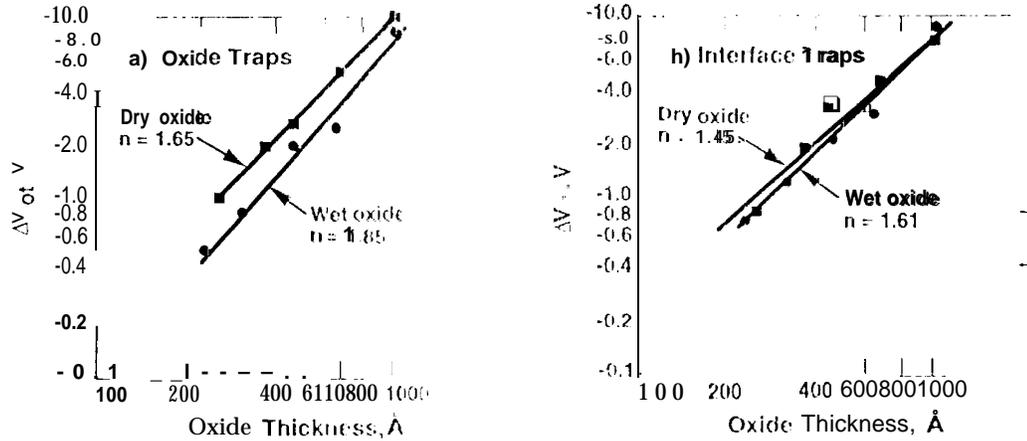
At high dose rates, hole trapping dominates, and using a criterion of ΔV_T exceeding 1 V, excessive leakage current will appear at approximately 600 krad(SiO₂). At intermediate dose rates, hole traps and interface traps compensate, and the device will operate above 2 Mrad(SiO₂). However, at lower dose rates the device will fail below 500 krad(SiO₂). Furthermore, the failure mode at low and high dose rates is completely different. The interface traps will cause switching speeds to increase. In this example this was the cause of failure at the circuit level.

This example[†] shows how the competition between the two charge components affects test structures and circuit failure. It illustrates the difficulty of interpreting tests of complete circuits without supporting data from test structures.

The time scale and total dose level over which rebound effects are important differs for different technologies. For nuclear scenarios, high dose rate response is often the most important, whereas for space applications the low dose rate response is generally the most critical.

[†]After P. S. Winokur, et al., IEEE Trans. Nucl. Sci., vol. NS-33, p. 1343 (1986)

Dependence of Threshold-Voltage Shift on Oxide Thickness



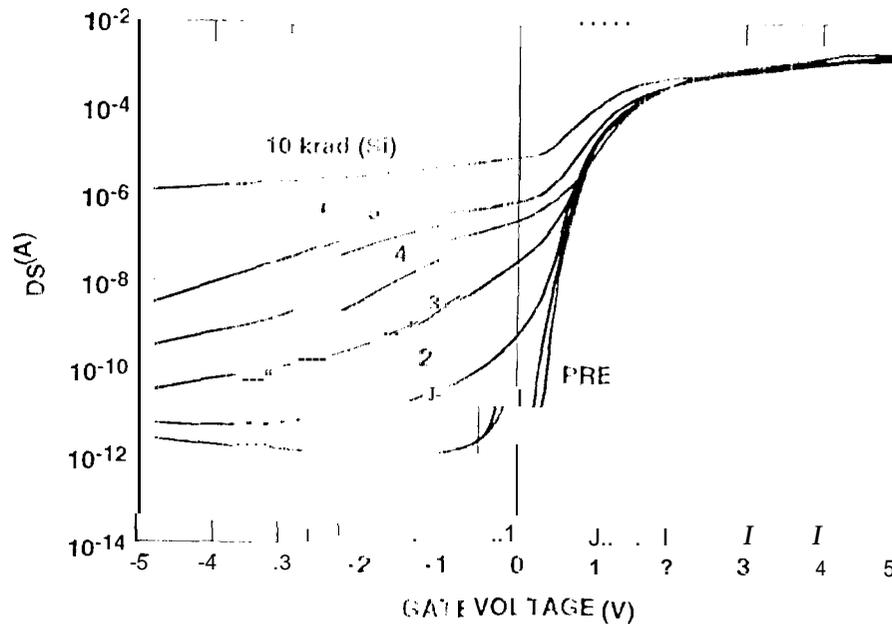
Oxide Thickness Dependence

The threshold shift in oxides is reduced as oxides are reduced in thickness, which generally occurs as devices are scaled to smaller feature sizes. This figure¹ shows the dependence of hole traps and interface traps on oxide thickness. Older devices used very thick oxides, leading to large radiation induced changes at relatively low total dose levels, but newer technologies exhibit much lower threshold shifts. However, as discussed in the next slide, thick field oxides are still required, and field oxide inversion is often the dominant problem for more advanced technologies.

Devices with high voltage ratings must use thicker gate oxides because of breakdown limitations. For this reason, power MOSFETs and CMOS A/D converters usually exhibit much higher sensitivity to total dose effects than digital devices.

¹J. M. Schwank, Short Course Notes from 1991 Nuclear and Space Radiation Effects Conference, Section II, p. 69.

I-V CHARACTERISTICS OF N-CHANNEL TRANSISTOR SHOWING FIELD OXIDE INVERSION

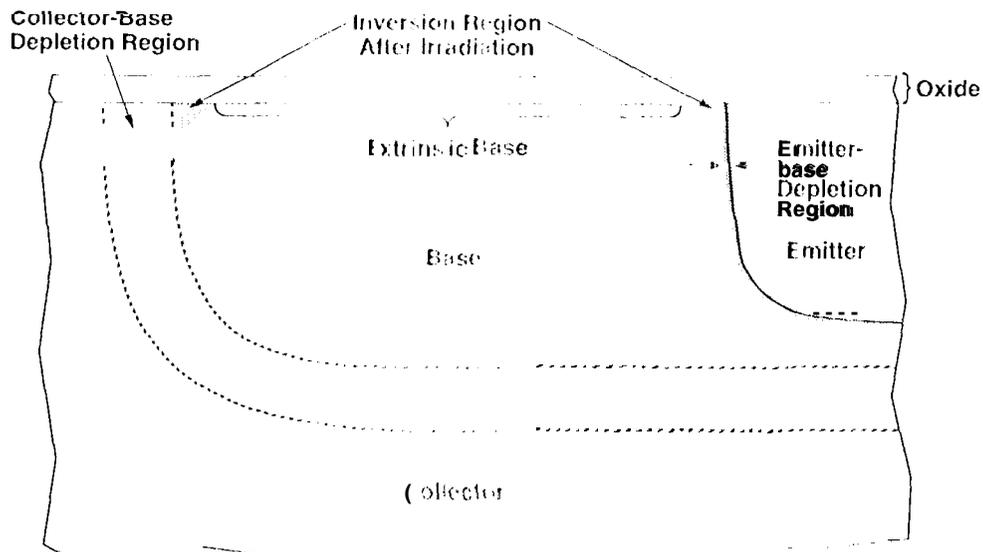


Field-Oxide Inversion

This figure shows the I-V characteristics of an NMOS transistor at various total dose levels. Only small shifts occur in the gate oxide threshold, but field-oxide inversion causes the leakage current to increase at low currents. As the radiation level increases, field-oxide leakage eventually swamps out the transistor, leading to very large current flow.

Circuits that are dominated by field oxide leakage usually exhibit a sudden increase in power supply current that is highly nonlinear with dose. The current will typically increase from a few milliamps to several hundred milliamps, and this failure mode can occur at levels well below 20 krad(SiO₂). This is the dominant failure mode for many commercial integrated circuits, and also limits the performance of some hardened technologies.

Surface Recombination and Inversion Regions in an n-p-n Transistor



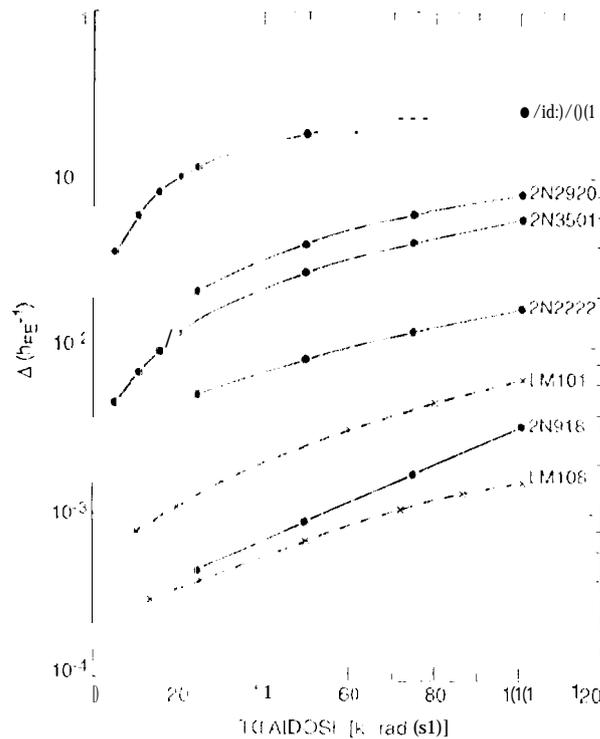
Total Dose Effects in Bipolar Devices

This figure shows a physical diagram of a bipolar transistor. The charges produced by ionization in the oxide region over the transistor can be trapped at the interface. Two effects occur: (1) the trapped charge at the surface of the emitter-base depletion region increases recombination in the emitter base depletion region, and (2), interface traps increase the recombination rate at the surface of the extrinsic base. Both mechanisms cause a decrease in transistor gain. In p material, the trapped charge can invert the surface, causing the surface of the depletion regions to spread into the base.

These processes degrade transistor gain, particularly at low operating current. Transistors that are specified over a wide range of operating currents can be particularly vulnerable to ionizing radiation damage because they are specified (and used) at very low current densities. Devices with high voltage ratings are often more affected because the lower doping levels that are required to meet the voltage rating are more easily inverted by surface charge.

The magnitude of these effects is strongly dependent on bias conditions during irradiation, particularly for discrete transistors. Large increases in leakage current can also occur when devices are irradiated with ionizing radiation. Voltage breakdown can also be affected.

A $\left(\frac{1}{h_{FE}}\right)$ vs. DOSE FOR TRANSISTORS AND OPERATIONAL AMPLIFIERS

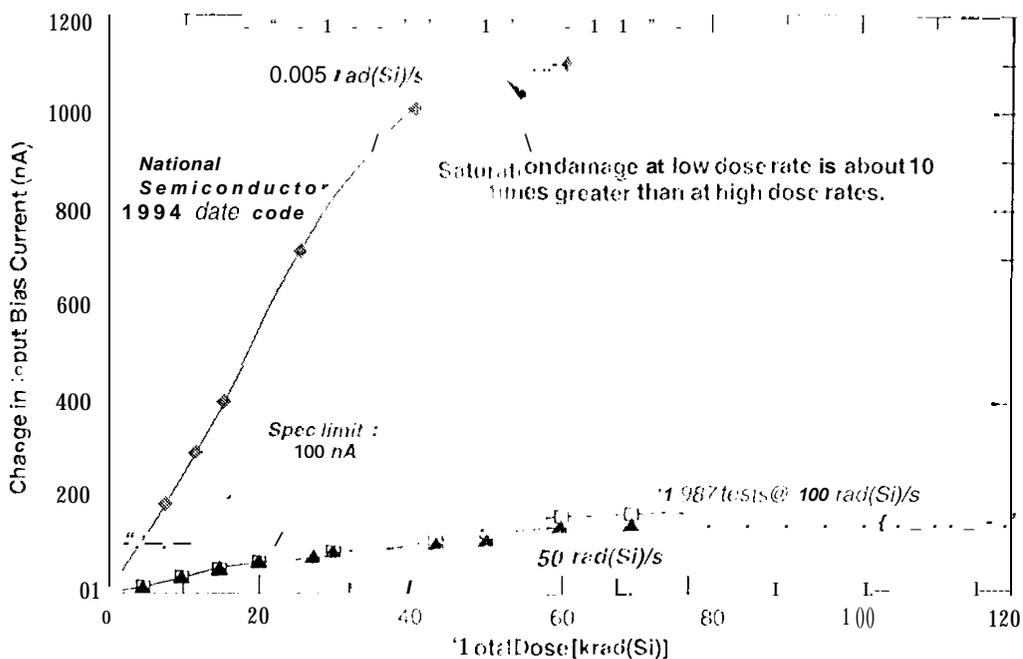


Response of Typical Transistor Types to Ionizing Radiation

This figure compares **total** dose degradation for several different types of npn transistors. The parameter that is plotted is $1/h_{FE} - 1/h_{FE}(\text{initial})$, which is linear with **total** dose at low radiation levels. Saturation generally occurs at higher levels because of the internal field produced by the depletion region as it spreads at the surface.

This figure compares different transistor types at low operating currents. Less damage occurs at higher operating currents. The large difference between transistor damage is due to several factors, including doping levels (devices with high voltage ratings have lower doping levels, and are more easily inverted), current density, and oxide properties. Much less damage generally occurs for pnp transistors because the p-type region associated with the emitter-base junction is the highly doped emitter; the high doping level requires more surface charge to cause inversion.

Degradation of Input Bias Current of LM111 Comparator at Low and High Dose Rate



Dose Rate Effects

During the last two years, several different laboratories have observed that more damage occurs at low dose rates in some types of linear integrated circuits. This figure shows the change in input bias current of a comparator with a substrate transistor input transistor; which is fabricated very differently from conventional discrete transistors. For this circuit, increases in input bias current are directly proportional to the inverse gain of the input transistor. Note the very large difference in the response of this device at high dose rate (specified by current test standards) and a much lower dose rate, which is within about an order of magnitude of the dose rates encountered in space.

Dose Rate Effects in Bipolar Devices

Significantly more damage occurs at low dose rates

- Factors of 2 to 10 have been reported
- Extremely low dose rates are required for some technologies
- Failure modes may differ at high and low dose rate

Depends on device technology and processing

- Large differences between vendors
- Special structures (such as lateral pnp transistors) are more affected

Mechanisms not fully understood

- Active research area
- Severely complicates testing and application of bipolar technologies

Dose Rate Effect Status

Enhanced damage also occurs at low dose rates in npn transistors, but most npn devices are no longer affected by dose rate for dose rates below about $1 \text{ rad}(\text{SiO}_2)/\text{s}$. The mechanism for enhanced damage in these devices is still being investigated, **but it appears** to be due to a combination of the **very thick**, poorly controlled oxides that are used in linear integrated circuits, in combination with the peculiar nature of some transistor structures in linear ICs. There also appear to be large differences in the way that parts from different manufacturers respond at low dose rates.

A number of laboratories are investigating the dose-rate problem for bipolar devices. One key issue is how to modify radiation testing approaches to deal with the problem, because it is clearly impractical to mandate time-consuming tests at low dose rate for bipolar devices. Irradiation at elevated temperature is one possible approach, but more work is needed to determine if this will work satisfactorily for all device technologies.

Recent references on dose-rate effects in bipolar devices:

R. N. Nowlin, E. N. Enlow, R. D. Schrimpf and W. E. Combs, IEEE Trans. Nucl. Sci., NS-39, p. 2020, 1992

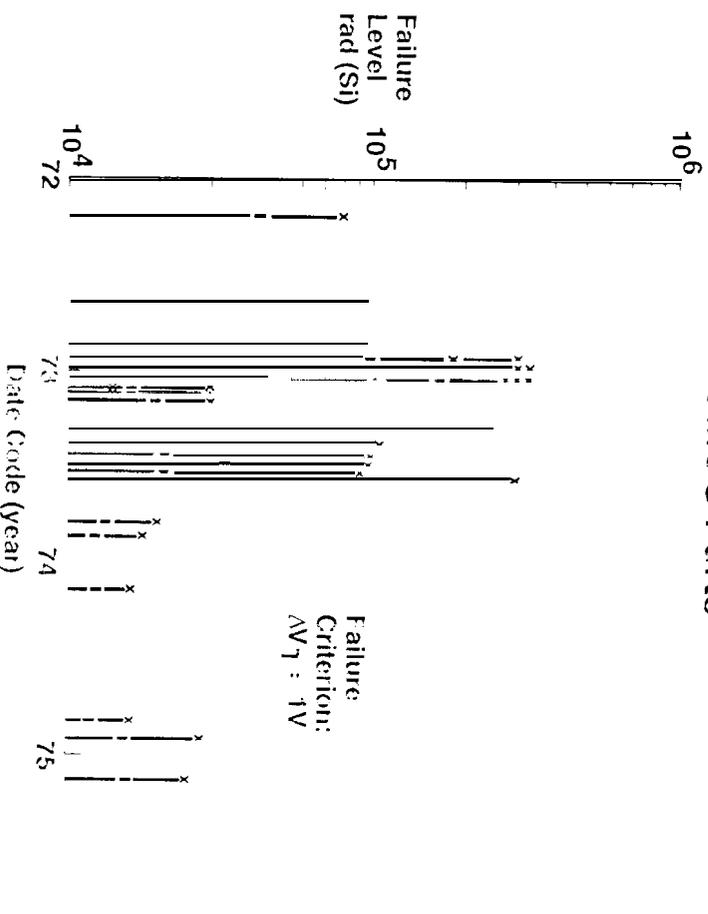
D. M. Fleetwood, et al., IEEE Trans. Nucl. Sci., NS-41, p. 1871, 1994

S. McClure, R. L. Pease, W. Willard and G. Perry, IEEE Trans. Nucl. Sci., NS-41, p. 2544, 1994

A. H. Johnston, B. G. Rax, and C. Lee, IEEE Trans. Nucl. Sci., NS-42, p. 1660, 1995

R. D. Schrimpf, et al., IEEE Trans. Nucl. Sci., NS-42, p. 1641, 1995

Hardness Versus Reliability of Type 4000 Series CMOS Parts



Processing Effects

Small changes in processing can have a large influence on the total dose hardness of MOS devices. This example, although dated, shows how the total dose failure level of CD4000-series devices varied with time. This was an unhardened commercial process that had been extensively tested. The sudden drop in hardness occurred because of small changes in the way that the gate oxide was grown during processing. These results illustrate how total dose hardness can change for commercial processes.

Radiation-hardened processes are designed to carefully control the processing steps that affect the gate and field oxide. In most cases, radiation evaluation of these processes is done on a regular basis to make sure that the radiation response remains within acceptable limits.

Total Dose Failure Levels of Various Technologies

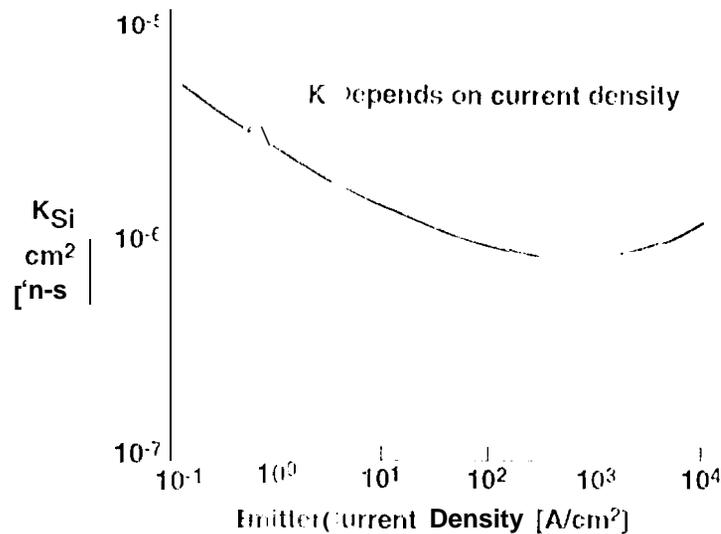
Device Category	Typical Failure Level Range [krad (Si)]	Comments
Bipolar op-amp (commercial)	5- 50	May be affected by close rate
Bipolar op-amp (hardened)	> 100	
A/D converter (commercial)	4- 20	Wick variation in designs
54AC Logic (CMOS)	(1) 30	
54F Logic (bipolar)	50- 100	
CMOS Microprocessor	8- 100	Usually dominated by field oxide

Typical Failure Levels

This figure shows representative total dose failure levels for various technologies. Considerable variation occurs for commercial processes because of the wide range of circuit designs and variations in processing. Commercial CMOS digital parts are usually dominated by field-oxide effects. The hardness level of linear devices varies widely because of technology differences.

Hardened processes are usually very well controlled. Several such processes are available that consistently produce parts with hardness levels above 1 Mrad(SiO₂). Some manufacturers provide foundry services so that their processes can be used for custom circuit fabrication. The main difficulty with hardened processes is that very few circuits are available, and that integration densities are lower than advanced commercial processes. Hardened circuits are also more costly, but much less effort and risk is involved in using these parts compared to commercial devices, which offsets much of the higher initial part cost.

Neutron Damage Constant of Semiconductors



Bipolar transistor degradation depends on base width (f_1):

$$\frac{1}{h_{FE}} - \frac{1}{h_{FE0}} = \frac{K_{Si} \phi_{neut}}{2\alpha f_1}$$

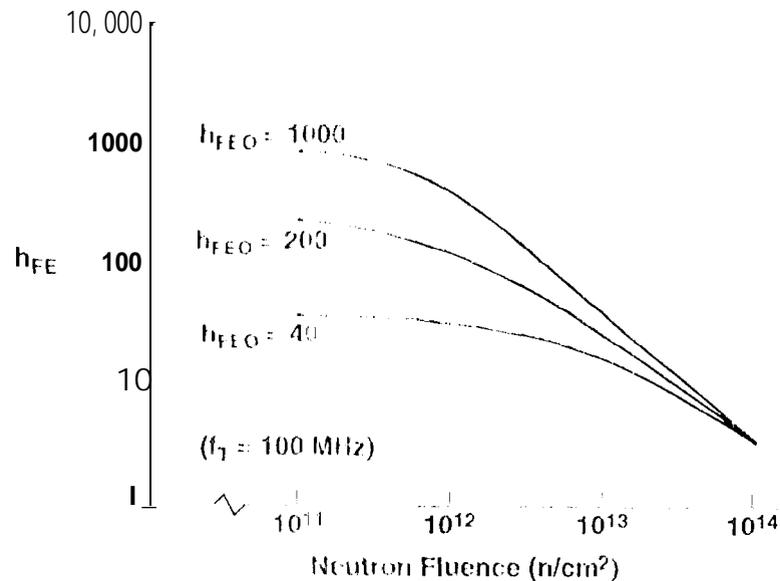
Neutron Displacement Damage

Displacement damage degrades minority carrier lifetime in semiconductors, which is a critical parameter for most bipolar devices. This figure shows the dependence of the damage constant, which affects lifetime, on injection level for p-type silicon. The damage constant increases significantly at low current densities.

The equation shows how transistor gain is related to the damage constant, neutron fluence, and unity-gain frequency response (f_1). The key point is that transistors with wide base regions (low f_1) are far more affected by neutron displacement damage than transistors with high frequency. Low f_1 transistors include transistors with very high voltage ratings, and special types of transistors used in some integrated circuits.

In addition to neutrons, protons and electrons also create displacement damage. This can be important in space applications. Again, devices with low f_1 are the main concern.

Example of "1 transistor Gain Degradation



Gain Degradation of a Typical Transistor

This figure shows how the gain degradation of a transistor with moderate f_1 degrades with neutron fluence when it is operated at high current density. The relative change in gain is much higher for devices that have high initial gain. However, a device with high gain will always have a higher post-irradiation gain (assuming the same damage constant and f_1 apply).

For this example, relatively minor degradation occurs until levels above 3×10^{12} n/cm² are reached. However, more degradation would occur at lower operating currents because of the dependence of the damage constant on current density.

Note once again that the gain degradation depends on the reciprocal of the gain-bandwidth product. A transistor with f_1 below 10 MHz will exhibit similar degradation at levels one order of magnitude below the levels shown in this example. High f_1 devices, including internal transistors in most logic circuits, will not degrade significantly until much higher irradiation levels.

Neutron Degradation of Various Technologies

Device Type	Neutron Fluence [n/cm ²]	Degradation
General-purpose bipolar transistor	10^{13}	3x gain reduction
Commercial op-amp	$0.5 - 2 \times 10^{12}$	5x increase in input current
Hardened op-amp	$> 10^{14}$	Parameter drift
54LS Logic	$> 10^{14}$	Parameter drift
Optocoupler	3×10^{11}	50% drop in current transfer ratio

Neutron Degradation of Various Technologies

This table shows some examples of the neutron levels at which significant degradation occurs. The most critical devices are linear integrated circuits with low f_T transistors. Note that although many common linear circuits fail at low levels, not all linear devices use late-era pnp and substrate pnp transistors. Thus the hardness level of linear devices can vary widely for different designs and processes.

Optical devices are often highly sensitive to displacement effects. This is caused by two factors. First, they often rely on injection gain transistors, and second, collection of optically induced carriers depends on lifetime, which is degraded by neutrons.

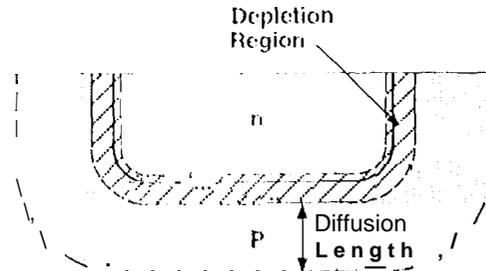
Primary Photocurrent

$$I_{pp} = q \dot{\gamma} A G (W + L)$$

Device Properties That Affect I_{pp} :

- 1) Junction Area
- 2) Depletion Width ($W - V^{-1/2}$)
- 3) Minority Carrier Lifetime ($L = \sqrt{Dt}$)
 - $L = 3 \mu\text{m}$ for $t \sim 10 \text{ ns}$
 - $L = 100 \mu\text{m}$ for $t \sim 10 \mu\text{s}$

($G = 4.2 \times 10^{13} \frac{\text{e-h pairs}}{\text{rad(Si)-cm}^2}$ in silicon)

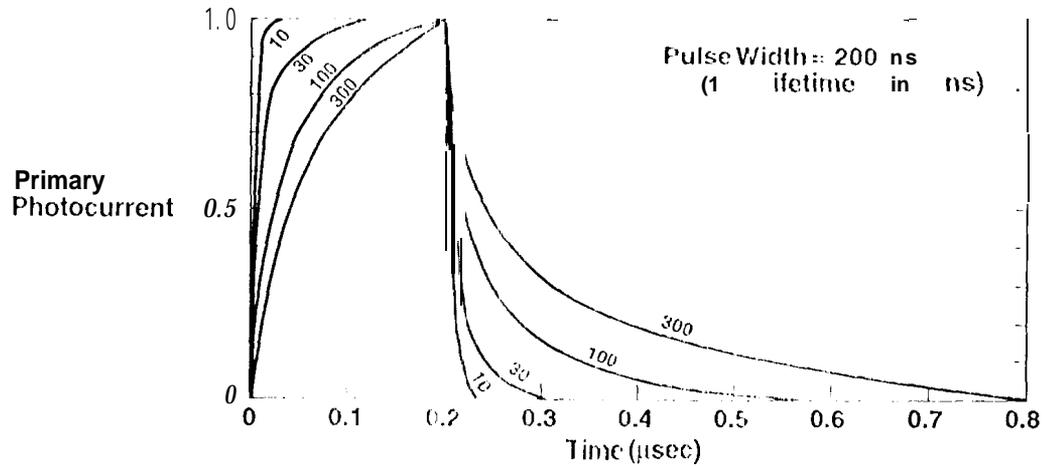


Primary Photocurrent

This figure shows the depletion region and diffused charge collection region associated with a p-n junction. Excess carriers are produced throughout the semiconductor by the ionization pulse, but only carriers within these regions are collected by the junction.

The equation shows that the current depends on the ionization pulse intensity, junction area, and the total collection depth. The diagram applies to a bulk device, where charge can be collected from the entire diffusion depth. This does not apply to structures that restrict the collection region, such as silicon-on-insulator devices or bulk devices where the presence of other diffused regions restricts the carrier collection.

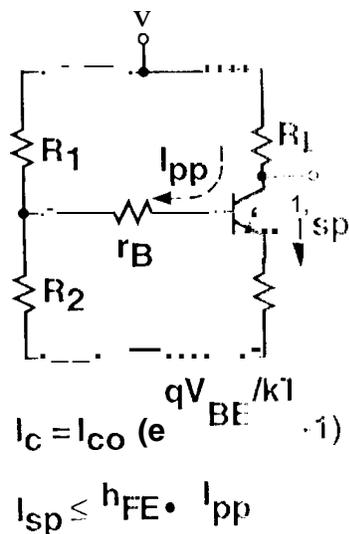
Primary Photocurrent Waveforms



Primary Photocurrent Waveforms

This figure shows the ideal time response of devices with different lifetimes to a transient radiation pulse that is 200 ns wide. For devices with short lifetimes, nearly all of the charge is collected in very short times. The diffusion component increases for devices with longer lifetimes. This not only extends the charge collection time, but also increases the magnitude of the photocurrent (see the equation in the previous figure).

Primary and Secondary Photocurrent



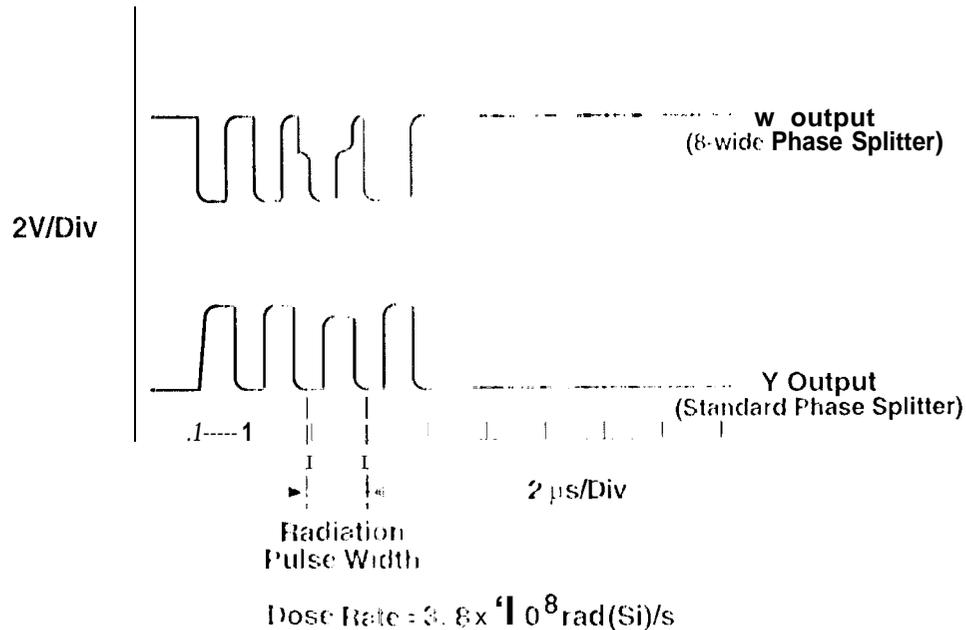
I_{pp} causes a voltage drop of $I_{pp} R_L$ before turn-on

I_{pp} flows out of base lead through r_B and external resistance

Secondary Photocurrent

Circuit effects can amplify the photocurrent collected in a p-n junction, resulting in a much higher total current. This figure shows how photocurrent in a simple transistor is amplified. At low dose rates, only primary photocurrent will occur. However, once the emitter-base junction is forward biased ($V_{BE} \approx 0.6$ V), the transistor will turn on, causing a secondary photocurrent to flow from collector to emitter. The resulting current is highly nonlinear with dose rate; a very large increase in current will usually occur once the turn-on threshold is exceeded. These effects occur in integrated circuits as well as in simple transistors. The details can be quite complex.

Output Responses of the 54151 8-Bit Multiplexer

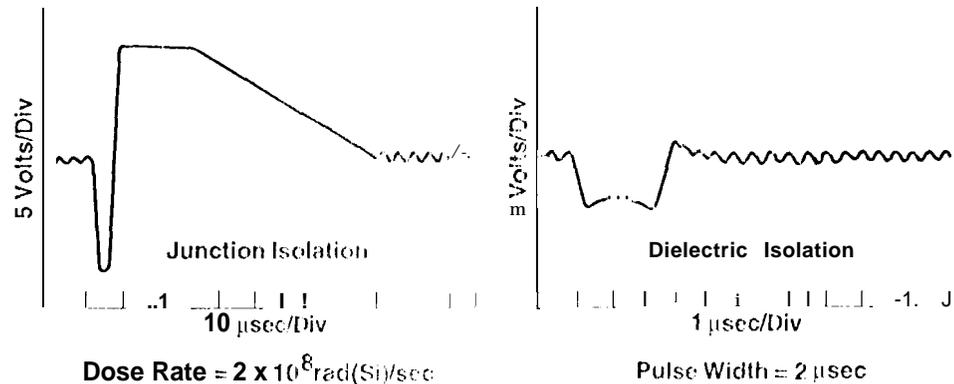


Digital Circuit Response

This figure shows the response of a digital integrated circuit to a 7 μs pulse of ionizing radiation. At this dose rate, the response of one of the outputs exceeds the noise margin, causing digital errors. Differences in internal circuitry cause the other output to have a lower response.

Dose-rate **effects** depend on the detailed circuit design and layout. The threshold upset rate of commercial digital ICs is typically between 1×10^7 and $1 \times 10^9 \text{ rad(Si)/s}$. Hardened devices are available with much higher threshold upset levels. Some hardened designs use special SOI processing to reduce the magnitude of internal photocurrents, which is an effective technique.

Transient Response of Operational Amplifiers



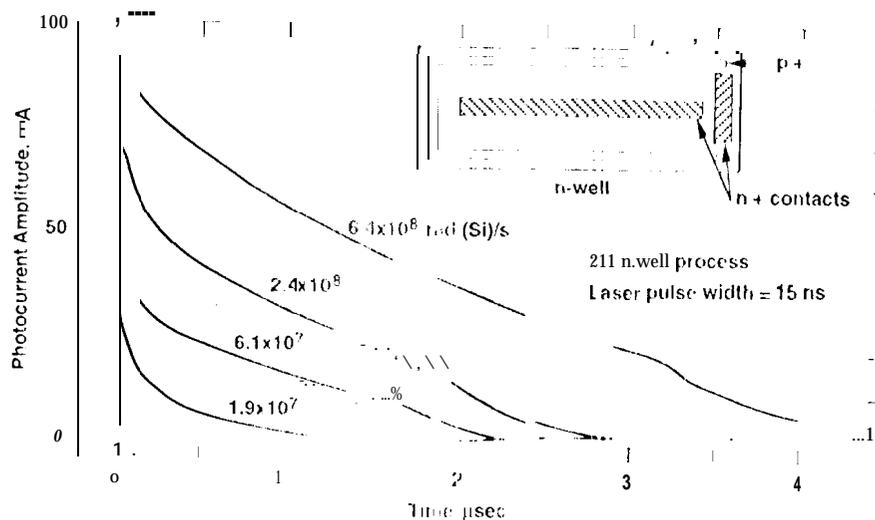
- Junction-isolated devices have long recovery times
- Feedback conditions influence recovery, not prompt response
- Radiation hardened op-amps do not operate during moderate transient ionization pulses

Linear Circuit Response

This figure compares the response of a commercial and hardened op-amp to an ionizing radiation pulse. These two circuits respond very differently. A small voltage transient occurs in the hardened device that temporarily cuts off the output signal, but the response is small, and the circuit recovers quickly after the radiation pulse subsides.

In contrast, the commercial device saturates at the negative supply voltage value. Several microseconds later, it abruptly switches to the opposite supply voltage limit, and gradually recovers at a time that is much longer than the time period of the initial radiation pulse.

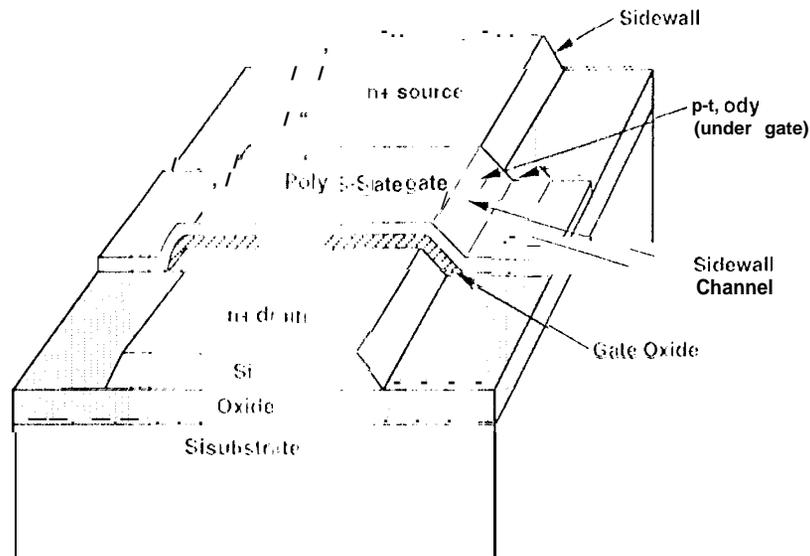
Primary Photocurrent in a Rectangular Well Test Structure



Primary Photocurrent of a CMOS n-Well

The previous examples have shown somewhat idealized photocurrent responses. Real devices can respond quite differently because of saturation of the voltage across the collection region, conductivity modulation due to the high injection level, and charge storage within the distributed structure. This figure shows the photocurrent of a CMOS n-well. Even at relatively low dose rates, the response is very different from the idealized waveforms discussed earlier. The magnitude of the photocurrent is no longer proportional to dose rate. As the dose rate increases, the time response extends to periods of several microseconds (the n well radiation pulse width was 15 ns). This shows the difficulty of understanding circuit responses to transient ionization effects.

Silicon-on-Insulator Transistor



SOI Technologies

One very effective way to harden devices to pulsed radiation effects is to use special structures that eliminate the parasitic junctions, with large photocurrents, and provide a sharp physical limit to the photocurrent collection volume. This figure shows a diagram of a silicon-on-insulator (SOI) transistor. In this example, the device is fabricated by growing islands on the top of an SiO₂ layer. Photocurrent is limited to the charge deposition volume provided by the very shallow islands.

Hardened **processes** are available that use such technologies. SOI technology typically raises the transient upset threshold by two-to-three orders of magnitude compared to junction-isolated technologies. SOI devices have much lower single-event upset error rates, and are generally immune to latchup. However, SOI processing is more costly. Some additional ionizing radiation problems are introduced because of the sidewall and the possibility of back channel leakage (the SiO₂ layer has a finite thickness), but these difficulties have been solved for hardened processes.

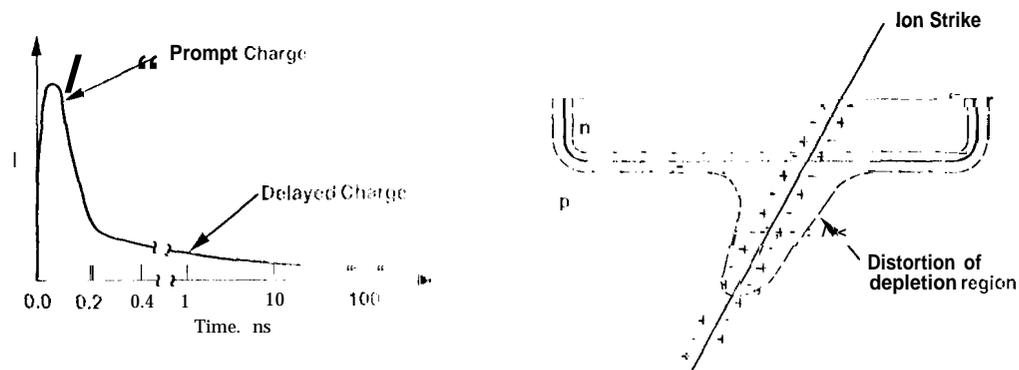
Transient Upset Threshold of Various Technologies

Device type	Typical Upset Threshold [tad (Si)/s]
54S Logic (bipolar)	$0.5 - 2 \times 10^8$
Commercial Op-amp (bipolar)	$1 - 3 \times 10^6$
Hardened Op-amp	$> 1 \times 10^8$
CMOS Memory (Commercial)	$1 - 4 \times 10^7$
CMOS Memory (hardened)	$> 10^{10}$

Typical Response Threshold of Various Technologies

This figure shows the approximate range of upset thresholds for various device technologies.

Charge Generation in p-n Junction by a Heavy Ion

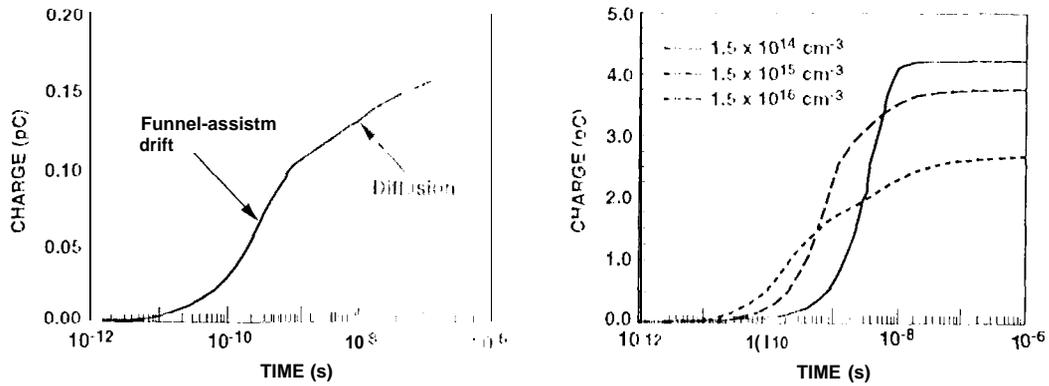


Charge Generation by Heavy Particles

This figure[†] shows the charge generated by a heavy particle in a p-n junction, along with the approximate time response. The depletion region is distorted by the very dense, localized charge track produced by the ion. This extends the prompt charge collection region well beyond the normal depletion region boundary (charge funneling). Charge collection also occurs from diffusion. The details of the charge collection process are quite complicated, depending on track density, doping level, and charge-carrier scattering processes.

[†]After J. C. Pickel, Section III of Short Course at the Nuclear and Space Radiation Effects Conference, Gatlinburg, Tennessee, July 18, 1982.

CHARGE COLLECTION IN n+/p DIODE STRUCTURES



a. 5 MeV alpha particle (0.09 pC/cm)

b. 10 MeV iron (0.27 pC/μm)

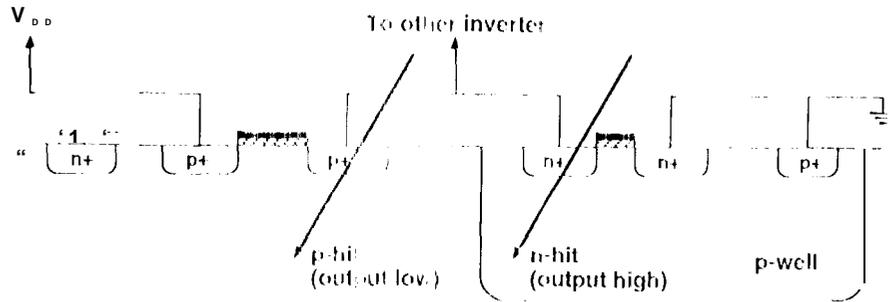
3-D simulations by P. F. Dold, et al. IEEE Trans Nucl. Sci., NS-41, 2005 (1994)

Computer Calculations of Collected Charge

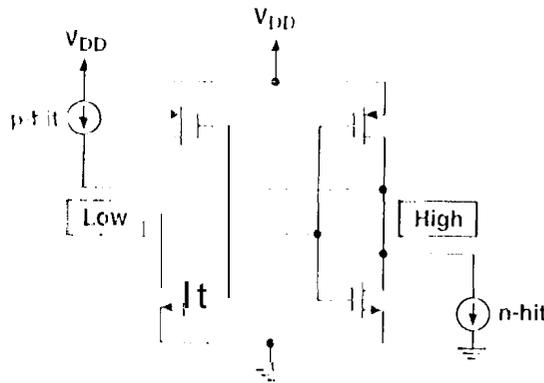
This figure shows recent results for computer calculations of charge-collection waveforms. Note that the presence of an epitaxial layer over a highly doped substrate does not reduce the total collected charge as effectively as might be expected intuitively. The time dependence is extremely important, because many single-event upset phenomena are only affected by the prompt charge that is collected in less than a few nanoseconds, whereas others, such as latchup, integrate the charge over a much longer time period.

Computer calculations of collected charge are particularly significant because of the difficulty of doing experiments with adequate time resolution. Sampling methods provide a way to overcome this limitation, but these approaches can only be implemented by using a heavy-ion microbeam or laser, both of which allow the location of the excitation to be well controlled.

Sensitive Nodes in a CMOS Inverter



- Low node is sensitive to p-hits.
- High node is sensitive to n-hits.



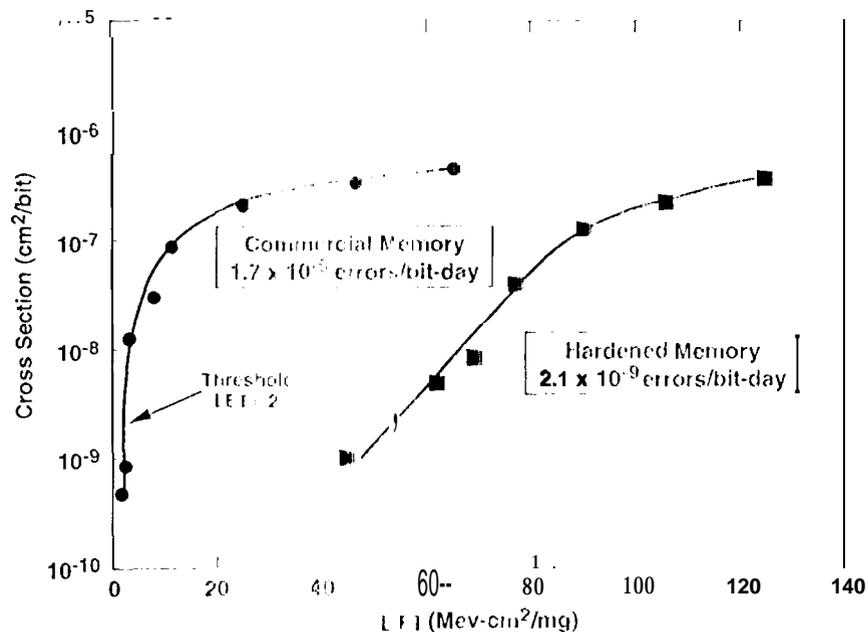
Single-Event Upset in a 6-Transistor CMOS Memory Cell

This figure³ shows how single-event upset occurs in a 6-transistor CMOS memory. A (1,1) memory cell can be upset by "hits" in either n- or p- regions, depending on the state at the output. No upset will occur until the charge collected from the ion strike exceeds the critical charge, which depends on the specific properties of the memory cell design.

This type of memory cell responds very quickly, and hence its response depends mainly on the short-time response of the collected charge waveform. Other memories, such as four-transistor SRAMs and DRAMs, respond more slowly, and are strongly influenced by diffused charge.

³After J. C. Pickel, Short Course at the Nuclear and Space Radiation Effects Conference, Gatlinburg, Tennessee, July 18, 1983.

Upset Cross Section for a Commercial and Hardened Memory



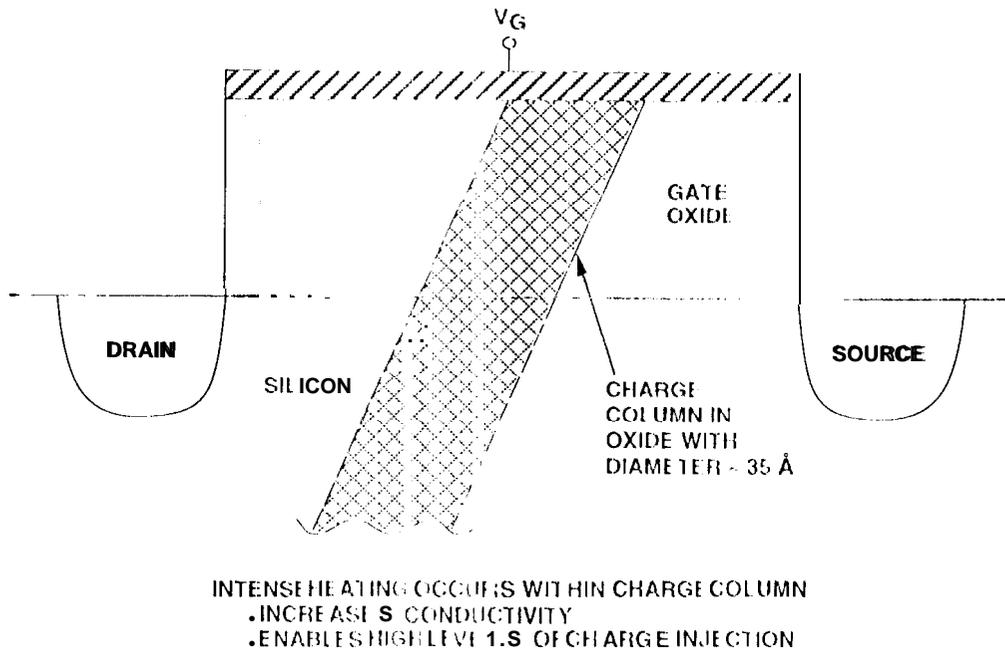
Typical Dependence of Upset Cross Section on Linear Energy Transfer

This figure shows the dependence of upset cross section on linear energy transfer for a radiation hardened and a commercial (unhardened) memory. Most experimental data uses only a few ion types, relying on changing the angle of incidence to change the effective LET. This leads to some uncertainty in cross section because of differences in charge deposition for different angles and ion types. Counting statistics also affect the cross section, particularly at low LET.

The upset rate in space depends on three factors: (1) the upset cross section, (2) the distribution of particles, which falls very rapidly with increasing LET, and (3) the charge collection volume. Often the cross section curve is fitted to a mathematical distribution (such as the Weibull distribution) in order to smooth out experimental differences and to provide a convenient way to include cross section data in upset rate calculations. However, one should remember that these distributions are strictly a mathematical convenience, and can give misleading estimates of the threshold LET in cases where limited cross section data are available near the threshold region.

The error-rate calculations shown in the figure are for a geosynchronous orbit, where galactic cosmic rays are the main concern. Even larger differences in the error rate for the two types of memories will occur in low orbits because the commercial memory can be upset by protons.

Charge Region Induced in Silicon Dioxide by a Heavy Ion



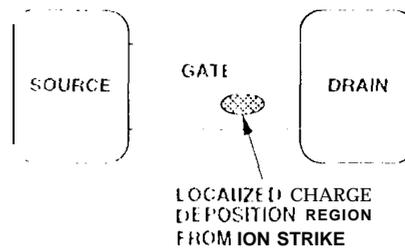
Charge Profile within a Gate Insulator

This diagram shows the approximate dimensions of the charge generated within a silicon dioxide gate insulator by a heavy ion. Some of the positive charge will be transported to the silicon-silicon dioxide interface, where it can be trapped, just as for conventional total dose effects. However, the density of charge is extremely high within a short time period after the ion passes through the insulator. This raises the temperature of the SiO_2 within the charge column. The localized temperature is high enough to raise the conductivity of this microscopic region by many orders of magnitude, which can introduce other response mechanisms, particularly for insulators which have a high electric field present during the time of the ion strike.

Microdose Hard Errors from Heavy Ions in Scaled Devices

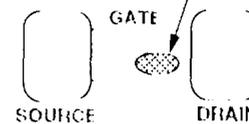
OLDER DEVICES

LOCALIZED DAMAGE REGION \ll GATE AREA
LARGE NUMBERS OF IONS MUST STRIKE
GATE TO CAUSE TOTAL DOSE DAMAGE



SCALED DEVICES

LOCALIZED DAMAGE REGION \approx GATE AREA
SINGLE ION STRIKING GATE CAN CAUSE TOTAL
DOSE FAILURE



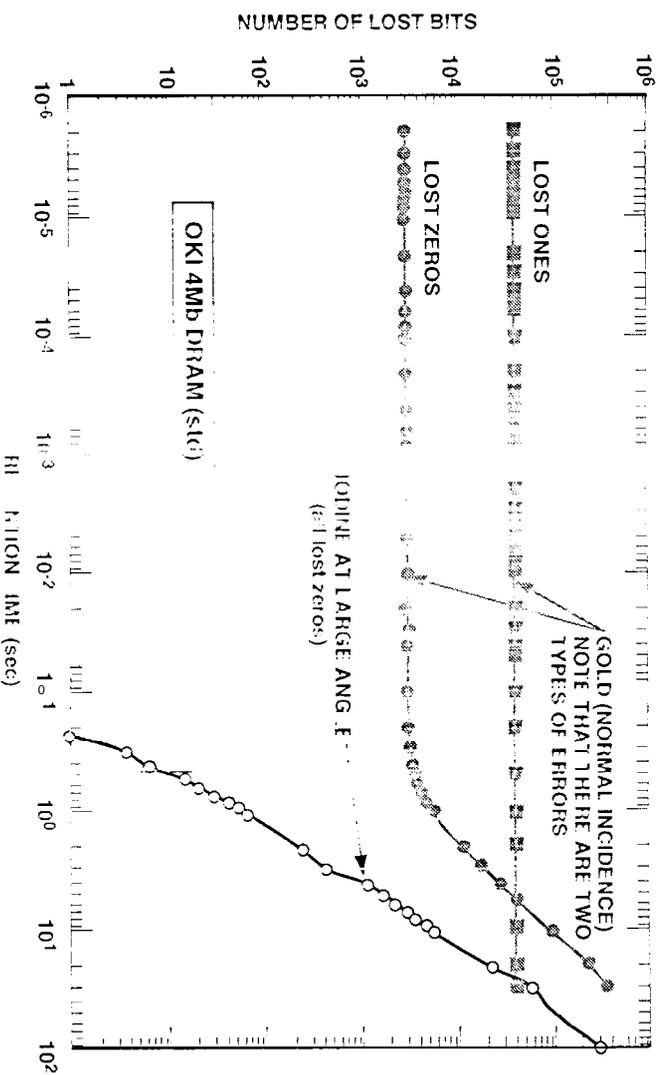
Microdose Errors from Single Particles

This diagram[†] shows how microdose hard errors can occur when the gate area of a device is reduced to the point where the localized charge collection area becomes a significant fraction of the total gate area. Microdose errors have been observed for devices with feature size below one micron, and are expected to become more important as devices are scaled further.

With these feature sizes, the localized dose is not sufficient to shift the gate threshold voltage very much, and the main concern is in circuit designs that are affected by small increases in subthreshold leakage, such as DRAMs and 4-transistor SRAMs. It may eventually become important for conventional logic as devices are scaled to smaller dimensions.

[†]Adapted from "P. Oldham, et al., IEEE Trans. Nucl. Sci., vol. NS-40, p. 1820 (1993).

RETENTION-TIME DISTRIBUTION AFTER IRRADIATION WITH HEAVY IONS



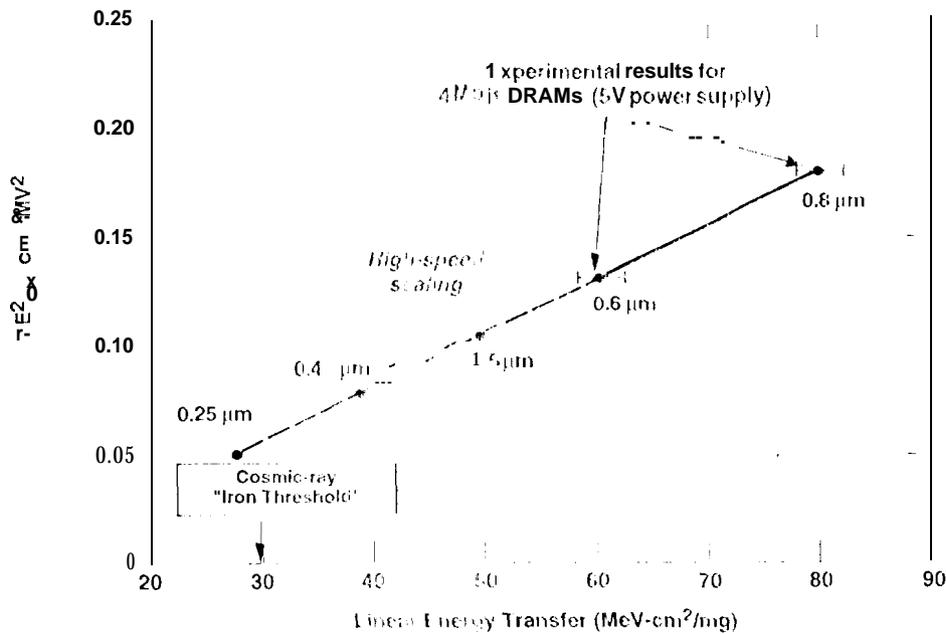
Catastrophic Hard Errors in High-Density Devices

This figure⁴ shows experimental results for a DRAM that exhibits microdose errors along with a second type of hard error that appears to be caused by gate failure. For ions with LET below 80 MeV-cm²/mg (such as the iodine ion shown in the figure), only microdose errors occur. The effect of the microdose errors is to increase the leakage current, increasing the minimum retention time. The distribution of retention times occurs because the amount of damage depends on the particular location of the ion when it traverses the gate. Note that only "lost zeros" occur with this mechanism because the effect is to increase leakage current in the pass transistor between the DRAM storage cell and the sense line.

When the device was tested with gold ions, a second mechanism appears (in addition to microdose errors) that causes the retention time to fall to very low values. The internal element struck by the ion can no longer be controlled by the gate voltage, and both types of errors occur (stuck ones and zeros). The second type of hard error is potentially far more serious because it may occur with random logic devices as well as in storage arrays.

⁴After G. W. Swift, J. Padgett, and A. Johnston, IEEE Trans. Nucl. Sci., vol. NS-41, p. 2013 (1994).

PREDICTED TREND IN HARD ERROR THRESHOLD FOR SCALED DRAMs WITH VARIOUS FEATURE SIZES



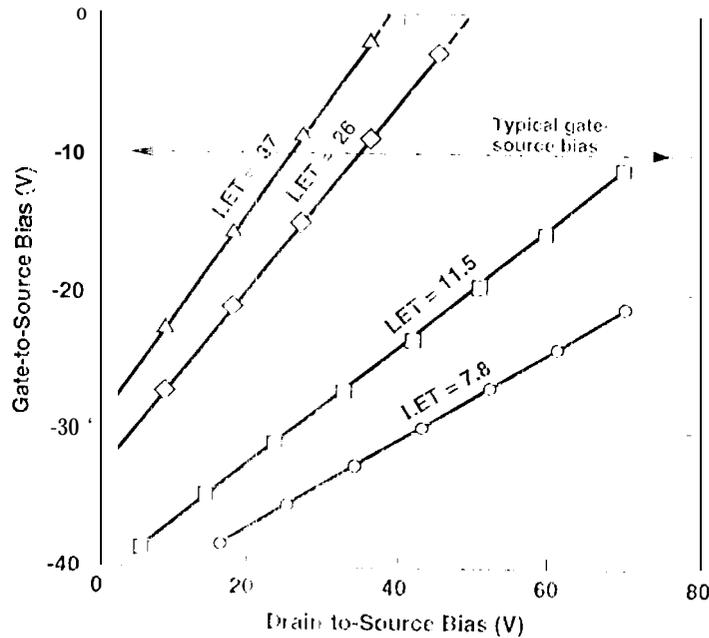
Predicted Effects of Scaling on Catastrophic Hard Errors

Although catastrophic hard errors can be found experimentally, the error rate in practical space environments is so low that the problem is not very significant for present technologies. However, the limited data available on scaling shows that the threshold LET decreases with decreasing feature size.

This figure¹ shows a prediction of the effect of scaling on threshold LET as feature sizes are reduced. The increased sensitivity occurs because basic scaling relationships require the gate oxide field to be increased in order to take maximum advantage of scaling. Once the threshold LET decreases below 40 MeV-cm²/mg, hard error rates will increase to the point where several hard errors will occur per year in a high-density device. This will rise to much higher levels if the threshold drops below 30 MeV-cm²/mg because of the increase in abundance of galactic cosmic rays below the iron threshold. More work needs to be done on the effect of scaling and device design on hard errors, but this may eventually be a major stumbling point for the application of high-density devices in space.

¹After A. H. Johnston, G. W. Swift, and D. C. Shaw, Digest of Papers from the IEEE Symposium on Low Power Electronics, p. 88, October, 1995.

Gate Rupture in a Power MOSFET



Gate Rupture in Power MOSFETs

Heavy ions can cause gate rupture in power MOSFETs. A strong vertical electric field is present in these devices, and this causes the LET at which gate rupture will occur to depend on the drain-source bias as well as on gate bias.

This figure[†] shows how both parameters affect the gate rupture threshold. For typical gate biasing, the effect LET threshold is approximately 20 MeV-cm²/mg, but it drops to much lower values when a higher gate-to-source voltage is used.

Tests of gate rupture are difficult and costly because the device is destroyed once gate rupture occurs. A large number of devices are required in order to characterize devices in sufficient detail.

[†]Adapted from M. Allenspach et al., IEEE Trans. Nucl. Sci., vol. NS-41, p. 2160 (1994)

Summary of Hard Error Effects

MICRODOSE MECHANISM

- INCREASE. STRANSIS10II LEAKAGE CURRENT
- CAUSED BY LOCALIZED CHARGE TRAPPING

GATE FAILURE MECHANISM

OBSERVED IN DRAMS WITH 0.6 AND 0.8 μm FEATURE SIZE

SIMILAR MECHANISM IN POWER MOSFETS

- AFFECTED BY CURRENTS IN UNDERLYING SUBSTRATE
- ERROR RATE CAN BE LOWERED BY REDUCING BIAS CONDITIONS

ALSO OBSERVED IN PROGRAMMABLE GATE ARRAYS

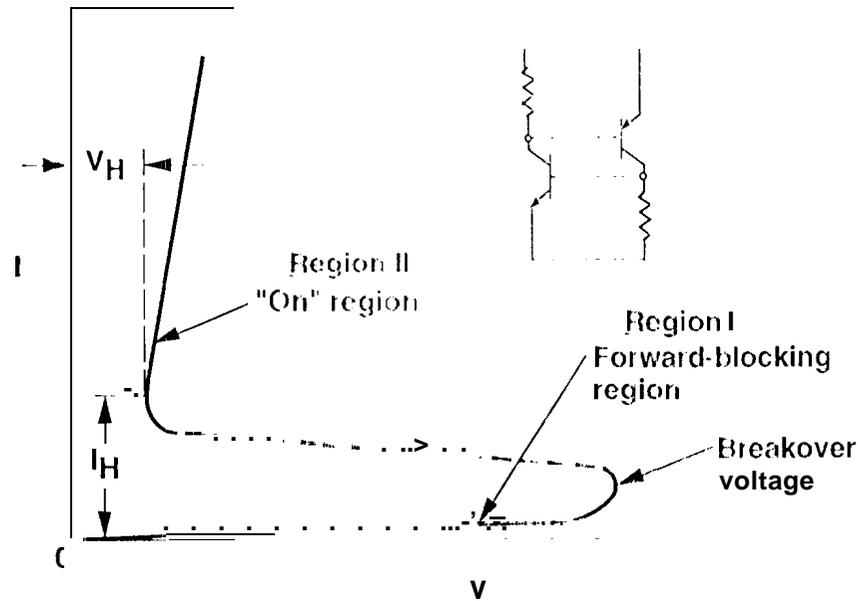
- HEAVY IONS CAN PROGRAM ANTI-FUSE S, (HANGING GATE ARRAY CONFIGURATION)
- OBSERVED IN TECHNOLOGIES WITH 1 μm FEATURE SIZE
- EXPECTED TO BE A MAJOR ISSUE FOR SECOND-GENERATION DEVICES

Summary of Hard-Error Effects

This figure summarizes the main issues for hard errors. Gate rupture has also been observed in programmable gate arrays in addition to memory devices. For gate arrays, the effect is to permanently alter the gate array by shorting the antifuse structure that is used to program the array.

Ions with very high LET values are required to introduce hard errors in CIII'milt technology devices. However, manufacturers are planning to introduce new designs with lower operating voltages and low power dissipation. Programmable gate arrays are planned for the near future which will require lower programming voltages and will also use reduced insulator thicknesses. It is likely that hard errors will increase in importance in the future, particularly for highly scaled devices.

I-V Characteristics During Latchup

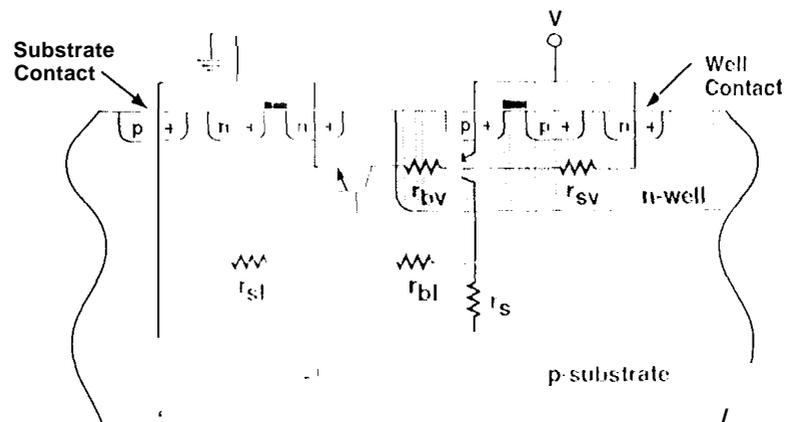


Latchup Characteristics

This figure shows the current-voltage characteristics of a four-region structure (a p-n-p-n region), similar to a silicon-controlled rectifier. The device can be switched into a low-impedance condition, where it functions as a very efficient switch.

Key parameters are the holding voltage and holding current. The structure will only remain on if the circuit conditions are sufficient to keep the holding voltage and holding current above their minimum values.

Latchup Path in a CMOS Circuit



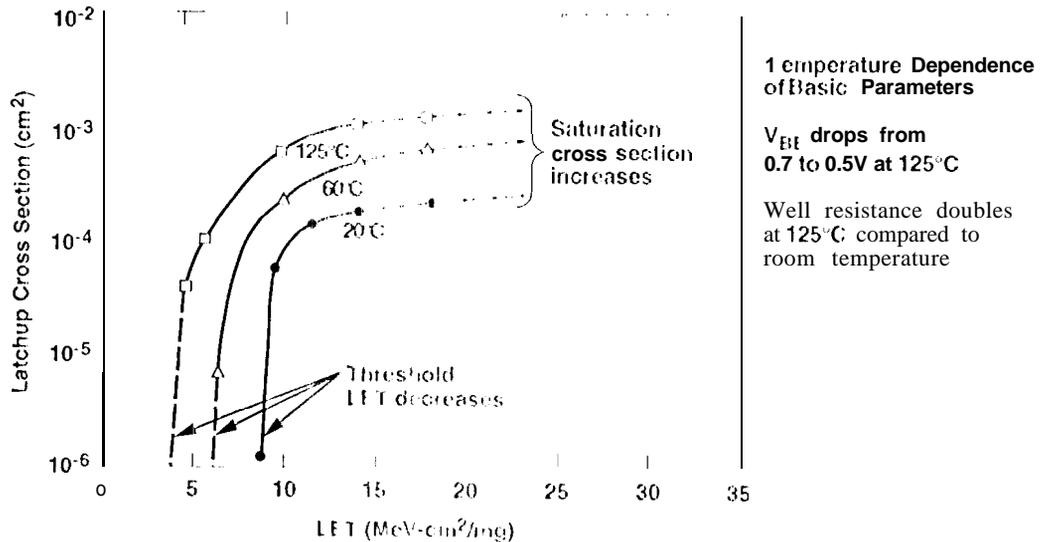
Parasitic Transistors in CMOS

This diagram shows the way that npn and pnp parasitic transistors in a CMOS circuit form a parasitic four-region structure. A vertical pnp transistor is formed by the anode (PMOS source or drain diffusion), the n-well used to isolate PMOS transistors, and the p-substrate. A lateral npn transistor is formed by the cathode (NMOS source or drain diffusion, substrate, and n-well).

The parasitic structure in most CMOS devices can be triggered by either a transient ionization pulse or by heavy ions under the right conditions. Once the device is triggered, it will draw very large currents, and will remain in that condition until the device is destroyed by overheating of the metallization or contacts, or until the power is removed. Note that junction-isolated bipolar devices can also exhibit latchup.

Latchup is an extremely important problem for military and space systems, but it is very difficult to deal with because it depends on the detailed topology of the circuit as well as on specific operating conditions and temperature. Some systems use 100% screening, testing each individual device with a high-level transient ionization pulse in order to make sure that none of the parts used in the system will be affected by latchup.

Effect of Temperature on Latchup Characteristics of a Bulk CMOS Memory



Effect of Temperature on Latchup

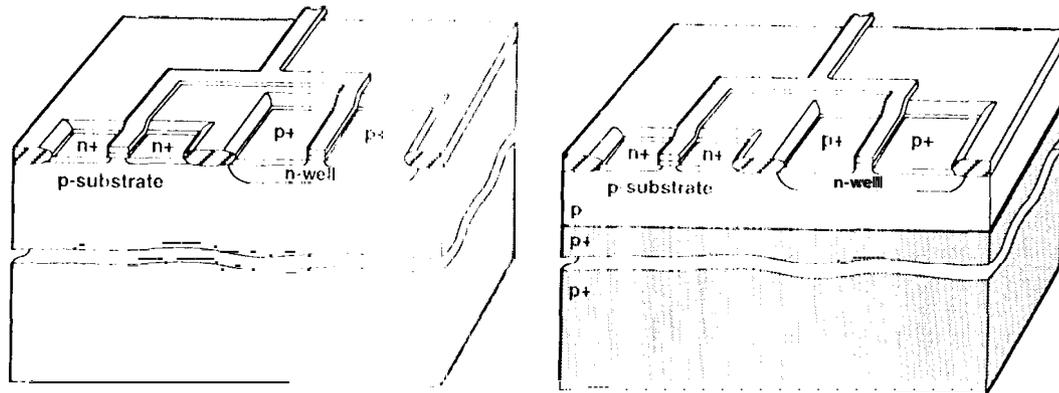
Elevated temperature lowers the minimum conditions for triggering and sustaining latchup. The main factor is the well resistance in CMOS, which approximately doubles at 125 °C compared to room temperature. This figure¹ shows a decrease in threshold LET of more than a factor of two, along with nearly an order of magnitude increase in saturation cross section at high temperature. This result is typical of most circuits, and depends on the fundamental properties of the parasitic bipolar transistors.

Because of this strong temperature dependence, it is important to do single-event latchup testing at the highest specified temperature. Calculations of expected latchup rates must take temperature into account. A factor of two decrease in threshold LET can have a very large effect on the upset rate in space.

Latchup from transient ionization is also affected by temperature. This may be important in determining the effectiveness of latchup screening techniques. Leakage currents can also be a factor in latchup sensitivity, and may cause a stronger temperature dependence than shown in the figure for some technologies.

¹After A. J. Johnston, B. W. Humphreys at IRE Plaug, IEEE Trans. Nucl Sci., vol. NS-38, p. 1435 (1991).

Bulk anti Epitaxial CMOS Structures

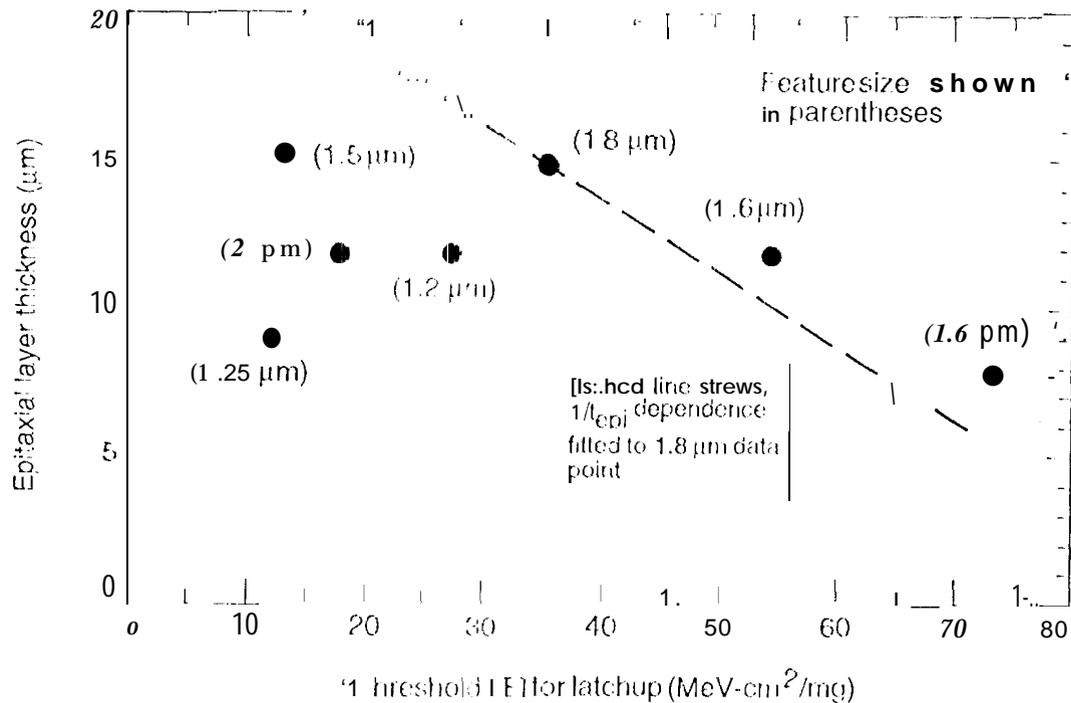


Bulk and Epitaxial CMOS Technology

This diagram compares bulk and epitaxial CMOS technologies. At first glance there is not much difference, but the line in the right diagram shows the demarcation between a lightly doped epitaxial layer and a highly doped substrate. The substrate has a much lower resistivity than the substrate in the bulk device, which is entirely composed of lightly doped material. The low substrate resistance raises the minimum current (or charge) required to trigger latchup, and also increases the holding voltage.

Epitaxial CMOS is used in many commercial circuits. However, epitaxial wafers cost considerably more than bulk wafers, limiting their use. Epitaxial substrates always improve latchup characteristics, but results vary widely for different processes, as discussed in the next figure.

Weak Correlation of Latchup Threshold and Epitaxial Thickness for Different Device Technologies



Dependence of Latchup on Epitaxial Thickness

This figure[†] shows experimental results for a number of different CMOS part types fabricated on epitaxial wafers. If only the epitaxial thickness is varied, the minimum triggering current (I_{ET} in this case) should scale as the reciprocal of the epitaxial layer thickness, as shown by the dashed line which is arbitrarily fitted to the 1.8 μm feature size point.

There is rough agreement with this relationship for some devices, but others deviate widely. Several of the parts have threshold I_{ET} values for latchup that are extremely low, comparable to the threshold I_{ET} of bulk technologies. The important point is that although epitaxial substrates generally raise latchup triggering levels, simply selecting devices that are fabricated on epitaxial substrates is not sufficient. Other factors in device design and layout have a strong influence on latchup characteristics.

[†]Adapted from T. Chapuis, H. Constantinescu and J. Rozier, IEEE Trans. Nucl. Sci., vol. NS 37, p.1839 (1990).

Latchup Detection and Power Shutdown

Simple Concept: Detect Increased Current and Shut Down Power

Complications;

Different Latchup Paths Can Produce Different Current Signatures

Some Circuits May Exhibit Only Small Current Increases after Latchup

Temperature Can Affect Latchup Characteristics

Metallization Failure May Occur in Very Short Time Periods

Power Supply Shutdown Is Not Straightforward

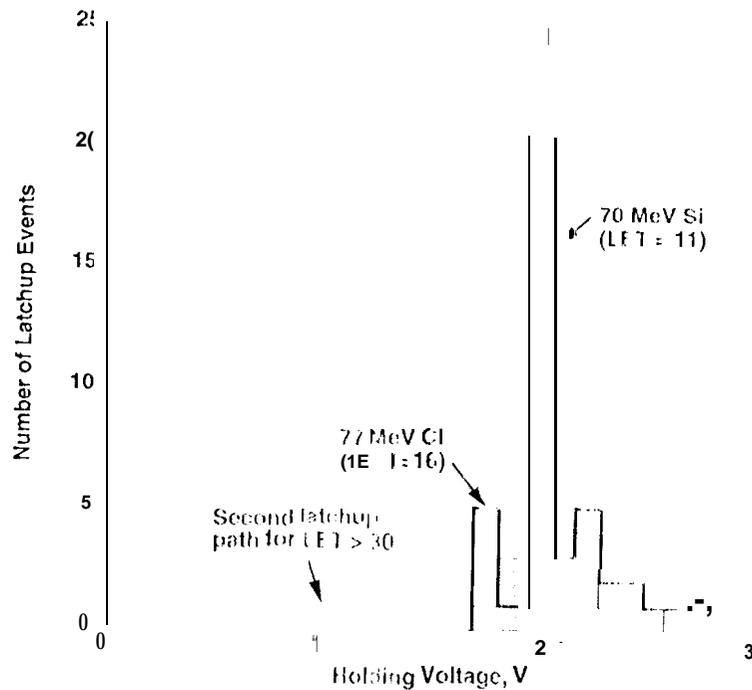
Latchup Detection and Quenching

Latchup detection and power shutdown is sometimes used to overcome the latchup problem at the system level. The basic concept is simple, but there are a number of complications that may limit its effectiveness.

- (1) Complex circuits usually have many different latchup paths, with different current signatures. This may make it impossible to set a current limit trip point that will be effective for all latchup conditions. This is a more severe limitation for single-event latchup than for latchup induced by transient ionization.
- (2) In some cases only small current increases occur after latchup, making it very difficult to sense the latchup condition.
- (3) Temperature can alter latchup characteristics, as noted earlier.
- (4) Metallization failure can occur in very short time periods. This can cause catastrophic failure before the circuit voltage can be lowered to the point where latchup no longer occurs.
- (5) Power supply shutdown is complicated because usually a number of different circuits **are affected**. The large capacitors that are present in most power supply lines makes it difficult to lower the voltage in very short time periods.

Clearly a number of factors determine how effective this approach will be. Its success also depends on the likelihood that latchup will actually take place during the time **that a** system is deployed. For example, if only one or two latchup events are expected during the mission duration, the risk of the latchup circumvention scheme not working may be low enough to be acceptable.

Histogram of Holding Voltages for SEU-Induced Latchup in 7187 SRAM



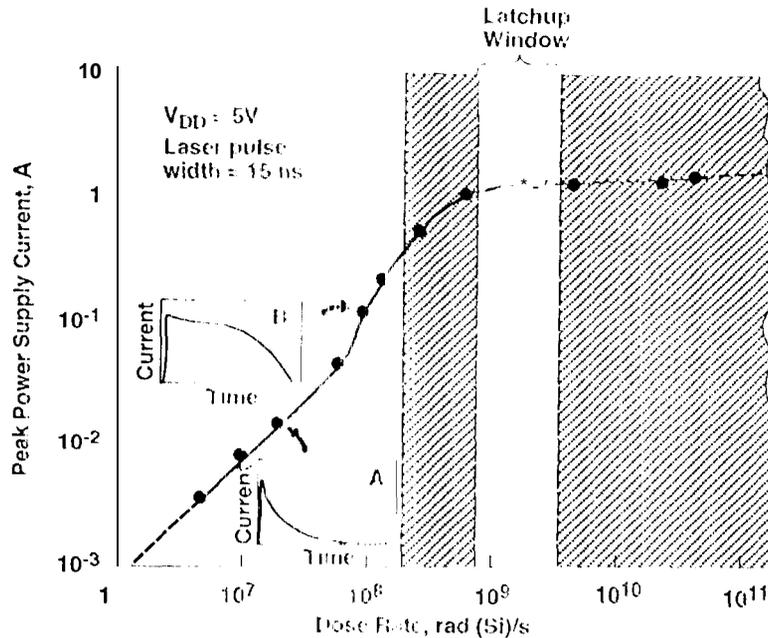
Equilibrium Conditions During Latchup

This figure shows the holding voltage at the *circuit* level for a number of different latchup events, triggered by heavy ions. The voltage was established by limiting the current to 200 mA, which was necessary to keep the device from being destroyed. Devices with high equilibrium voltages effectively have higher holding currents if they are connected to a power supply with higher current limiting.

For ions with LET = 11 MeV-cm²/mg, most of the events have a terminal circuit voltage of 2 V, with a small number as low as 1.7 V. When the test is done with a slightly higher LET, the distribution broadens, and there are more events with high holding voltage. The key point is that the equilibrium current during latchup varies by about a factor of two for this one individual device. A second latchup path with much lower holding voltage can occur for ions with even higher LET. This latchup path could not be detected if the current trip point was set based on the primary latchup path.

This illustrates the difficulty of characterizing latchup for a device of even moderate complexity. Temperature and unit-to-unit variations further complicate this issue.

Power Supply Current vs. Dose Rate for a 64k CMOS SRAM



Latchup Windows

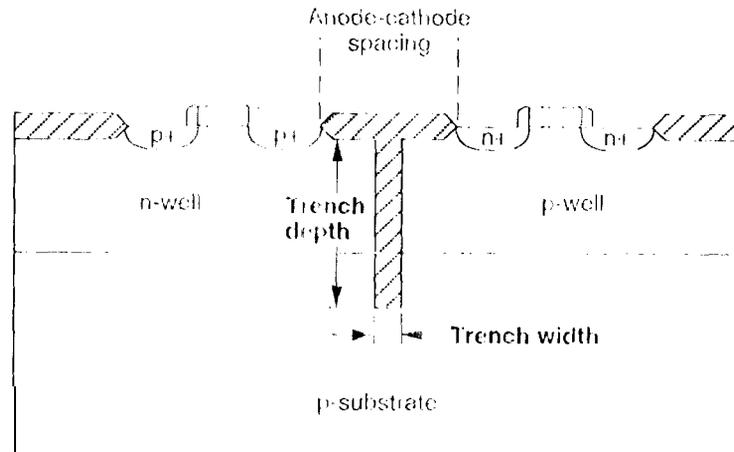
This figure shows experimental results for a circuit with a so-called latchup window, which is shown by plotting the response of the device to successively higher dose rates (global irradiation). As the dose rate increases, the device exhibits latchup. At rates somewhat above the latchup threshold latchup no longer occurs. This is due to the large internal voltage drops that result from primary photocurrent in the large isolation wells. (Recall the earlier figure that showed how internal saturation extended the photocurrent of an isolation well to times on the order of microseconds). If these currents are large enough, the internal voltage drops are sufficient to keep the internal voltage below the holding voltage, and the device no longer exhibits latchup.

At much higher dose rates, a second latchup path can be triggered, and the device once again exhibits latchup. Latchup windows depend on the detailed layout of the circuit, including the distance between the power supply and ground connections and the dominant latchup paths. Latchup windows are very important in practice, primarily because they can cause misleading test results for devices that are subjected to 100% screening to determine latchup susceptibility. Such testing is usually done at a single dose rate [often a short pulse of a few hundred rad(Si) is used]. If the latchup window overlaps the screening level, erroneous results are likely to occur.

Latchup windows cannot occur from single particles because only a single, localized latchup path is involved.

¹After A. H. Johnston, R. E. Plaag, and M. P. Baze, IEEE Trans. Nucl. Sci., vol. NS-36, p. 2229 (1989).

Cross Sectional View of Trench Isolation

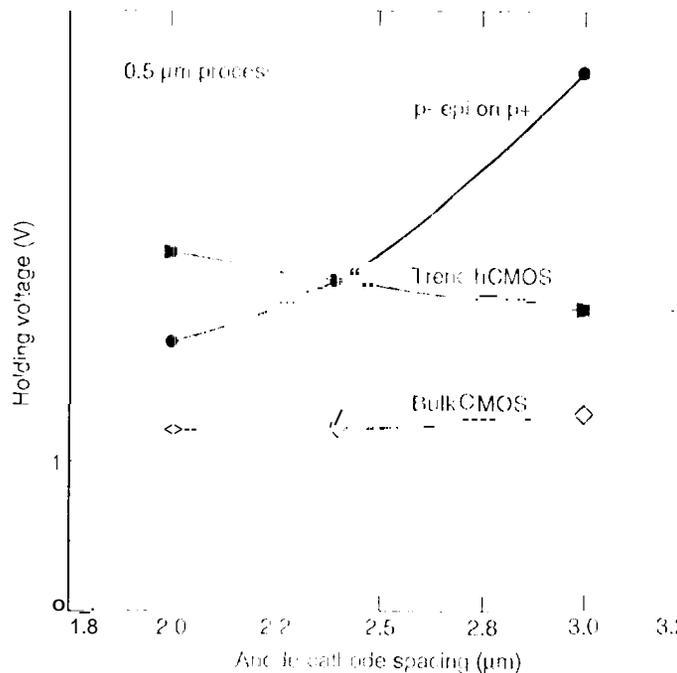


Trench Isolation : An Example of an Advanced Technology

This diagram shows how vertical trenches can be used for lateral isolation in MOS devices. Trench isolation improves packing density compared to conventional isolation, but still relies on junction isolation in the vertical direction, and hence latchup can still occur for devices with trench isolation. However, the presence of the trench reduces the gain of the lateral bipolar transistor that is involved in latchup. The key factor in reducing latchup is trench depth, rather than lateral spacing. Devices can be fabricated with deep trenches that raise the holding voltage well above the normal power supply voltage, eliminating the possibility of latchup.

Trench isolation is used in some commercial technologies because of the improved packing density that it provides. One additional problem which can occur is inversion of the region surrounding the trench, caused by positive charge buildup from ionizing radiation.

Dependence of Holding Voltage on Anode-Cathode Spacing for Different Technologies



Effects of Isolation Methods on Latchup

This figure[†] shows how the holding voltage depends on anode-cathode spacing (a fundamental layout parameter for latchup) for devices with different technologies. It is a useful way to look at latchup, because if the holding voltage can be raised **above the power** supply voltage, latchup cannot occur. The results are for a highly scaled process with **very** shallow diffusions.

For conventional bulk CMOS the triggering current increases **only** slightly with increased spacing, and there is only a small effect on holding voltage. For epitaxial devices, holding voltage increases **much** more strongly with increased anode-cathode spacing. A **very** different result occurs with trench isolation. In this case the holding voltage **actually decreases** with increased anode-cathode spacing. This nonintuitive result occurs because the trench depth is the important parameter for this technology.

This figure illustrates the difficulty of determining topological conditions that will reduce latchup susceptibility. This is particularly difficult for advanced processes, partly because the anode-cathode spacing has to be reduced to the point where substantial lateral transistor gain is present in order to achieve the required transistor density. Older technologies used much wider anode-cathode spacing, which was more effective in altering latchup conditions.

[†]After P. V. Gilbert, P. E. Crabtree, and S. W. Sun, Digest of Papers from the IEDM, p. 731, December, 1993.

Commercial Semiconductor Technologies

Wide Ranges in Radiation Response May Occur

- Lot Variations
- Unit-to-Unit Variations
- Technology Changes Between Initial Evaluation and Procurement

Uncertainties in Evaluating Device Responses

- Complex Circuit Responses
- Testing Complications

Commercial Technologies Increase Performance and Reduce Part Cost

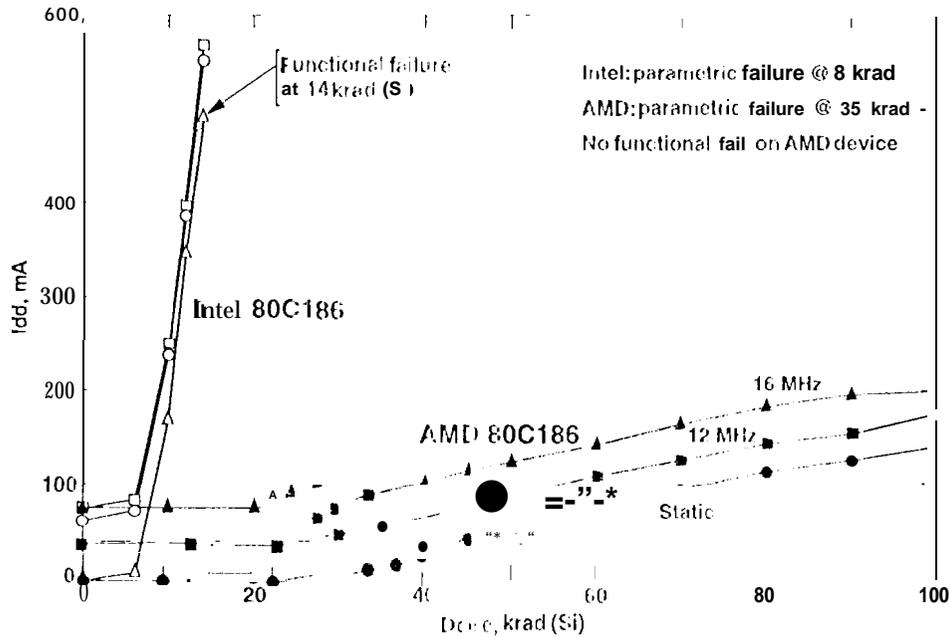
- Higher Risk Because Processing and Device Designs Are Unknown
- Higher Cost for Radiation Testing and Hardness Assurance
- Higher Risk of Problems that Affect Cost and Schedule

Special Problems for Commercial Device Technologies

The next section of the short course will address commercial device technologies in considerable detail. There are a number of problems in using commercial devices in highly reliable applications, particularly if the circuits are fabricated on high-volume commercial processing lines where the complexity of the operation and proprietary considerations make it impossible to establish sufficient control or knowledge of the fabrication process.

Much of the material in this section has addressed radiation responses of unhardened technologies, but in the context of military or space qualified parts, where the manufacturer has a vested interest in producing parts that meet those specific requirements. A different set of problems arises when commercial parts are used because the manufacturer no longer "buys in" to high-reliability applications. The net effect will probably be increased costs for radiation testing and hardness assurance, along with higher schedule risk. The effectiveness of archival data banks in selecting candidate parts for new systems may also change.

Total Dose Degradation of Commercial Microprocessors

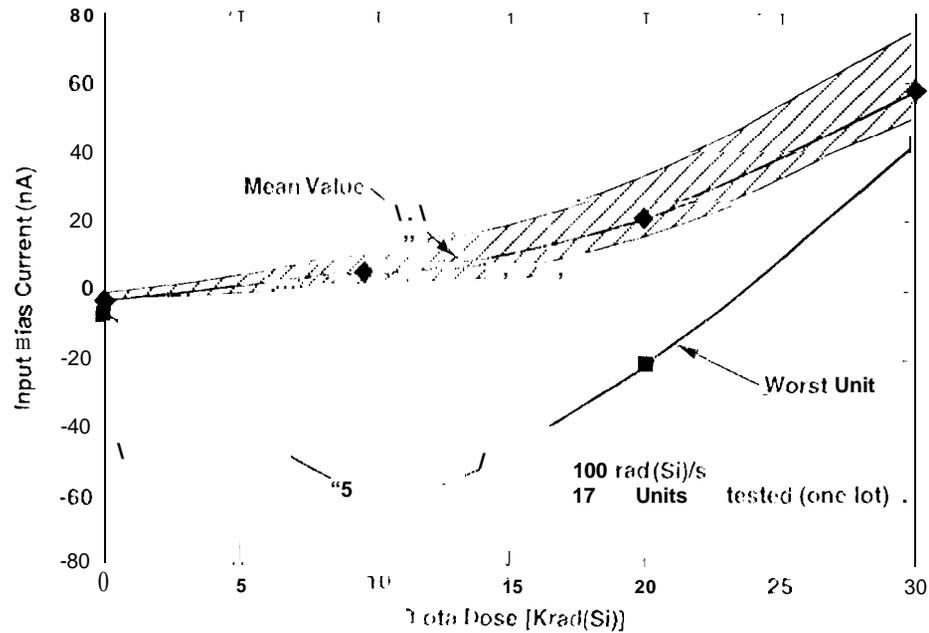


Microprocessor Test Methods: An Example of Manufacturing Variability

This figure shows recent total dose test results for microprocessors produced by two commercial vendors. Devices from one manufacturer exhibit very large changes in power supply current below 10 krad(Si), and functional failure occurs at slightly higher levels. Devices from the second manufacturer perform far better. Only small increases occur in power supply current, and devices continue to function even after 100 krad(Si).

Based on these results, the second manufacturer is clearly the better choice. However, with no detailed knowledge or control of the processing, it is not at all clear that the superior results of the second manufacturer can be relied upon in the future. The difference in the response of the two device technologies is in the field oxide, and the processing steps that affect the radiation response of the field oxide are often not very important in the commercial application of CMOS devices. Minor changes in processing could easily degrade the performance of this vendor to the point where there would be little difference in the radiation performance of the two suppliers.

OP-27 Input Bias Current vs. Total Dose



Linear Integrated Circuit Responses: An Example of Linear Device Complexity

Another problem that occurs with commercial parts is the possibility of large differences in the responses of different devices from the same wafer or processing lot. This problem is not fully appreciated because radiation testing is often done with very small sample sizes.

This figure shows the effect of total dose on input bias current of a commercial operational amplifier. Nineteen units were tested, with the same date code. Most of the devices behave in a very consistent manner, but one device has a much different radiation response, particularly at low radiation levels. The parameters of this device before radiation were consistent with those of the other eighteen units.

Characterizing this type of behavior is difficult and costly. Once identified, it must be taken into account in determining post-radiation design parameters. Conventional statistical approaches are of limited value in dealing with this type of behavior.

Summary

This Section Has Covered a Wide Range of Topics

- **Device Structures**
- **ionization Damage**
- **Transient Ionization Effects**
- **SEE Effects**

Much of the Presentation is Review Material

New Phenomena and Effects of Device Scaling Have Been Emphasized

Dose Rate Effects in Bipolar Devices

Latchup from Transient Ionization and Heavy Ions

Catastrophic Hard Errors in Advanced Devices

Summary

This section of the short course has discussed the response of several basic device technologies to various radiation phenomena. The main emphasis in the oral presentation is on new phenomena, such as hard error effects in highly scaled devices and the dependence of total dose damage in bipolar devices on dose rate. These are both interesting topics, which are not fully understood, but must be taken into account when designing future systems.

The course also discussed latchup in more detail because it has not been covered in as much depth in previous courses, and it is also likely to increase in importance as devices are scaled to smaller feature sizes.

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