GaAs MULTIPLEXERS FOR VLWIR DETECTOR READOUT BELOW 10 KELVIN

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A multiplexer and buffer based on GaAs JFET technology is presented. This multiplexer operates normally from room temperature down to 4 Kelvin and is suitable for the readout of Very Long Wavelength Infrared Detectors that must be cooled to below 10 Kelvin. The noise, dark current, and power dissipation of the multiplexer is presented and shown to be within the range required for typical VLWIR detector readout applications.

INTRODUCTION

Photoconductive and photovoltaic detector arrays for the very long wavelength infrared (VLWIR) are typically cooled to below 10 K to reduce the dark current, and improve the signal to noise ratio. It is necessary to have electronics that can buffer and multiplex the signals from each pixel in the array, but this is presents a challenge, since conventional silicon-based electronics do not operate well below 10 K. Previously it had been possible to run a wire from each pixel in the array to a multiplexer kept in a warmer electronics compartment, held at 60 K or above. However, this wire bundle carries heat to the focal plane cold head, and in addition the wires are susceptible to noise pickup from microphonics or EMI. This approach is becoming less practical for the larger array sizes and sensitivities expected of future NASA missions. Therefore, future missions require development of readout electronics that can operate at the detector ambient temperature and that can be placed in immediate contact with the VLWIR detector array. Such electronics are also required for some visible or near infrared detector arrays, such as the star trackers for the Space Infrared Telescope Facility or for the Gravity Probe-B instrument, in which the visible star tracker must be mounted on a cryogenic platform.

For semiconductor electronics to function properly below 10 K, the semiconductor technology must avoid or circumvent carrier freeze-out. One way to avoid freeze-out is to degenerately dope the semiconductor, that is, dope it so heavily that the bound state orbits overlap and it becomes possible for an electron to travel from one bound state to the next. The individual bound states then transform into a band of traveling wave states that merge with the ordinary conduction or valence band . When this happens, the semiconductor is immune to freeze-out because the carriers still conduct even when occupying the lowest energy states. While all semiconductors become degenerate at some doping level, silicon

does not become degenerate until concentrations on the order of 10^{18} cm^{-3}, which is too high to allow depletion at reasonable voltages. On the other hand, because of the small electron effective mass in GaAs, n-type GaAs becomes degenerate at a concentration of approximately 5×10^{15} cm^{-3}[1]. This makes it feasible to build an n-channel GaAs JFET that is immune to carrier freeze-out, and that operates normally from room temperature down to below 4 K.

DISCRETE JFETS

At JPL, we have been investigating GaAs JFETs for use in VLWIR readout electronics.[2,3] For this application the critical parameters are the input leakage current and the amplifier noise, as well as the power dissipation, so we first concentrated on the development of discrete GaAs JFETs with low leakage current and noise. The GaAs JFETs were fabricated using an etch-back technique. Molecular beam epitaxy was used to grow the layer structure. Starting on a semi-insulating GaAs substrate, and undoped buffer layer is grown, followed by the n-type channel, and ending with the p^{+}-type gate layer. Wet chemical etching through the gate and channel layer and into the buffer layer is used to define the device mesas that electrically isolate one transistor from another. Wet chemical etching is also used to etch away the gate layer over the source and drain regions and expose the n-type channel. Metal layers of nickel, germanium, and gold are deposited by electron beam evaporation and then alloyed to form the ohmic contacts to the source and drain. Metal layers of titanium, platinum, and gold are deposited to contact the p-type gate electrode. These metal layers do not alloy. The completed device structure is shown in Figure 1.

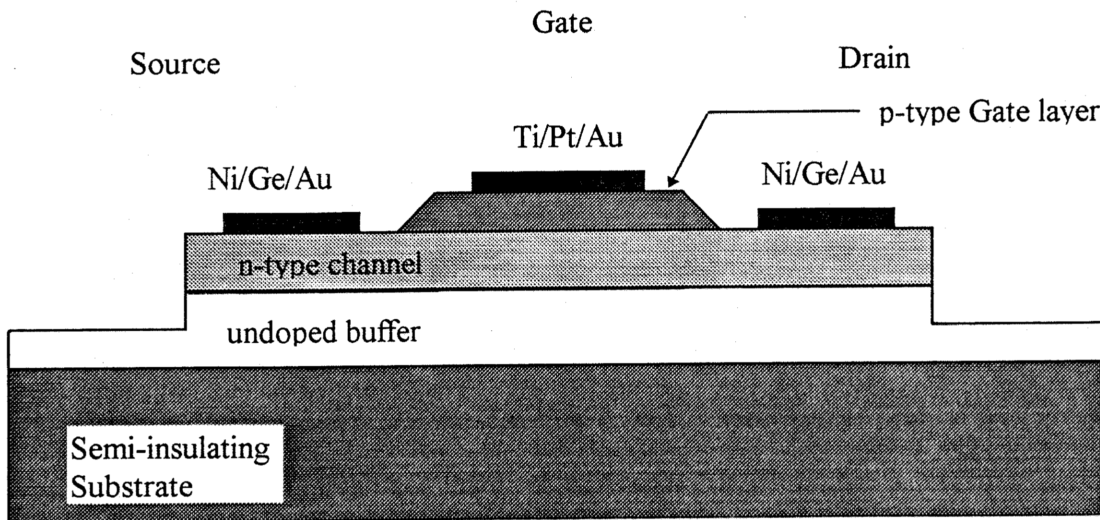

Figure 1: A cross section of a GaAs JFET discrete GaAs JFET.

The wet chemical etching was done using a highly isotropic HF-based etchant[4] using a photoresist etch mask. This results in a gently tapered profile of the gate and mesa edges, reducing the electric field concentration that occurs at sharp edges. The resulting JFETs having very low input leakage current. When measure at 4 K, these devices functioned normally without any kinks or other anomalies, exhibiting a leakage current below 1 fA, and an input referred noise typically on the order of 1 $\mu V/Hz^{1/2}$ at 1Hz, when biased with 1 to 10 μA drain current. The results for these discrete JFETs has been reported previously [5,6].

THE MULTIPLEXER

Having demonstrated suitable discrete devices, the next step was to develop a low scale integrated circuit suitable for the readout of VLWIR photovoltaic linear arrays. This was realized by constructing an 8x1 linear buffer and multiplexer using a source-follower per detector architecture. A compressed schematic of the multiplexer is shown in Figure 2.

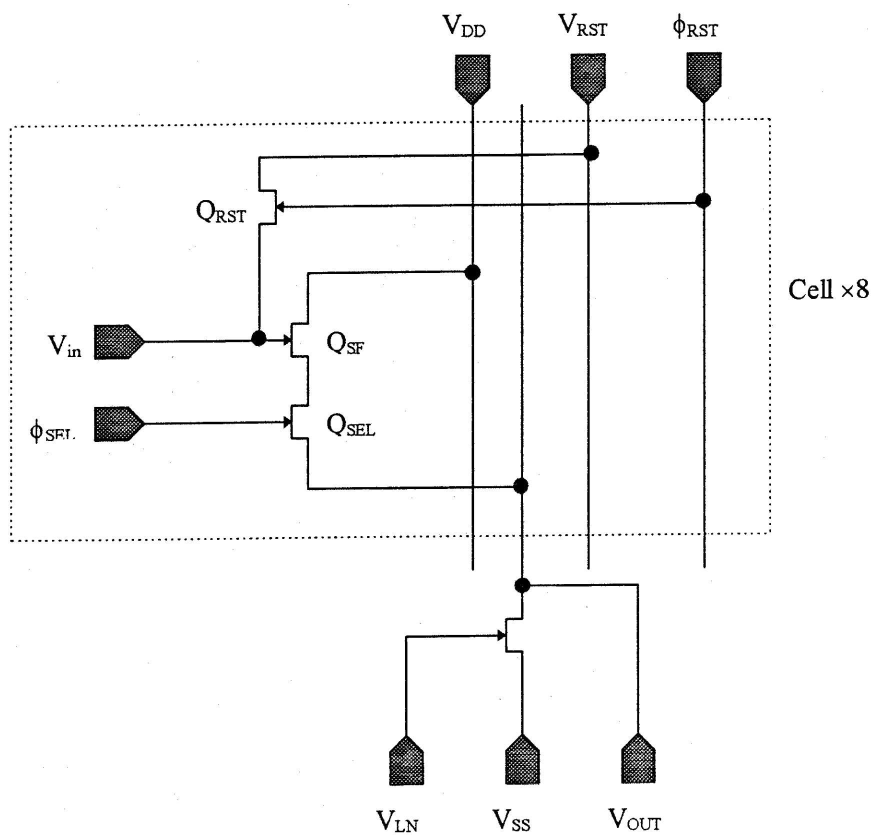

Figure 2: A compressed schematic of the GaAs JFET multiplexer showing the common circuitry and one cell. The full circuit has eight cells.

This multiplexer consists of 8 cells connected to a common load transistor and a set of common column lines. The multiplexer can read out a linear array of 8 VLWIR detectors; the anode of each detector would be connected to the V_{in} pad in each cell by a wire bond, and the cathodes would all be connected to ground.

The circuit operation is as follows: The dc biases V_{DD}, V_{RST}, V_{LN}, and V_{SS} are set to there appropriate values. At the start of a frame, ϕ_{RST} goes high, turning on the JFET switch Q_{RST} in each cell. This resets the circuit by applying a reverse bias of V_{RST} on each detector. ϕ_{RST} then returns low, turning off Q_{RST}, and leaving V_{RST} stored on the input capacitance of each cell. (This capacitance is the sum of the detector capacitance, the gate capacitance of Q_{SF}, as well as any stray capacitance in the wiring.) During the integration period, photons striking the detectors cause the detectors to discharge, and the voltage across the detectors relaxes toward zero, depending on the amount of photon flux integrated. To read out any cell, the corresponding ϕ_{SEL} is brought high, turning on the select transistor Q_{SEL} in that cell, and connecting the source of Q_{SF} to the column bus. V_{LN} and V_{SS} are set so as to bias the load transistor Q_{LOAD} as a constant current sink.

CHARACTERIZATION

Several multiplexers of the type described in the previous section were fabricated and tested. The best results were obtained for a multiplexers fabricated from material with the layer thicknesses and doping concentrations listed in Table 1. All of the results in this section are for a multiplexer made from this material.

Layer	Thickness (nm)	Doping type	Doping Concentration cm^{-3}
Gate	50	p^+-(Be)	$>5x10^{18}$
Channel	375	n-(Si)	$5x10^{16}$
Buffer	1000	undoped	-

Table 1: The layer thicknesses and doping concentrations for the GaAs material from which the multiplexer described in this section was made.

The multiplexer was measured at 4 K under a variety of circumstances in order to characterize its performance. First, the gain of the source-follower was measured using the set-up shown in Figure 3. An external current sink of 50 μA was attached to V_{OUT}; the on-chip current source was not used. V_{DD} was set to 3 V, and Q_{RST} was turned on in each cell by setting ϕ_{RST} to 0.5 V. One cell was enabled by setting the corresponding ϕ_{SEL} to 1 V; ϕ_{SEL} for the others cells was set to -5 V, disabling them. A slow square wave toggling between 0.1 and 0.6 V was applied to V_{RST} and the amplitude of the corresponding square wave at V_{OUT} was recorded as 0.44 V. The gain is then given by equation 1:

$$Gain = \frac{\Delta V_{out}}{\Delta V_{RST}} = 0.88 \qquad (1)$$

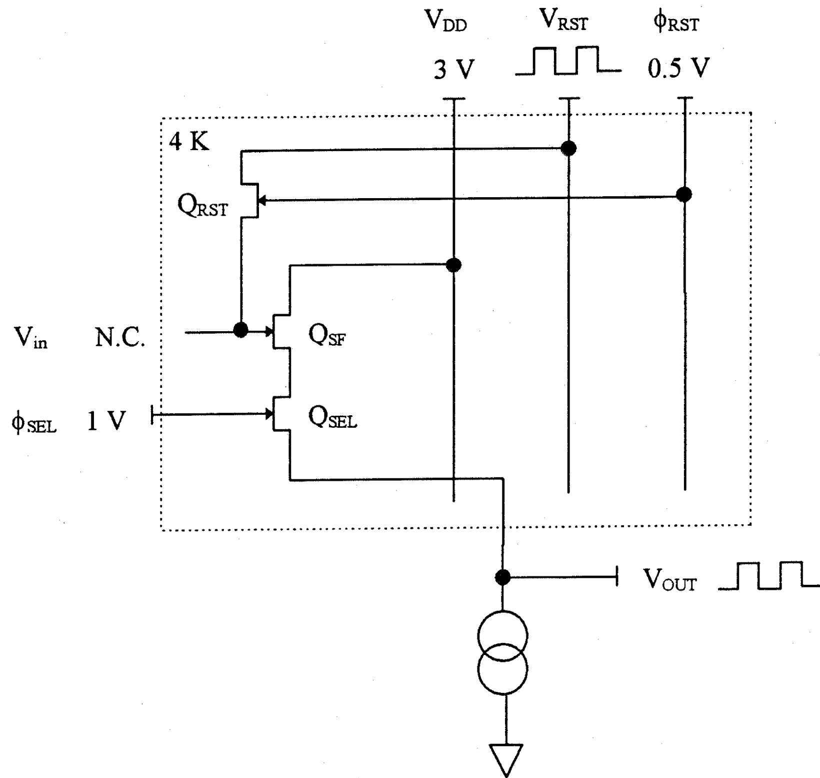

Figure 3: The experimental setup for measuring the source-follower gain. A square wave injected on the reset voltage node results in a square wave output. The voltage gain is ratio of the amplitudes.

The input capacitance was measured using the set-up shown in Figure 4. A 1 pF chip capacitor was bonded directly onto the contact pad for V_{in} on one cell on the chip. A bond wire was used to connect the other side of the capacitor to an external lead. The bias voltages were the same as for the gain measurement described above, except that V_{RST} was held constant at 0.1 V. The voltages on the ϕ_{SEL} lines were set to select the cell with the input capacitor and to deselect all others. A low frequency square wave was applied to one side of the capacitor, producing a square wave on the output. The resulting ratio of the output amplitude divided by the input amplitude was 0.85.

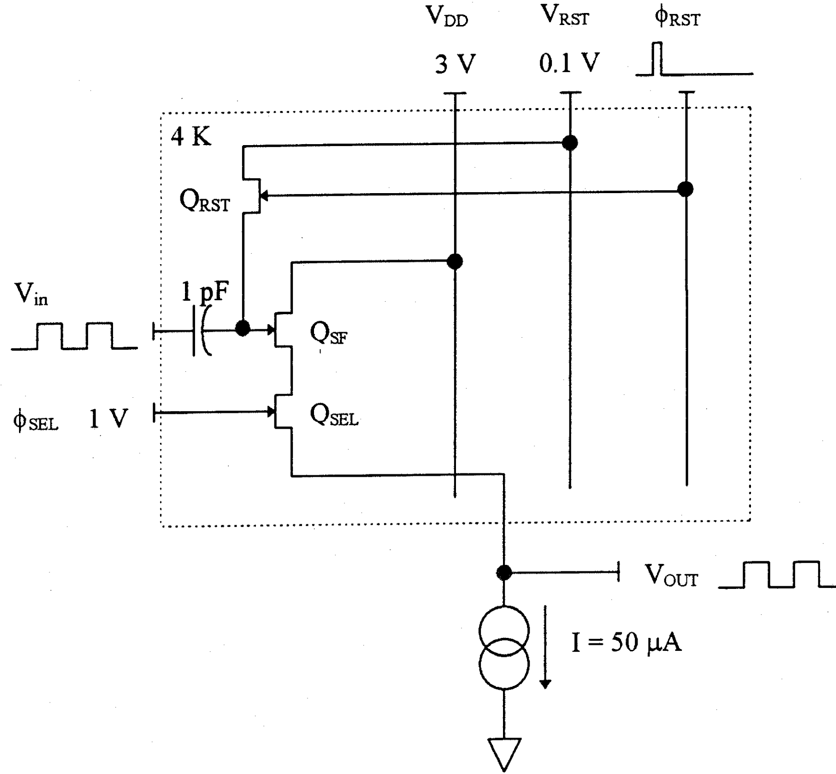

Figure 4: The experimental setup for measuring the multiplexer input capacitance. A square wave injected onto the input through a 1 pF capacitor, producing a square wave on the output. The input capacitance can be calculated from ratio of the amplitudes.

The multiplexer can be modeled as a buffered capacitive divider shown in Figure 5. This makes obvious the equation relating the input and output amplitudes in terms of the input capacitance. This equation is shown in Equation 2.

$$\Delta V_{OUT} = \left(\frac{1\ \text{pF}}{C_{in} + 1\ \text{pF}} \right) \cdot A_V \cdot \Delta V_{in} \tag{2}$$

Using the voltage gain from the set-up of Figure 3, $A_V = 0.88$, and the signal ratio from the set-up of Figure 4, $\Delta V_{OUT} / \Delta V_{IN} = 0.85$, the input capacitance is calculated as:

$$C_{in} = 0.035\ \text{pF} \tag{3}$$

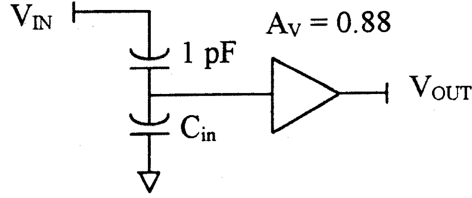

Figure 5: The equivalent circuit of the multiplexer with the input capacitor, forming a capacitive divider.

The leakage current was measured using the set-up shown in Figure 6. This set-up is similar to that used for the gain and leakage measurements. The input nodes are left floating. One cell is selected, and all others are deselected. ϕ_{RST} is pulsed high then returned low at the beginning of the measurement which sets the voltage on the input node to V_{RST} and then isolates the node, allowing the input voltage to drift due to leakage currents, which is effectively integrated on the input capacitance. The output voltage is sampled once immediately after ϕ_{RST} is brought low, then again at several other times within an integration period T. The leakage current is related to the drift in the output voltage by Equations 4 and 5.

$$I_{leakage} = C_{in} \frac{dV_{in}}{dt} \tag{4}$$

$$I_{leakage} = C_{in} A_v \frac{\Delta V_{OUT}}{\Delta T} \tag{5}$$

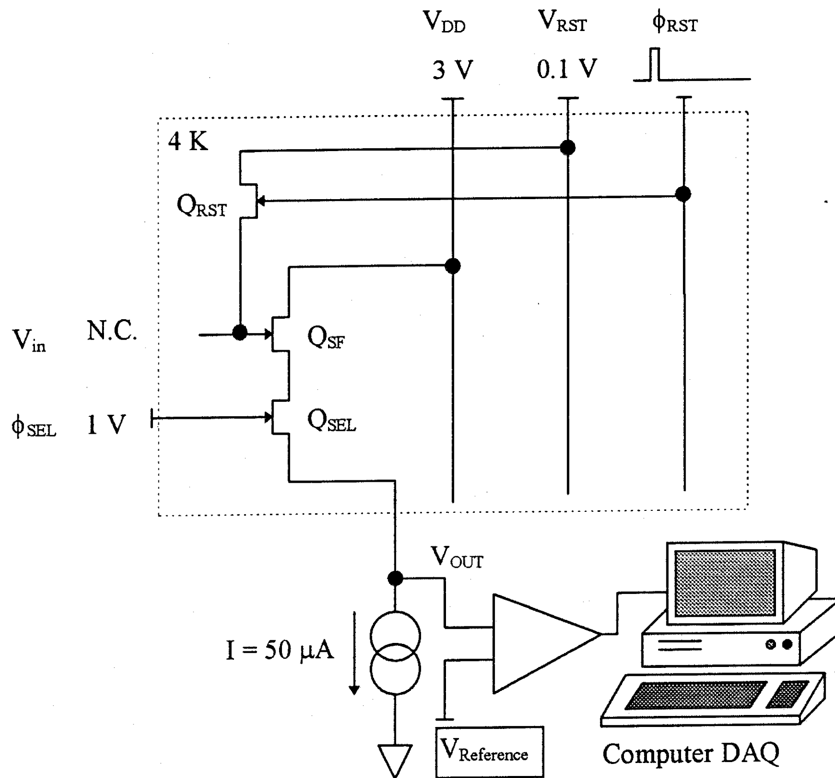

Figure 6: The experimental set-up for finding the input leakage current by measuring the drift in the output voltage in time.

The measured output drift as a function of time for a typical pixel is shown in Figure 7. As can be seen, the behavior exhibits an anomaly, as the initially the output voltage drifts more negative, then the trend reverses itself, and begins to drift toward more positive voltages. The reason for this is not known at this time.

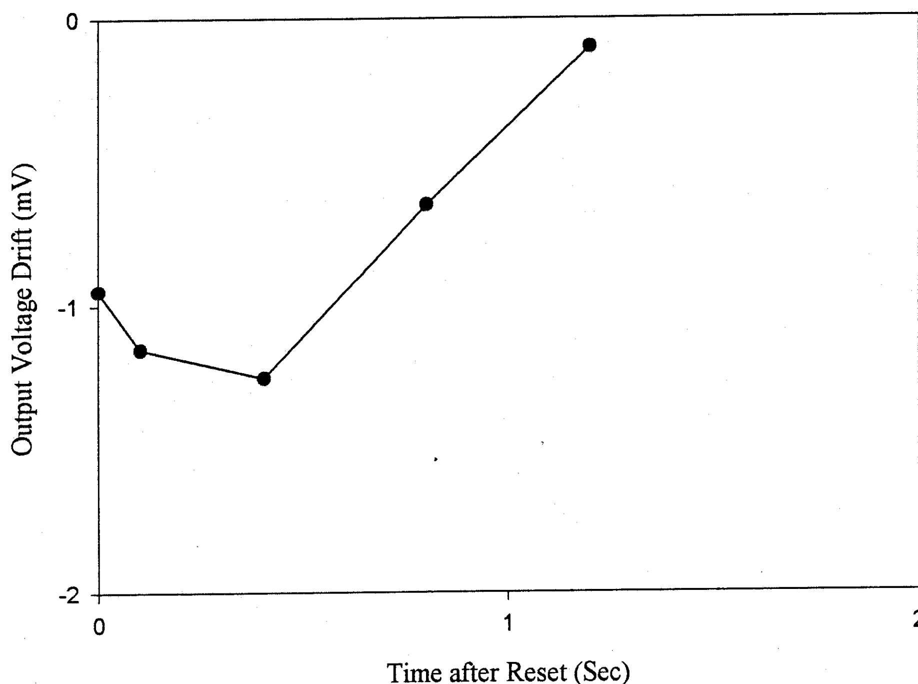

Figure 7: The drift in the output voltage as a function of time after the end of the reset period. The output voltage is measured with respect to a reference voltage set to null the output within a few millivolts.

The noise was measured using the set-up shown in Figure 8. The set-up is very similar to that shown in Figure 6. As in that setup, one cell is selected, and all others are deselected. The multiplexer is not clocked during the noise measurement. ϕ_{RST} is pulsed high then returned low at the beginning of the measurement which sets the voltage on the input node to V_{RST} and then isolates the input as before. For the noise measurement, however, the output voltage is fed by ac coupling into a dynamic signal analyzer. The dynamic signal analyzer takes a time series of measurements and then performs an FFT on the data to get a noise spectrum between dc and 100 Hz. The resulting noise spectrum is shown in Figure 9. The noise is on the order of 1 $\mu V/Hz^{1/2}$ between 1 and 10 Hz.

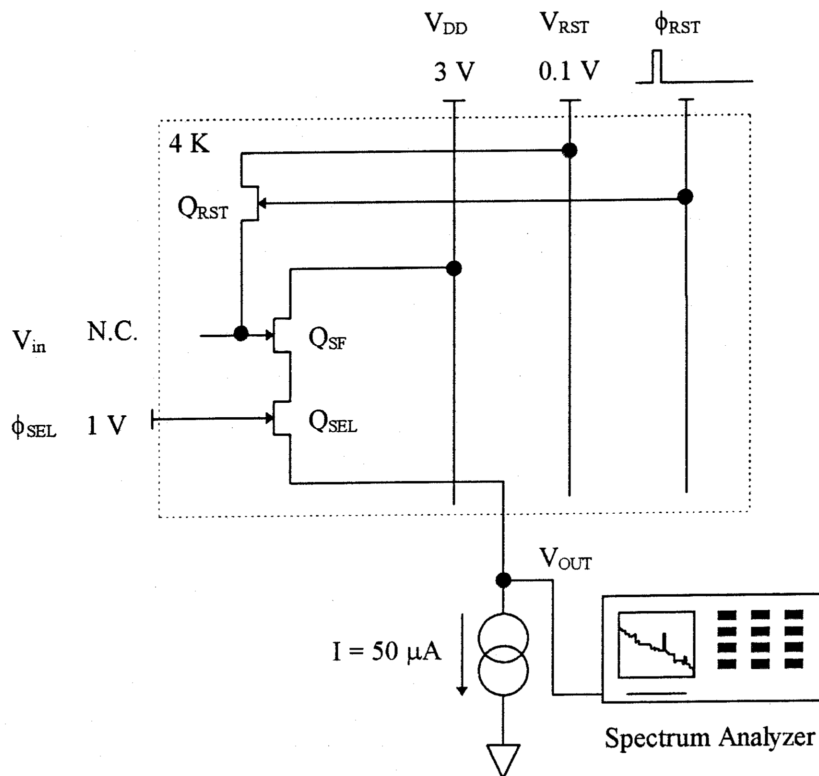

Figure 8: The experimental setup for measuring the multiplexer noise. The multiplexer was not switched during the measurement.

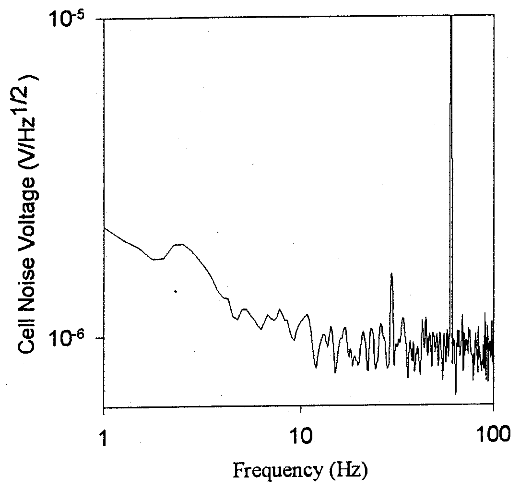

Figure 9: The noise spectrum for one pixel of the 8x1 multiplexer. The reset switch is open, and the multiplexer is not clocked during the measurement.

SUMMARY

A 8x1 multiplexer suitable for the readout of VLWIR detectors operating below 10 K has been fabricated using JPL's cryogenic JFET technology. This JFET technology uses a p^+ gate with an n-type channel, making the JFETs immune to carrier freeze-out effects at cryogenic temperatures. In addition, a highly isotropic HF-based wet chemical etchant is used with a photoresist mask to define the gate and mesa regions. This etchant provides a very smooth etch profile, eliminating sharp edges the lead to abnormally high field concentrations, and thereby reducing excess gate leakage current.

The multiplexers made using this cryogenic GaAs JFET technology operate normally from room temperature down to 4 K. Such a multiplexer is suitable for the readout of VLWIR detectors requiring cooling below 10 K. A multiplexer has been tested without a detector attached and its performance is shown to be adequate for VLWIR readout. The effective input capacitance was approximately 0.035 pF. The input leakage current was less than 100 electrons per second. The voltage gain is 0.88, and the low frequency noise is on the order of 1 $\mu V/Hz^{1/2}$ at 1 Hz.

ACKNOWLEDGEMENT

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