# High Responsivity CMOS Imager Pixel Implemented in SOI Technology

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## Introduction

Availability of mature sub-micron CMOS technology and the advent new low noise active pixel sensor (APS) concept have enabled the development of low power, miniature, single-chip, CMOS digital imagers in the decade of 1990's. [1] The primary advantages of CMOS APS include low-cost, low-power (100-1000x lower than CCDs), simple digital interface, random access, simplicity of operation (single CMOS compatible power supply), high speed, miniaturization, radiation hardness, and smartness by incorporating on-chip signal processing circuits.

However, there are several limitations in implementing CMOS imagers in deep sub-micron technology. Reduction in depletion length needed for implementing sub-micron MOSFETs as well as the reduction in the epitaxial silicon thickness cause a reduction in quantum efficiency (QE) and an increase in pixel-to-pixel cross-talk (CT) due to collection of photo-generated electrons through diffusion over field-free region. Furthermore, beyond 0.25 $\mu$m CMOS technology, the use of SOI technology seems imminent. Typical SOI designs use 40-200 nm thick silicon films, depending upon whether it is partially or fully depleted. In either case, the film thickness is too small to provide adequate absorption of photons in the visible spectrum. For instance, only a small fraction (< 5%) of 600 nm photons is absorbed in a SOI film of 100 nm thickness [2]. Hence, SOI technology is generally considered to be incompatible with CMOS imager implementation.

## Implementation

The schematic and cross-section of the front-illuminated high responsivity CMOS imager pixel implemented in SOI technology is shown in figure 1. The key to achieving high photo-response is to implement the photodiode in the SOI substrate (also called the "handle-wafer"), while the thin SOI-film is used for implementing only the FETs necessary for pixel readout. As shown in figure 1, the pixel consists of the handle-wafer photodiode, and three SOI FETs. The two n-FETs ($M_{sf}$ and $M_{sel}$) serve as source follower input and row selection FETs respectively. The voltage from the pixel is output over the column line when $M_{sel}$ is activated. A p-FET ($M_{rst}$) is used to clear the photodiode of all charges and reset it to the power supply potential at the beginning of every exposure.

The handle-wafer thickness is large and its doping can be chosen to be very low ($<10^{15}/cm^3$). While low handle-wafer doping does not degrade SOI FET performance, it provides excellent isolation between transistors, and provides large depletion widths (> 3 $\mu$m). Thus the photo-electrons generated in the handle-wafer are collected under a drift field in the $n^+$ region, providing excellent photo-response, and minimal cross-talk. The holes are rapidly drained away to the $p^+$ implant that is biased at ground potential. The $p^+$ implant is in form of a guard ring as shown in figure 2, for efficient disposal of the photo-generated holes. Figure 2 shows the pixel layout implemented in a special 0.35 $\mu$m fully depleted SOI technology made available by MIT/LL. It consists of horizontally continuous handle-wafer islands, interspersed with SOI regions. The SOI regions consist of the FETs that are connected to two horizontal bus (RST and ROW-SEL), and two vertical bus (COL-BUS and Vdd) as shown in figure 2. The pixel pitch is 12x12 $\mu$m and the optical drawn fill-factor is 50%. However, the depletion region in the handle-wafer spreads horizontally as well, causing the effective fill-factor to be much higher than 50%.

The cross-section shown in figure 1 is eminently compatible with conventional SOI process flow. It can be implemented with only one extra lithography step to etch through the buried oxide. No additional high temperature steps are necessary, since $n^+$ and $p^+$ implants in the handle-wafer can be done during source and drain implants for the SOI FETs. Thus, this implementation approach makes it feasible to implement high performance imagers in mainstream SOI technology. In addition, due to superior isolation provided by SOI technology, it also becomes possible to provide integrated single-chip smart imager solutions far beyond what is possible with bulk CMOS.

## Experimental Results

A 128x144 format imager with different pixels in 32x32 clusters were made for evaluation of CMOS imager

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performance. The proof-of-concept detector was found to respond in the entire visible region from 400 nm to 1100 nm (silicon cut-off). The spectral response shown in figure 3 indicates that the photoresponse is high (> 4 μV/photon), and flat over a large wavelength region of 440 nm to 900 nm, indicating the presence of large depletion widths. Furthermore, SOI-imager peak responsivity is nearly double that of a state-of-the-art bulk-CMOS imager. Bulk-CMOS imager also exhibits markedly poor response at longer wavelengths. The loss of response in short wavelength is due to the presence of traps in the oxide-handle-wafer interface, and can be eliminated through additional blanket implants. In conclusion, a SOI CMOS imager with excellent photo-response over a large spectral range is demonstrated for the first time, with responsivity exceeding that of imagers implemented in bulk CMOS.

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**References**

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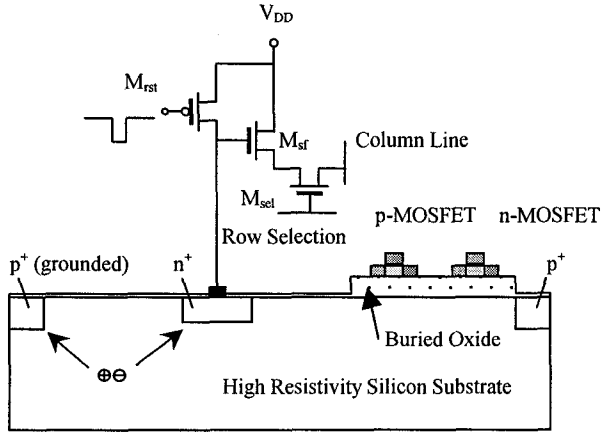


Figure 1: Cross-section and schematic of a SOI CMOS imager pixel. The photodiode is implemented in the handle-wafer

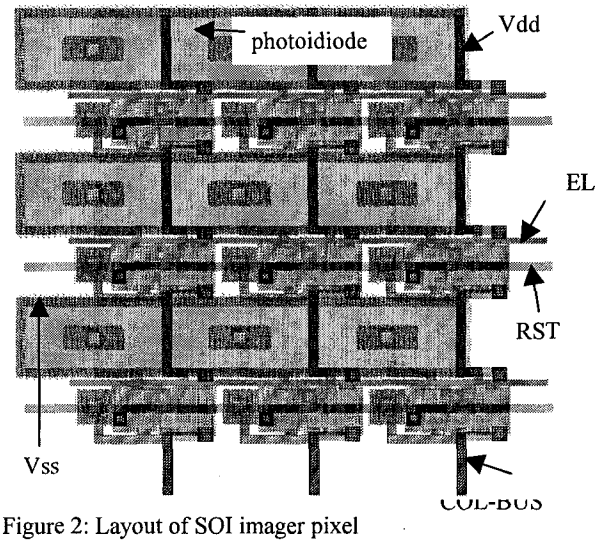


Figure 2: Layout of SOI imager pixel

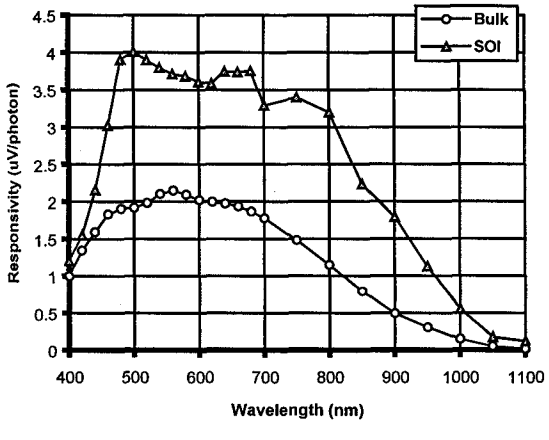


Figure 3: Comparison of Responsivity of imagers implemented in bulk and SOI technology