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An Open Systems Architecture of a Standardized Command Interface Chip-Set for Spacecraft

B. Ian Ruiz
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
M/S: 198-138
Pasadena, CA 91109
818-354-0625
Ian.Ruiz@jpl.nasa.gov

The Jet Propulsion Laboratory's (JPL) X2000 Integrated First Delivery Project (IFDP) is focusing on the development of revolutionary technologies that will enable JPL to enhance our future solar system exploration missions through the advent of a standardized set of avionics hardware, which will also enable rapid development. This is being accomplished by constructing a distributed architecture that utilizes several different busses to disseminate commands to the various sub-systems. As such, the Power System Electronics (PSE) sub-system is developing a standardized command interface chip-set that primarily consists of two mixed-signal ASICs'; the Command Interface ASIC (CIA) and Analog Interface ASIC (AIA). This chip-set provides an intelligent gateway between the system's flight computer and the control of the spacecraft's loads, valves, and pyrotechnics as well as the regulation of the power and battery bus.

The CIA-AIA chip-set receives commands over a redundant set of I2C busses that conform to a derivative of the Phillips I2C bus standard. Depending upon the type of command received it is then either decoded and executed entirely in hardware or decoded and executed by an embedded 8051 microcontroller. The embedded controller can execute from on-chip micro-code or can be post-production customized by executing from an external PROM. In addition, the CIA is capable of digital commanding and analog (voltage and current) monitoring of 16 power switches that are packaged in the form of four Power Actuating Switching Modules (PASM), which is being developed by Lockheed Martin. Furthermore, the CIA can address up to 63KB of external data memory or other memory mapped I/O via the embedded 8051's external data memory bus.

The CIA-AIA chip-set is being used by X2000 to construct a distributed power control system that will in turn be used for a wide variety of large or small solar system exploration missions. The open systems architecture of this chip-set enables a multitude of other mission uses, of which JPL has just begun to explore.

The CIA provides the following capabilities:

- 1KB of on-chip RAM
- 8KB x 8 of on-chip ROM
- Interface with two redundant I^2C busses.
- Provide Fault Protection.
- Monitor 4 analog channels with an internal 8-bit analog to digital converter.

- Command (digital) and Monitor (analog voltages and currents with internal 8-bit ADC) four Power Actuated Switching Modules (PASMs), which equate to 16 switches.
- Perform intelligent data sequencing and buffering tasks using an embedded 8051 microcontroller.
- Capable of accepting power from two redundant power sources.
- Capable of Addressing up to 63 KB of external RAM or other memory mapped I/O
- Capable of booting the embedded 8051 microcontroller from an external PROM.

The AIA is a companion chip to the CIA and provides two electrically isolated physical drivers for the redundant I2C busses. This was necessary for X2000's fault tolerant implementation of the Phillips I2C bus.

The CIA and AIA are currently in the design phase with a prototype build planned to be available in July of '00 and flight parts available in May of '01. The first mission planned to use this chip-set will be the Europa Orbiter, which may launch as early as late 2003.