An 800 GHz Broadband Planar Schottky Balanced Doubler

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Abstract

A broadband planar Schottky balanced doubler at 800 GHz has been designed and built. The design utilizes two Schottky diodes in balanced configuration on a 12 μm thick Gallium Arsenide (GaAs) substrate as supporting frame. To minimize dielectric loading of the waveguides and reduce RF losses in passive circuits, a new fabrication technology is used where the GaAs substrate under the transmission lines is removed during the back-side processing, leaving free standing metal lines suspended in air from GaAs frame. Metal beamleads are used for DC and RF contacts with the waveguides, and they allow the doubler chip to be dropped inside the split waveguide block, making assembly procedure simple, fast, and robust. This broadband doubler (736 GHz to 848 GHz) achieved $\approx$ **10%** efficiency at 765 GHz, giving **700** μW of output power when pumped with about 6.5 mW of input power at room temperature. This represents the best performance from any doubler at these frequencies to date in literature. This paper describes the design, fabrication, assembly, testing, and performance both at room temperature and at cryogenic temperatures.

I. Introduction

MILLIMETER and submillimeter wave detectors for astronomical, remote sensing, and atmospheric sciences applications are being developed with ever-increasing capability, to meet the growing demands of the immensely powerful set of new and future space-borne and ground-based telescopes and facilities. Many of the instruments have cryogenically cooled heterodyne receivers for use in high sensitivity, high resolution spectroscopy measurements. These receivers require wideband tunerless local oscillators (LO) to pump superconductor insulator superconductor (SIS) and hot electron bolometer (HEB) mixers.

Current state-of-the-art solid state sources above 200 GHz are constructed from chains of cascaded Schottky-barrier varactor diode frequency multipliers. Using new planar *substrateless* technology [1], we have designed and developed a 800 GHz broadband doubler for use in the 730 GHz to 850 GHz frequency range. The motivation for designing a frequency multiplier in this frequency range is two fold. The primary goal is to use this doubler as a LO source to pump SIS receivers for spectroscopic measurements of a few transition lines. The important transition lines at these frequencies are: (i) at 807 GHz **CO 7 $\rightarrow$ 6** transition line, (ii) at 809 GHz **C** transition line, and (iii) at 835 GHz $\mathbf{CH^+}$ transition line. The secondary motivation is to use this doubler as the input to pump a 1600 GHz doubler. There is an important transition line at 1612 GHz; **CO 15 $\rightarrow$ 14** transition line.

This 800 GHz balanced doubler incorporates two symmetrical pairs of diodes configured in such a way that they only respond to odd harmonics at the input and even harmonics at the output, making it easier to separate the input and output frequencies without any filter structure [2].

II. Design, Fabrication and Assembly

The 800 GHz balanced doubler design process involve a few steps: Advanced Design System's (ADS) [3] nonlinear harmonic balance simulator is used to optimize the doping profile and diode dimensions like the anode and mesa size for a given input power (7 mW in our case). From this simulation we also calculate the diode junction characteristics as a function of frequency and the embedding impedances for optimum performance of the multiplier. Then the multiplier input and output matching circuits are synthesized using High Frequency Structure Simulator (HFSS) – a finite element electromagnetic simulator [4]. Using the S-parameters obtained from HFSS simulations, and the diode properties obtained from the nonlinear diode simulations, we optimize the design in a linear simulator with waveguide matching components for maximum

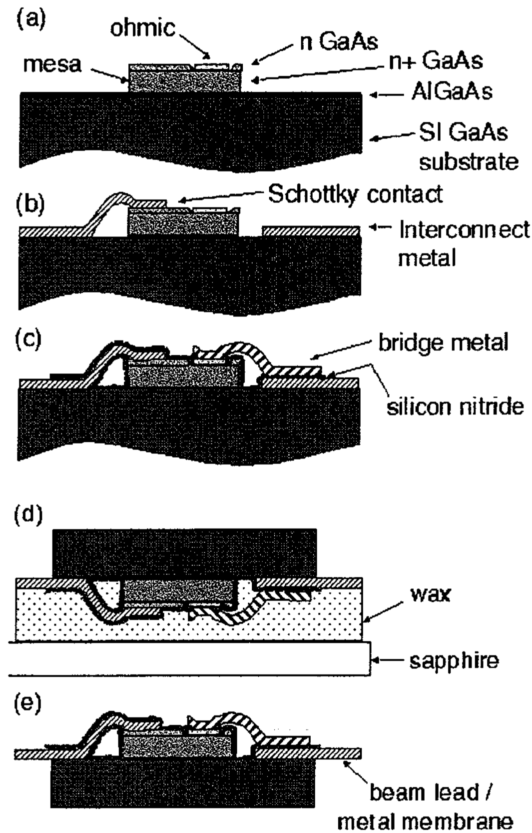

Fig. 1. Fabrication process steps: (a) Ohmic and mesa definition, (b) interconnect metal and air-bridged Schottky deposition, followed by passivation and bridge metal definition, (c) backside thinning and device separation, (d) release of device from carrier wafer.

doubler efficiency.

The input signal is directly coupled to the diodes which are placed in the reduced height input waveguide. The output signal is coupled to the output waveguide by means of E-field probe. The input matching is accomplished with the input backshort and waveguide matching sections, and the output circuit is optimized using waveguide matching components, a waveguide channel connecting the input and output waveguides, and a small open stub on the input side of the diode which tunes out the inductance of the diode structure at the output frequency. An integrated Si_3N_4 metal insulator metal (MIM) capacitor, at the end of output coupling probe, is used as RF short and DC bypass. One of the critical design criteria is to make the input reduced height section below cut-off for TM_{11} mode at the output frequency. The holder for the MIM capacitor should also be designed carefully not to allow any output frequency signal leak through it. Fig. 2 shows the diode circuits placed inside the split waveguide block.

The device and circuitry for the doubler is fabricated on Gallium Arsenide (GaAs) substrate using optical lithography and conventional epitaxial layers. What is unique about this fabrication process is the use of metal beam leads for DC and RF contacts with waveguides. Also, to minimize dielectric loading of the waveguides and reduce RF losses in passive circuits, GaAs substrate under the transmission lines is removed in back-side processing, leaving free standing metal lines suspended in air from GaAs frame. The starting

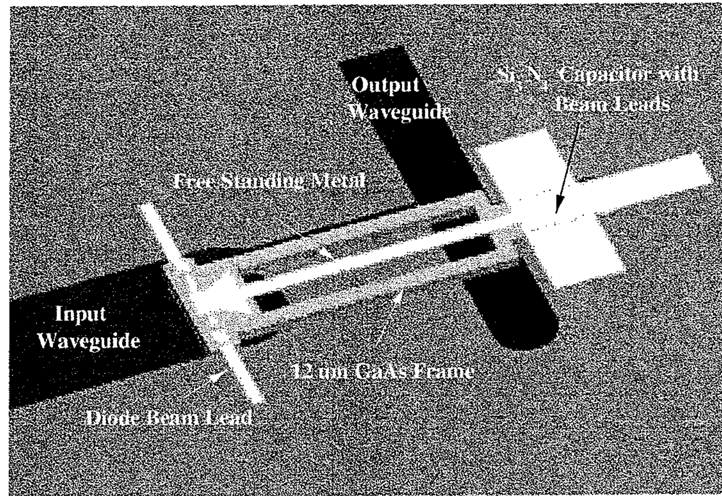

Fig. 2. Sketch of the 800 GHz doubler. The doubler chip rests on its beam leads on the split waveguide block.

material for device fabrication is semi-insulating GaAs with epitaxial layers grown by molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) process. The fabrication process steps for *substrateless* technology is shown in Fig. 1. The diode structure consists of a $\sim$ 200 nm thick n-type (4×10^{17} /cm^3 doping) Schottky layer on top of a heavily doped (5×10^{18} /cm^3) 1.5 μm thick n+ contact layer grown on a 50 nm $Al_{0.5}Ga_{0.5}As$ etch-stop layer. After a few process steps which define the anode and the mesa, and develops the air bridges and other metallic circuit areas, the GaAs substrate is thinned to 12 μm by lapping, polishing, and wet etching. Then GaAs is removed from selective interconnect metals and circuits, and the individual chips are removed from the diode wafer [1].

Assembly for this device is simple, fast, and robust. The diode chip is dropped inside the split waveguide block with the diode beam leads resting on the waveguide metal. The beam lead from the MIM capacitor is bonded to a chip capacitor which in turn is wire-bonded to the bias connector. The assembled doubler picture is shown in Fig. 3.

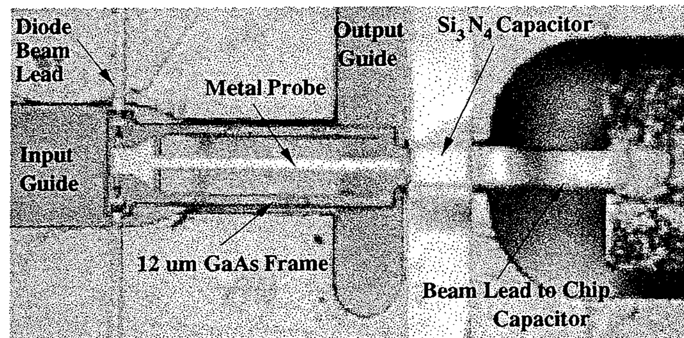

Fig. 3. Picture of the assembled 800 GHz doubler. The anode size for the doubler is 1.1 μm $\times$ 1.0 μm.

III. Measurement and Results

The doubler was measured using 400 GHz input signal derived from a Gunn oscillator and power amplifiers at 100 GHz and two doublers at 200 GHz and 400 GHz respectively [5]. Input and output power was measured using a calorimeter [6]. The waveguide dimension for the output waveguide is 12 inches × 6 inches. A transition from the output waveguide to W-band was used to connect the doubler to the calorimeter. The performance of the doubler at room temperature is shown in Fig. ??. No corrections were made for losses within the multiplier block or in the external waveguide adaptor. NOTE: in the result graph, mention about the anode size.

IV. Conclusion

We have designed and evaluated a wide band fixed tuned 800 GHz balanced frequency doubler... We also evaluated the multiplier at cryogenic temperatures in a calibrated dewar, using a corrugated horn. This represents the best performance from any doubler at these frequencies to date in literature.

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