Deep Impact PPC50 Performance Report (DRAFT)

Purpose

The Deep Impact (DI) project needs to collect realistic performance measurements of the target processor hardware, for the purpose of measuring the adequacy of the proposed X2000 real PPC750 for the DI mission. The desire is to execute a legacy spacecraft flight software system on a commercial equivalent of the target processor hardware. The closest equivalent COTS product is a Motorola PowerPC 750 Compact PCI single board computer (SBC).

The purpose of the performance testing is to collect information about the effects of system memory usage by an existing set of flight software on CPU performance. Specific issues are the performance effects of operations requiring the reloading of the L1 cache (cache misses) and use of the relatively slow system memory bus. The DS1 flight software (version M3 and M6) comprise the desired legacy spacecraft flight software, and it has been ported to a PPC750.

Objective - to evaluate the performance of the PPC750 flight computer under a variety of typical high CPU utilization Flight Software activities.

The performance evaluations will be used by the DI team in determining where performance problems may arise and whether the performance of a single PPC570 flight computer is adequate for use on the mission.

Success Criteria

1. Provide sufficient performance data for the PPC750 flight computer to allow the DI project to determine whether their current design for flight computer hardware and software is adequate to meet their mission goals.
2. Produce a report that establishes a set of typical flight software performance baselines for the PPC750 flight computer that allow a potential user to evaluate the capability of the compute to meet their missions goals.
3. Produce a report that the X2000 flight compute team can agree is an accurate representation of the performance capability of the PPC750 flight computer.

Technical Approach

Testing:

- Use the DS1 PPC750 testbed (babybed) in the Mist Avionics lab to run the DS1 Flight Software.
- The data will consist of measurements of ten percent of available processing time used by each of the approximately sixty major DS1 tasks, include idle time. In addition data consisting of measurements of L1 instruction cache misses, L1 data cache misses and total instructions executed during the test will be collected.
- From this data close estimates the actual instruction per second performance of the processor during different operational loads can be calculated.

- During the test the L1 cache will be enabled and the L2 cache will be disabled since the flight configuration for Deep Impact has no L2 cache
- Performance measurements were recorded according to one of the following two guidelines:
  - The activity was repeated six times recording data cache misses half the time and instruction cache misses the other half (explain why ie tracking register limitations prevent both simultaneously
  - Measurements were recorded repeatedly until the activity completed. These test were run twice.

Tests: Describe what was actually done below as to version

- Using unmodified DS1 FSW Version M3:
  - Generic Cruise Idle (no navigation, maneuver, or science activities)
  - A Maneuver - Detumble
  - Collection and Downlink of Science Telemetry - DSEU during scan and burst modes
  - Collection and Downlink of an OpNav image with image compression (requires version M6)
  - OpNav with Autonomous bright spot pointing (requires version M6)

- Using DS1 FSW with Deep Impact Navigation additions for tracking, if available:
  - Collection and Downlink of an OpNav image with image compression
  - Autonomous OpNav with bright spot target tracking

Testbed:

- The DS1 Flight Software has been converted to run o a commercial Motorola PPC750 single board computer running a 233 MHz. The flight unit will run at 133MHz. To compensate, either the sysClock rate will be adjusted at the vxWorks operating system command level , or a suitable "fudge factor' for performance reduction will be calculated.
- Impacts of difference between the commercial and the flight Bridge-chip performance may be ignored since the flight bridge chip design is not yet confirmed
- The response of the flight hardware is simulated using the DS1 Sim Software, which has been converted to run on the PPC603 single board computer. The Flight and Sim hardware/software communicate through a pair of reflective memory boards plugged into their respective Compact-PCI backplanes and connected by high speed optical cable.

Test Results: I need to talk to you about how to adjust the performance test results to the processor speed that is where in the results to "fudge up/down" from the 233mhz effect to the 133 mhz actual flight proc speed. But I have to go now to a meeting so more later. Tal

Test #	Test Name	I-Cache Miss %			D-Cache Miss %			RAD6000* CPU %	PPC750 CPU %	PPC750 CPU IDLE %
1	post launch detumble	0.013	0.015	0.015	0.024	0.026	0.027	37.1	3.4	96.6
2	pre launch idle		0.009			0.017		14	1.2	98.8
3	post detumble idle		0.012			0.026		14.1	3.3	96.7
4	dseu and ips	0.016	0.016	0.016	0.049	0.049	0.05	72.1	4.4	95.6
5	dseu in scan mode	0.015	0.015	0.015	0.031	0.031	0.03		3.7	96.3
6	dseu in burst mode	0.03	0.03	0.03		0.036			4.3	95.7
7	bursting dseu and ips	0.016	0.016	0.017	0.064	0.065	0.066		5.0	95.0
11	acs in rcs control mode	0.015	0.014		0.027	0.027			3.5	96.5
12	Image Compression	0.039	0.044	0.043	1.14	1.168	1.168		60.2	39.8
13	Op Nav		0.104		0.734	0.777			67.0	33.0
14	Manuever Planing		0.018		0.034	0.035			4.9	95.1

- data from X2000 SFC Performance Analysis, Aug. 24, 2000, SFC Performance Analysis Team

These PPC750 CPU% values are slight lower than results prevously published. The Fault Protection task was activily running when the earlier results were taken. Fault Protection was not activily running during these tests. PPC750 CPU% was calculated by subtracting the tIdleTask time from 100%.

Analysis:

The MICAS compression algorythm requires between 5 and 10 seconds to compress the sample image from the actual DS1 Space Craft. During this time, compression uses nearly all of the available idle time. That is, the idle task does not get to run for a few seconds.

Image Compression

	ave.	agr.	burst
micas	95.605	100	0
nav	0	100	0
tIdleTask	0	100	0

	ave.	agr.	burst
micas	86.602	91.1	0.011
nav	8.848	100	0.022
tIdleTask	0.039	100	0

	ave.	agr.	burst
micas	87.266	91.3	0.021
nav	8.691	100	0.021
tIdleTask	0.02	100	0

The image compression measurements were take over 5 and 10 second intervals so as to minimize the amount of idle cycles recorded by perfmon and the cache miss counting software.

Though perfmon shows that on average, 39% of the cpu's time is available during image compression, the reality is that in few seconds it takes to compress an image, the processor is 100% subscribed. The data results above show that the idle task either did not run or did not run for a significant amount of time.

During Orbit Determination, most of the processing time is allocated to the Nav task. It too completes in less time than required for the RAD6K.

Orbit Determination

	ave.	agr.	burst
acs	2.128	3	0.011
nav	47.942	54.1	1.022
tIdleTask	45.871	100	0

	ave.	agr.	burst
acs	2.17	3	0.011
nav	71.853	79.2	1.033
tIdleTask	20.844	100	0

	ave.	agr.	burst
acs	2.157	2.9	0.011
nav	60.458	67.3	1.035
tIdleTask	32.653	100	0

	ave.	agr.	burst
acs	2.157	2.9	0.011
nav	60.458	67.3	1.035
tIdleTask	32.653	100	0

The Orbit Determination (OD) measurement were not recorded at specific intervals the way the Image Compression measurement were. By recording measurements at 5 to 30 intervals (increments of 5 seconds), we would have been able to characterize the duration of the OD activity. It appears that IdleTask uses 20% to 46% of the CPU time. Measurement over 5 seconds might reveal that OD is as intensive as image compression.

Conclusions:

Recommendations:

Attachments 2

Perfmon data

Instruction and Data Cache Miss data