SYNTHESIS AND CHARACTERIZATION OF NANOMETER-SCALE STRUCTURES FOR ELECTRONIC DEVICES

L.D. Bell, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, USA; E.A. Boer, M.L. Brongersma, M.L. Ostraat, R.C. Flagan, and H.A. Atwater, Caltech, Pasadena, CA, USA

NASA's needs for small, low-power microspacecraft has motivated development of micro- and nano-scale electronics that address NASA's unique needs. This talk will discuss synthesis and characterization developments at JPL and Caltech that address these needs. This includes several device concepts for future NASA missions to high-radiation environments such as Europa or other autonomous missions to the outer planets.

One class of devices are non-volatile memory arrays using silicon nanocrystals for bit storage. When combined with heterostructure tunnel barriers for write/erase operations, the potential exists for higly radiation-tolerant, low-power, fast memory devices. These structures can also be adapted for sensor and imager applications.

In an effort to understand device operation on the single-nanocrystal level, nanoscale characterization techniques such as conducting-tip atomic force microscopy (AFM) and ballistic-electron-emission microscopy (BEEM). BEEM was developed at JPL and uses scanning tunneling microscopy (STM) to probe subsurface electronic properties of thin films and interfaces such as interface barrier heights and electron scattering processes. BEEM probes at energies within several electron volts of the Fermi level, a range of direct interest to device operation. In addition, the extremely local electron injection by STM allows nanometer-scale resolution of device properties, of great interest as device dimensions continue to shrink. Unique capabilities of BEEM will be discussed.

This talk will provide an overview of materials characterization and device development leading to low-power, robust microelectronics for JPL's space applications.