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CMOS IMAGER WITH CHARGE-LEAKAGE COMPENSATED FRAME DIFFERENCE & SUM OUTPUT

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ABSTRACT

This paper presents a new technique for implementing a low-power CMOS imager with simultaneous on-chip computation of the difference and sum of two successive frames. Existing difference imagers are susceptible to errors due to collection (by the sense element and in-pixel storage node) of photo-generated charge that diffuses from the photo-active pixel area during integration of the second frame. This leakage cannot be removed in post-processing without frame rate reduction and additional frame memory penalties to readout and store the original frames. Our proof-of-concept imager uses a new unbalanced differential signal chain to provide 17 fold reduction in leakage error in the frame-difference output. The resulting residual error is < 1.5% of the actual frame difference value, over >100x illumination range. Error reduction is achieved without noticeable fixed-pattern-noise (FPN) or random noise in the image, preserving high image quality. Power dissipation in the 256x256 imager is measured to be only 18 mW.

1. INTRODUCTION

CMOS imagers have made rapid progress in recent years for multi-media and digital imaging applications [1]. Unlike charge coupled devices (CCDs), CMOS imagers are low-cost, consume ~100-1000x lower power, provide an integrated solution with simple digital interface and random access, and enable significant system miniaturization [2]. Thus, the ability of CMOS imaging technology to integrate timing, control and processing circuits on the focal plane enables system-on-a-chip solutions as exemplified by single-chip digital cameras [3,4].

Frame difference output is often used in multimedia applications for motion detection, motion-estimation, video compression, object segmentation through boundary detection, and surveillance systems. Computation of the frame-difference on-chip eliminates the need for external frame memory, saving power and enabling miniaturization. Furthermore, in cases where a small difference between two large signals is measured, on-chip difference computation will lead to lower errors with faster update rates due to the fact that frame rate is determined by the output rate and the digitization accuracy.

On-focal-plane frame difference computational imagers have been reported earlier using both photogate [5] and photodiode approaches [6]. In either case, the pixel features an in-pixel storage element that holds the signal from the previous frame, while the current frame is being exposed. Frame-difference is computed on a pixel-by-pixel basis by subtracting the current frame value from the stored previous frame value in the imager signal chain.

The main problem in either of these approaches is the corruption of the stored previous frame value during the current frame exposure by the collection (at the optically shielded sense and storage elements) of photo-generated electrons that diffuse from the photo-active pixel area. For an imager implemented in sub-micron CMOS technology, such leakage errors can easily be very large (and pixel implementation dependent), vastly degrading image contrast and introducing inaccuracies. Most importantly, since the signal mixing occurs at the pixel level, no post-processing techniques can correct for the errors without additional frame memory to store the original frames and proportional frame rate reduction to readout them out. Similarly, large pixels, extra transistor switches and/or double-poly storage capacitors may reduce the leakage, but only with unacceptable loss of fill factor, as well as spatial and signal resolution. Even then, further leakage compensation may be necessary.

In this paper, we report a 256x256 CMOS imager with simultaneous on-chip computation of leakage error-compensated frame-difference and frame-sum outputs. The error suppression works over a large range of illumination and illumination-difference, and does not increase imager FPN or random noise. It should be emphasized that leakage compensation also enables the original frame images to be determined from just the sum and difference images, if necessary. However, only the frame difference output is discussed in this paper, since the leakage compensation technique is the crucial element for both sum and difference outputs. Data on the frame sum, which is used as a normalization factor for the difference signal, will be included during the presentation.

2. IMAGER PIXEL & SIGNAL CHAIN

2.1 Imager Pixel

Figure 1 shows the schematic of the frame-difference pixel. The pixel consists of a photogate (PG) under which photoelectrons are accumulated during exposure, a transfer gate (TX) for transferring the electrons from PG to the sense node (SENSE), implemented as a reverse-biased p-n junction. The sense node also acts as an in-pixel frame memory. It is covered by metal to provide optical shielding. For resetting and reading out the pixel, the source-follower (M_{sf}), selection (M_{sel}), and reset (M_{rst}) FETs are used. In addition to the floating diffusion, the sense node consists of a FET connected as a capacitor (Cs) to increase the sense node capacitance to 150 fF. A large capacitance is used since this particular imager is designed for operation in high-flux conditions, requiring a large full-well capacity.

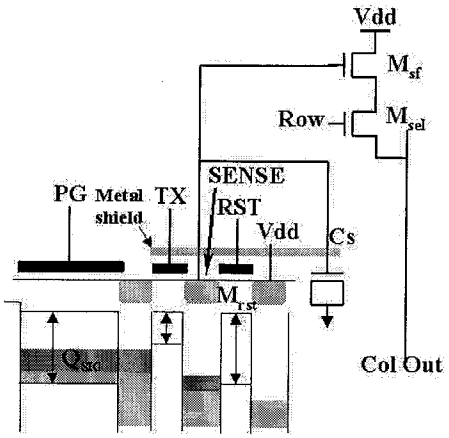

Figure 1. Schematic diagram of the frame-difference imager pixel circuit.

Under normal imaging mode [7], the sense node is sampled twice: once after it is reset by momentarily pulsing M_{rst} high, and a second time, after the photoelectrons are transferred into the sense node by momentarily pulsing PG low. By computing the difference between the samples, the imager provides a signal proportional to the photoelectrons collected in each pixel. Differential readout also ensures FPN suppression via elimination of offsets due to pixel-to-pixel threshold mismatches.

For frame-difference mode operation, the sense node is used for storing the previous frame signal. During readout, the previous frame signal stored on the sense node is sampled first, followed by a reset, and sampling of the current frame signal that was accumulated under PG. As a result, the sample-and-hold capacitors at the bottom of the column (see figure 2) store the signals from the two successive frames. Since the signal chain is differential, frame-difference is automatically computed.

2.2 Signal Chain

Figure 2 shows the schematic of the analog differential signal chain for reading out the pixel data. The column block consists of six capacitors and switches. For pixel readout, a row of pixels is selected, and the respective outputs are simultaneously sampled over the column bus on the column capacitors. For computing frame-difference, capacitors CS1 and CS2 are used, while the capacitor quad (CSS, CRH, CRS, and CSH) are used for generating the frame-sum. The switches shown in the schematic are implemented by FETs. To complete the readout of a row of pixels, the signals stored on the capacitors are scanned out by successively enabling the column select switch (COL). Once a particular column is selected, capacitors in that column are connected to the global switched capacitor amplifier, providing differential imager outputs. The global switched-capacitor amplifier consists of two differential opamps, buffered by unity gain drivers, and feedback capacitors (CIS1, CIS2, CI1, and CI2). The difference output can be written as:

$$V_{diff} = VoutS\,1 - VoutS\,2 = \alpha_1 \cdot V_{S1} - \alpha_2 \cdot V_{S2} + V_{off}$$
$$\alpha_1 = \frac{CS1}{CIS1}; \alpha_2 = \frac{CS2}{CIS2} \quad (1)$$

where $V_{s1}$and V_{s2} are the pixel signals from frame 1 and 2 respectively, and V_{off} is due to threshold mismatches.

The frame sum is generated using a similar signal chain, but using a different timing scheme. The pixel value for the previous frame (frame 1) is sampled on CSS by momentarily pulsing SHS1. Following this, the pixel is reset, and the reset level is sampled on CRS and CRH by momentarily pulsing SHR. Finally, the pixel is sampled again following the charge transfer, and the current frame value is stored on CSH by momentarily pulsing SHS2. As a result, the frame 1 signal is stored on the a.c.-coupled capacitor CSS, while the frame 2 signal is sampled on CSH with respect to ground. Hence, the sampling scheme ensures that the signal of the two frames are stored with opposite polarity. Since the signal chain is also differential, the global output produces the frame sum, instead of frame difference. The frame sum output can be written as:

$$V_{sum} = \beta_1 \cdot V_{S1} + \beta_2 \cdot V_{S2} + V_{off\,2}$$
$$\beta_1 = \frac{\hat{C}_1}{CI1}; \beta_2 = \frac{\hat{C}_2}{CI2}; \hat{C}_1 = \frac{CRH \cdot CSS}{CRH + CSS}; \hat{C}_2 = \frac{CRS \cdot CSH}{CRS + CSH}; \quad (2)$$

2.3 Charge leakage error correction

Assuming that amount of photo-generated charge collected by the sense element and storage capacitor is a constant fraction of the signal in the current frame, irrespective of the signal strength, and assuming that the imager transfer function is linear, the conventional frame difference output can be written as:

$$V_1 - V_2 = g \cdot (N_1 + \delta \cdot N_2 - N_2) \quad (3)$$

where N_i is the number of photons captured in frame-i, V_i is the corresponding voltage sampled, g is the photon conversion gain

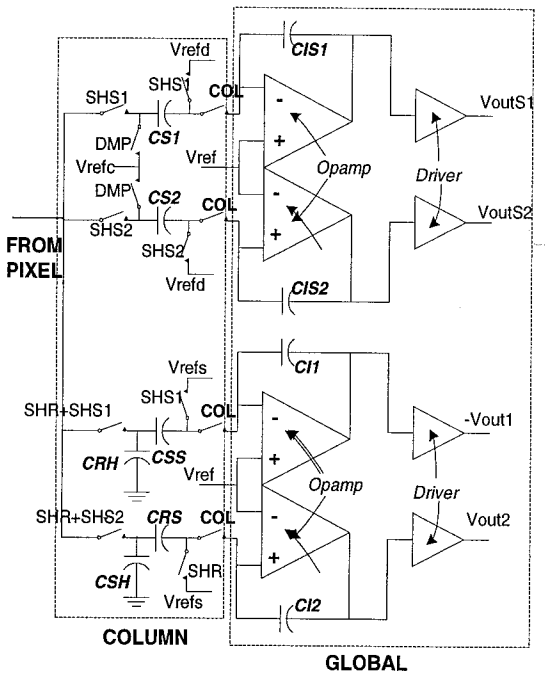

Figure 2. Schematic diagram of the frame-difference and frame-sum signal chain.

and δ is the fraction of leakage of current frame signal into the storage node. In this case, subscripts 1 and 2 denote the previous and current frames, respectively.

It is possible to eliminate the charge leakage error completely, if instead of computing true difference between the frame 1 and frame 2 signals, the differential signal chain is unbalanced appropriately. Unbalancing is done by applying different gains on the two branches of the differential signal chain. Since the gains are determined by capacitor ratios, as shown in equation 1, a programmable array of capacitors are implemented on chip to accurately cancel the errors. The chip output is thus given by:

$$V_{out} = V_1 - g_2 \cdot V_2 = g \cdot (N_1 - N_2 \cdot \{g_2 - \delta\}) \qquad (4)$$

By choosing $g_2 = 1 + \delta$, the leakage error can be made arbitrarily small. The chip is designed to provide 1% gain increments.

2.4 FPN suppression

In order to compensate for charge leakage errors, the two signal samples are weighted differently (i.e. different gains). However, unbalancing the signal chain can lead to increased FPN. On the other hand, pixel-to-pixel offset correction and flicker noise suppression depends upon exact difference computation, i.e., equal gain on both sides of the differential chain.

In order to provide both error compensation and FPN correction, a new sampling scheme is used. In this scheme, FPN is corrected first, and the unbalancing is carried out later. The pixel signals are sampled at the bottom of column on a pair of matched capacitors CS1 and CS2. As a result, the pixel source follower threshold voltage appears in the common mode, and it's effect is eliminated in the differential signal chain. By amplifying the offset-corrected charge, both error and FPN correction occurs simultaneously. This requires the programmable capacitor array to be placed on the feedback side in the global block. Specifically, variable gain is implemented by changing CIS1 and CIS2 only, and keeping the column capacitors fixed. This ensures that the area penalty for programmable capacitor implementation is insignificant.

3. TEST RESULTS

A 256x256 proof-of-concept imager was implemented in 0.5 μm single poly, triple metal CMOS technology made available through MOSIS. The photogate imager was implemented in a 15x15 μm pixel pitch. The switched-capacitor amplifier was implemented using a folded cascode opamp, with 150 MHz unity-gain bandwidth. The total chip area is 5.6 mm x 5.8 mm, of which the imager area is 3.85 mm x 3.85 mm. Figure 3 shows the micrograph of the chip.

Figure 4 shows the leakage-compensated frame-difference output of the imager as a function of the actual difference of the frame 1 and frame 2 signals. Excellent charge leakage error suppression is indicated by the linear difference output over a 100x range of intensity differences. Figure 5 shows the relative error between the ideal output and the frame difference output. The uncorrected error was found to be relatively independent of signal strength. After correction, the residual error is both small (< 1.5%) and constant across the entire signal range, indicating a 17x reduction

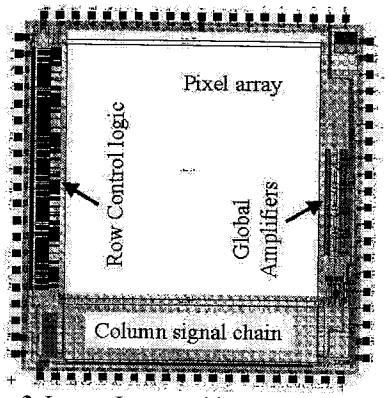

Figure 3. Imager Layout with component blocks.

in error. Since red photons are absorbed deeper in the silicon substrate, red LED was used in these measurements as a worst-case test. Deeper absorption of photons causes charge collection primarily by diffusion, leading to higher leakage errors.

"White" light tests were carried by using grey-scale bar-patterns of variable reflectivity ranging from 90% to <0.5 %. Images were captured at different several incident lamp intensities to cover the imager dynamic range. Figure 6a shows the direct mode image of the target pattern at a mean signal of 260 mV, figure 6b is captured in difference mode under same illumination and without any error correction, while figure 6c is captured in the difference mode with error correction. Ideally, the images in figure 6b and 6c should be uniformly grey. However, significant amount of residual pattern can be seen in figure 6b, due to charge leakage of current frame into the storage node. The image in figure 6b is indicates that without error correction, frame-difference imaging is not very practical. Figure 6c shows that once the error correction is applied, the residual pattern is practically invisible, except in regions of the largest intensity changes due to pixel-to-pixel cross-talk which has not been suppressed. Figures 5 and 6 indicate that charge leakage error has been reduced to an insignificant amount over the entire illumination range. Dark, flat field images showed no noticeable column FPN. Imager performance is summarized in table 1.

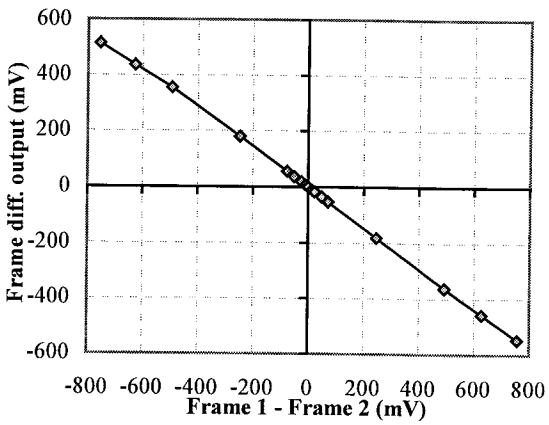

Figure 4. Frame-difference output as a function of the actual frame difference intensities.

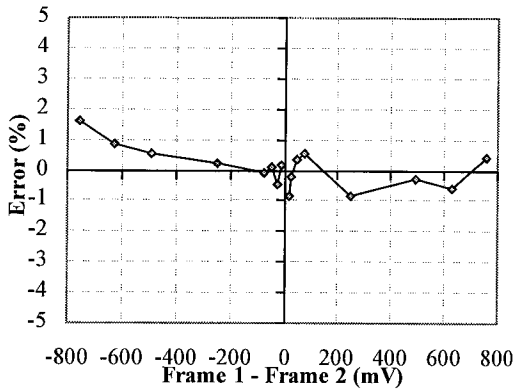

Figure 5. Error in the difference output normalized to the actual difference in frame intensities under flat-field, red LED illumination.

4. SUMMARY

A new technique for on-chip frame-difference imaging circuit is presented. The imager provides both direct and difference mode output, with errors due to charge leakage from one frame to another via substrate diffusion suppressed to invisible levels. Error compensation is achieved by providing different gains in the two branches of the differential signal chain. A single gain setting is capable of reducing charge leakage error to less than 1.5% over the entire range of illumination. The error correction does not affect the imager FPN or random noise. The 18 mW power dissipation, makes it greatly attractive for portable applications.

5. ACKNOWLEDGMENT

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Table 1. Performance Characteristics

Characteristics	Values	Comments
Format	256x256	
Pixel	15 μm x 15 μm	Photogate
CMOS tech.	0.5 μm 1P3M	
Responsivity	1.9 μV/e^-	Broad-band ill.
Full-well	500,000 e^-	
Uncorrected error	25%	@ 650 nm
Corrected residue	< 1.5%	> 17x reduction
Power dissipation	18 mW	@ 3.3V

6. REFERENCES

[1] E. Fossum, "CMOS image sensors: electronic camera-on-a-chip," *IEEE Trans. on Electron Devices*, Vol. ED-44, p 1689-1698, 1997.

[2] B. Pain, et al., "One chip digital camera with extended low-light detection capability," *Proc. 2000 13th. VLSI Design Conference*, p 342-349, 2000.

[3] M. Loinaz, et al. "A 200 mW 3.3V CMOS color camera IC producing 352x288 24b video at 30 Frames/s", *Tech. Dig. IEEE International Solid-State Circuits Conference (ISSCC)*, Vol. 35, p 168-169, 1998.

[4] S. Smith, et al., "A single chip 306x244-pixel CMOS NTSC video camera," Tech. Digest, IEEE ISSCC, Vol. 41 (FA11.2), pp.170-171, 1998.

[5] S. Ma and L. Chen, "A single chip CMOS APS camera with direct frame difference output", *IEEE J. of Solid-State Circuits*, Vol. SC-34, p 1415-1418, 1999.

[6] A. Dickinson, et al., "A 256x256 CMOS active pixel image sensor with motion detection", *Tech. Dig. IEEE ISSCC*, Vol. 38, p 226-227, 1995.

[7] S. Mendis, et al., "CMOS active pixel image sensors for highly integrated imaging systems," *IEEE J. of Solid-state Circuits*, vol. SC-32, pp. 187-198, 1997.

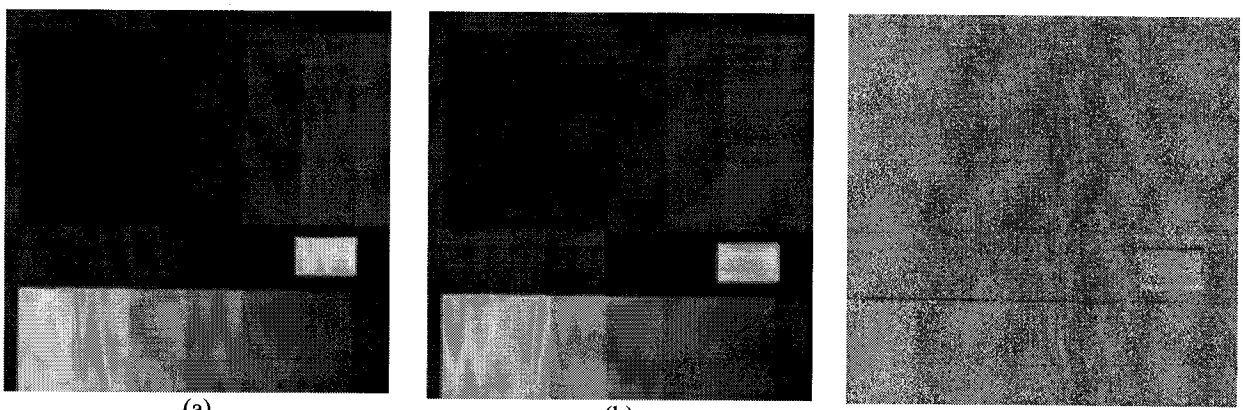

Figure 6. **(a)** Direct mode image of gray scale bar-pattern under "white light" illumination, **(b)** difference mode image without error correction, and **(c)** difference mode image after error correction.