Effect of Thermal Cycling Ramp Rate on CSP Assembly Reliability

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Abstract

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of team members representing government agencies and private companies, recently joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. The experience of the Consortium in building more than 150 test vehicle assemblies, single- and double-sided multilayer PWBs, and the environmental test results has now been published as a chip scale package *CSP)guidelines document and distributed by Interconnection Technology Research Institute (ITRI).

The Consortium assembled fifteen different packages from 48 to 784 I/Os and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring board (PWB). Another test vehicle was designed and assembled by a team member using their internal resources and is identified as TV-H. The TV-H assemblies were subjected to numerous thermal cycling conditions including -55°C to 125°C with two acceleration rates, one thermal cycle with 2° to 5°C/min and the other near thermal shock. Cycles-to-failure (CTF) test results to 1,000 cycles and 400 cycles under these conditions were presented for fine pitch ball grid arrays (FPBGAs), CSPs, and wafer level CSPs (WLCSPs) were presented. Decrease in CTFs due to accelerations and die size increase for different I/O FPBGAs with 0.8 mm pitch were compared and presented.

Introduction

Chip scale packages are now widely used for many electronic applications including portable and telecommunication products. The CSP definition has evolved as the technology has matured and refer to those packages with a pitch of 0.8 mm and lower. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of microvia printed wiring board (PWB) which is costly and they may perform poorly when they are assembled onto boards. A test vehicle (TV-1) with eleven package types and pitches was built and tested by the JPL MicrotypeBGA Consortium during 1997 to 1999. Lessons learned by the team were published as a guidelines document for industry use[1]. Recent information on the effects of underfill was present last year [2].

The finer pitch CSP packages which recently become available were included in the next test vehicle of the JPL CSP Consortium[3]. The Consortium team jointly concentrated their efforts on building the second test vehicle (TV-2) with fifteen (15) packages of low to high I/O counts (48 to 784) and pitches of 0.5 mm to 1.27 mm. In addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effects of PWB build and manufacturing variables.

One test vehicle, herein refer to TV-H, was designed and assembled by Hughes Network System using their internal resources. This paper presents the thermal cycling test results to 1,000 cycles (-55 to 125°C) for a variety of CSPs used on the TV-H assembly. CTF test results will be compared to those performed under this temperature range, but with a more sever near thermal shock condition to 400 cycles.

CSP TEST MATRIX

Test Vehicle Package I/O /PWB

The TV-H had eight packages ranging from 48 to 280 I/Os with pitches of 0.8 mm as shown in Figure 1. The PWB had four layers with the two resin coated copper (RCC) layers and an FR-4 core (1+2+1) having a total thickness of 0.43 mm. Microvia technology was used. The pad had a 0.1 mm (4 mil) microvia hole at the center of pad. A non-solder-mask-design (NSMD) pad with a diameter of 0.3 mm and 0.05 mm clearance was used. The surface finish of the PWB was Ni/Au immersion with about 2-8 micro inch of gold over 100-200 micro inch Ni. No clean solder paste for assembly was applied with a 5 mm thickness laser cut stencil. The test vehicle was 11.9 cm by 4.6 cm (4.75″ by 1.85″) with one connector attached for continuous thermal cycling monitoring.

Test Vehicle Features/Daisy Chain Patterns

Figure 1 shows a full populated test vehicle (TV-H) with two sites for the 280 I/O fine pitch ball grid array (U4 and U2 sites). All packages were daisy-chained, and they were divided into several internal chain patterns. The daisy chain pattern on the PWB completes the chain loop into the package through solder joints. Several probing pads connected to daisy chain loops were added for failure site diagnostic testing. A representative package and PWB daisy chains is shown at the bottom of Figures 2. All sites were populated for the thermal cycling assembly testing. All packages were prebaked at 125°C for 2 ½ hours prior to assembly.

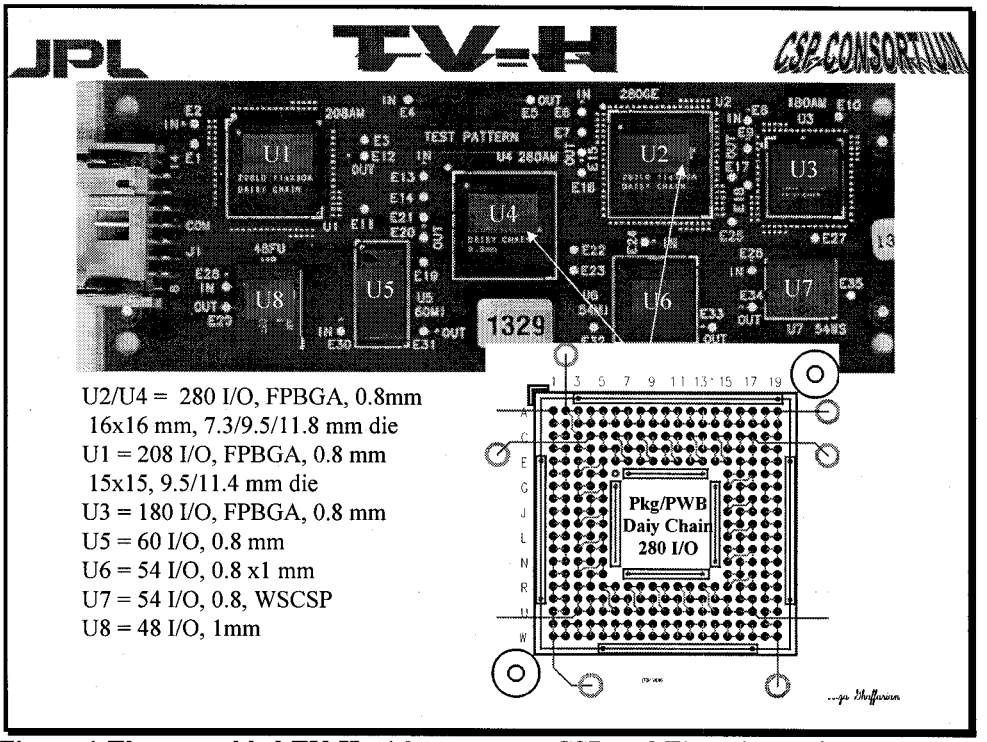

Figure 1 The assembled TV-H with numerous CSP and Fine pitch BGA packages. The package/PWB daisy chain for the 280 I/O FPBGA is shown on the bottom right.

TEST CONDITIONS

Thermal Cycling test

Thermal cycling was performed in the range of –55°C to 125°C under two different conditions. Chamber setting and thermal couple readings for conditions A and B are shown in Figure 2 and 3, respectively. For condition A, the heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time duration at the minimum temperature. Each cycle lasted 159 minutes.

The near thermal shock cycle, condition B, had the same temperature range performed in a chamber with three regions of hot, ambient, and cold. Heating and cooling rates were nonlinear and varied averaging between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

Monitoring

The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 7.8, were used as guidelines to interpret electrical interruptions. In general, it is expected that once the first interruption is observed, there will be a large number of additional interruptions within the 10% of the cycle life. This was not the case especially for the wafer level package assemblies. Failures detected by continuous monitoring were verified manually at room temperature after weekly removal from the chamber.

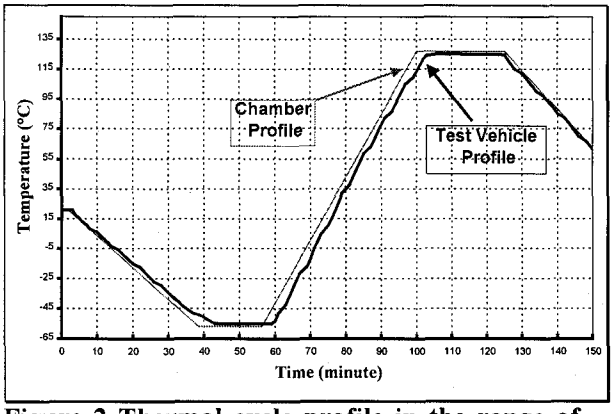

Figure 2 Thermal cycle profile in the range of –55°C to 125°C, condition A, 159 minutes/cycle

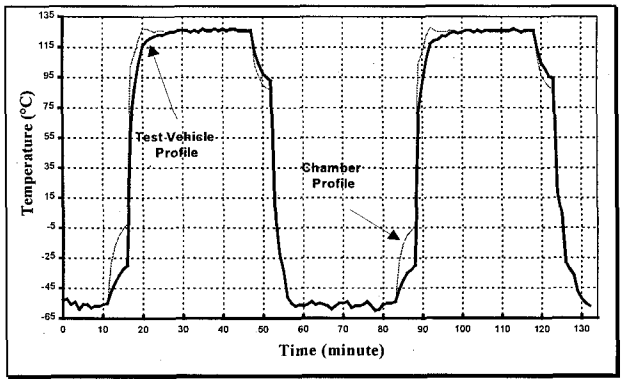

Figure 3 Near thermal shock profile in the range of –55°C to 125°C, condition B, 68 minutes/cycle

THERMAL CYCLING RESULTS

Failure Characteristics of Wafer Level CSPs

Figure 4 shows cycles to first failures for three different wafer level chip scale package (WLCSP) technology, I/O counts, and pitches. To generate plots, the CTFs were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$.

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull cumulative failure distribution was used to fit CTF data. The equation is

$$F(N) = 1- \exp (-(N/No)^m)$$

where

F(N) is the cumulative failure distribution function

N is the number of thermal cycles

No is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63.2% failure occurrence.

m is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by 1.2/CV; that is, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line will define the Weibull shape parameter. The cycles to failure data in log-log were fitted to a straight line and the two Weibull parameters were calculated.

Weibull parameters for cycles to failure were also generated and plotted shown as continuous graphs in Figure 4. Weibull parameters for each assembly failure is also given. The m value ranged from 7 to 13, with the lowest value projected for the WLCSP based an about 50% failures to 1,000 cycles.

The lowest CTFs were in the range of 276 to 451 cycles with No and m values of 383 and 8.5, respectively, for the 60 I/O WLCP with a 0.8 mm pitch. The solder joint failures for this package were at the package interface, verified by cross-sectioning and destructive testing after dye-penetrant. This package has already been modified by manufacturer showing improved reliability and this newer version is currently being evaluated by Consortium. The CTFs for the 54 I/O package with 0.8 by 1 mm pitches were in the range of 543 to 778 cycles with No and m values of 660 and 13, respectively. The 48 I/O package with a 1 mm pitch showed the highest CTFs, even though the first failure was at 638 cycles. The seven out of 17 other packages failed to 1,000 cycles in the range of 778 to 959 cycles with estimated Weibull parameters of No and m values of 1,030 and 7.

Effects of Die Size and I/O Counts

CTFs for the FPBGA package with different I/Os and die sizes are shown in Figure 5. For this package technology, the relative die size had the most significant effects on CTFs. The 208 I/O package with an 11.4 mm die size in a 15 mm package showed CTFs in the range of 176 to 573 cycles whereas the CTFs were in much higher range of 417 to 799 cycles for a 9.5 mm die size. The 280 I/O package with an 11.8 mm die in 16 mm packages failed in the range of 303 to 824 cycles. CTF data for assemblies at the center of PWB (U4 site) and the edge were also distinguished by plotting a square and triangle. Even though most of U4 packages failed at higher cycles, it is not clear if this is due to location of the package on the PWB or is a manufacturing anomaly.

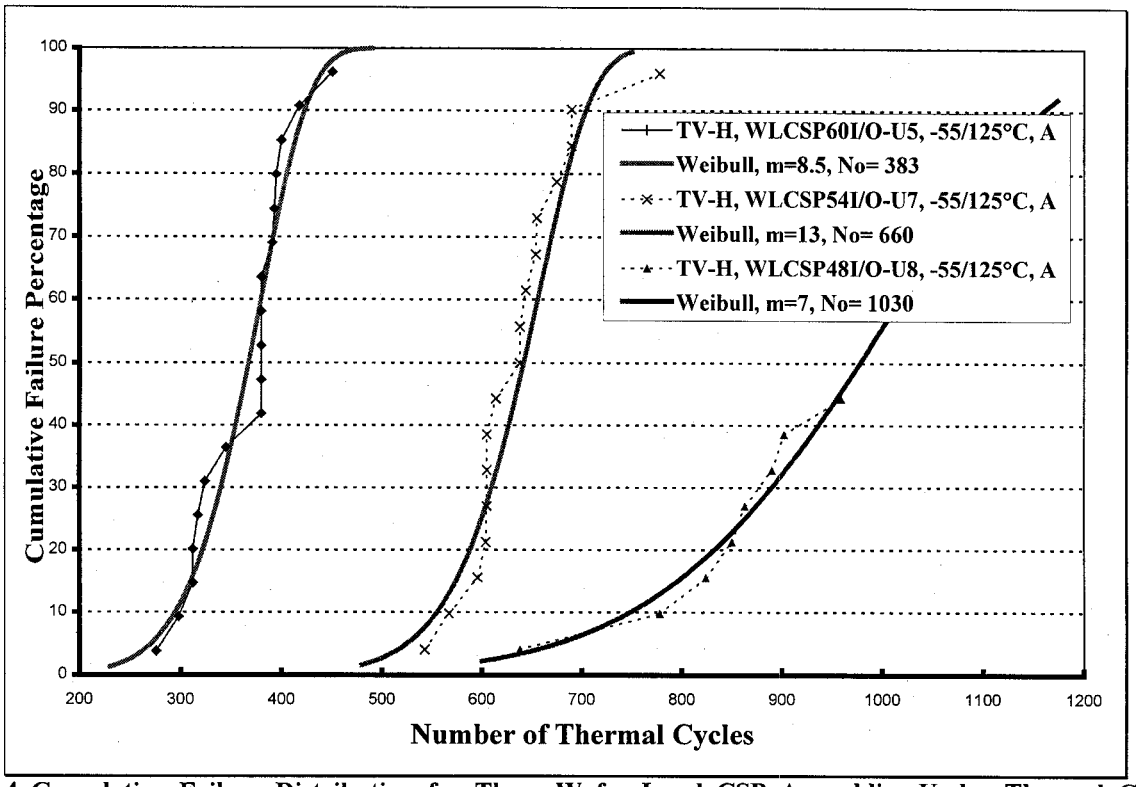

Figure 4 Cumulative Failure Distribution for Three Wafer Level CSP Assemblies Under Thermal Cycle A Condition (-55° C to 125°C)

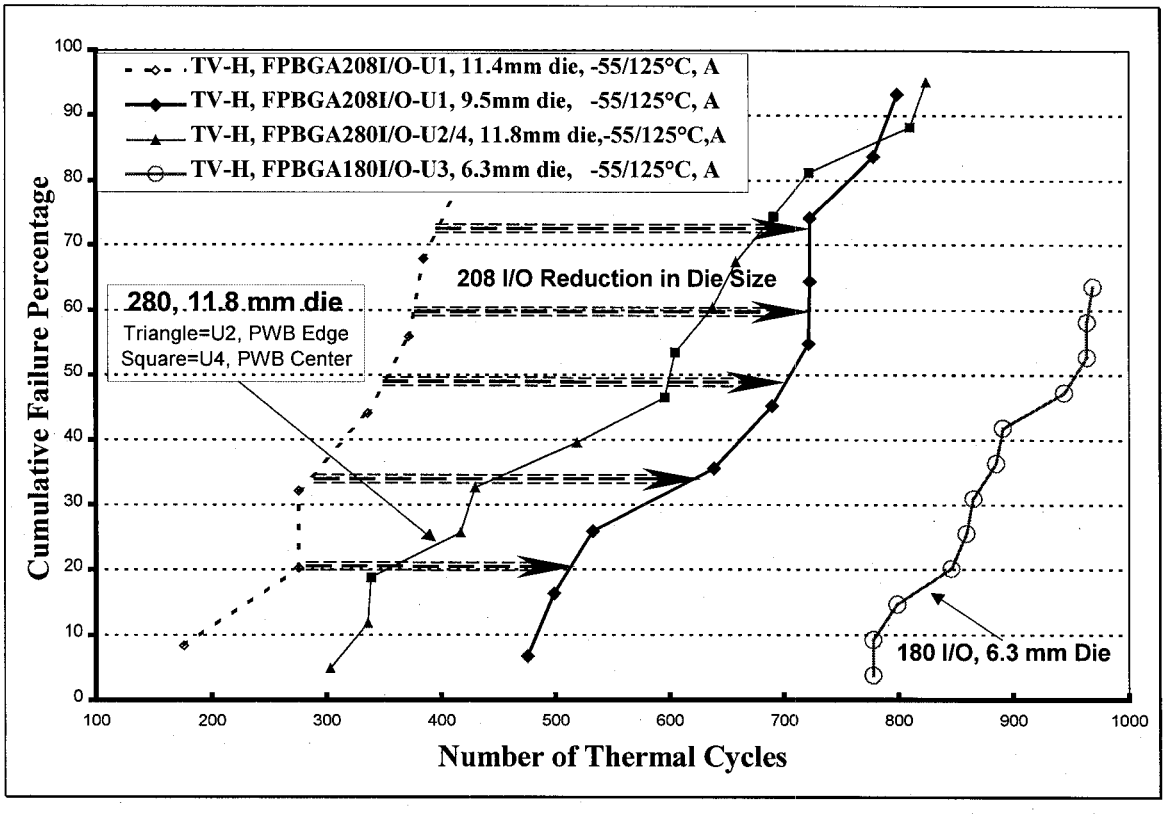

Figure 5 Cumulative Failure Distribution for an FPBGA Technology with three different I/Os and Die Sizes Under Thermal Cycle A Condition (-55 ° to 125°C)

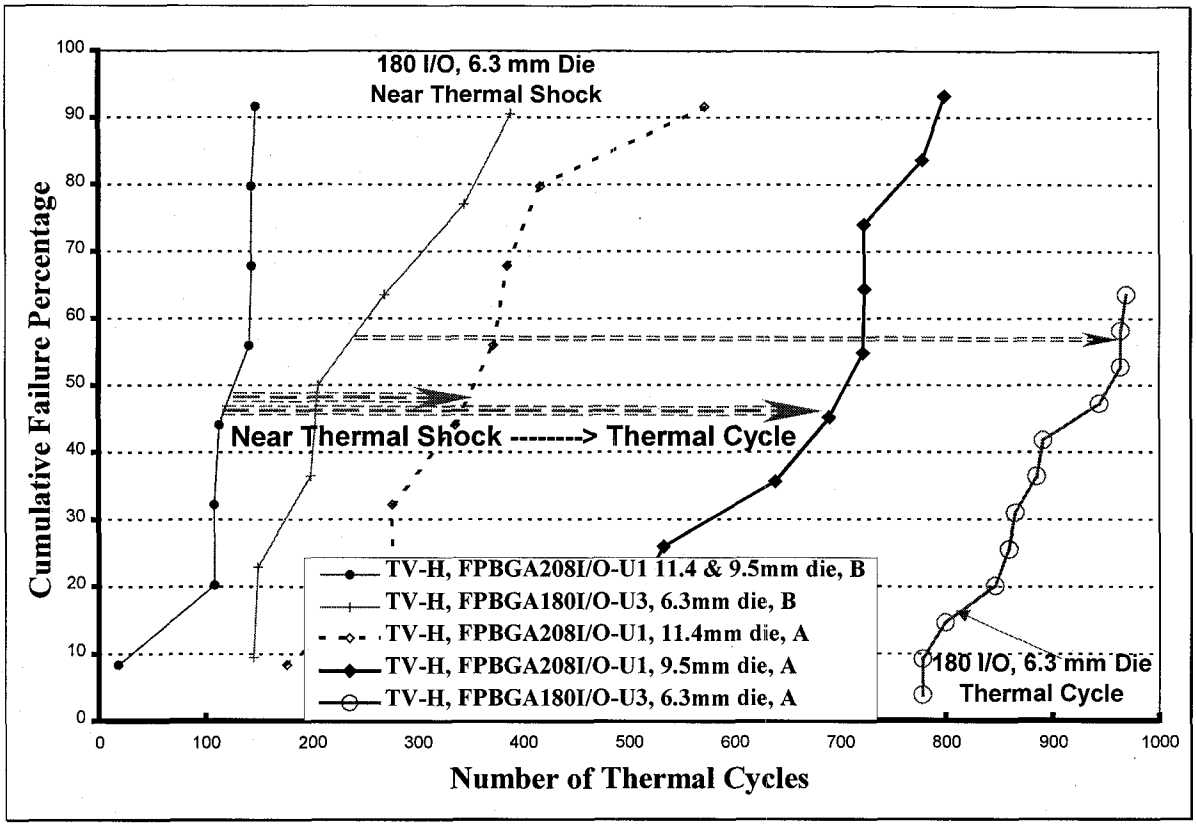

Figure 6 Cumulative Failure Distribution for the Same FPBGA Package and I/Os Under the Same Thermal Cycling Range (-55 ° to 125°C) But Two Different Rates

The 180 I/O package with a 6.3 mm die in a 12 mm package failed at much higher failure cycles, six assemblies showed no failures to 1,000 cycles. The CTFs for those failed were in the range of 778 to 969 cycles.

Effects of Thermal Cycle Ramp Rate

Figure 6 shows the test results for the 180 I/O FPBGA with a die size of 6.3 mm and the 208 I/O with the die sizes of 11.4 and 9.5 under two the same thermal cycling range (-55°C/125°C), but two different ramp rates, A and B conditions. It is apparent that the near thermal shock cycle is sever and CTFs for the 208 I/O package with 11.4 and 9.5 mm dies were within the data scatter. This is not the case for the results under thermal cycle A condition where the effect of die size is clearly demonstrated. The CTFs for the 180 I/O package with a 6.3mm die size are also differ significantly under two cycling conditions. The CTFs were in the range of 145 to 389 cycles for the near thermal shock whereas the first failure was observed at 778 cycles for the thermal cycle condition.

DISCUSSION

New applications of advanced electronics packaging, including CSPs, brought about new package technology including materials and processes as well environmental requirements not seen in their previous generation. Rapid insertion of electronics packaging necessitates faster qualification implementation and therefore development of accelerated test methods.

Electronics assembly failures occurs by the on/off cycles that introduce failure of solder joints due to thermal mismatch of package and PWB. Solder joint integrity is critical since the joints carry both electrical and mechanical load. As also discussed in this paper, failure of solder joints due to CTE mismatch are commonly characterized using a dummy package daisy chained through solder joints and the PWB by monitoring their failure under temperature cycling. A large number of thermal cycling/shock conditions differing in minimum, maximum, and heating/cooling rates have been used by industry.

A recently released specification, IPC 9701- Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, is aimed to standardize environmental testing by defining the key variables and their limitations. Use of power cycling, i.e. heating solder locally by imbedding resistance inside of the package, is now are also being considered as an alternative since it

provides higher reliability results much needed for miniature packages.

Accelerated thermal cycling with a large temperature swing can be used for environmental screening test and often has been considered as qualification requirement for harsh environmental applications. There are many concerns, however, when such accelerations are performed especially for electronics packages with no environmental testing heritage. These concerns include: the effects of cold and hot temperatures in a cycle range, time and temperature at dwell, maximum temperature above 100°C for eutectic solder, and the effects of heating/cooling rates.

In this investigation, in addition to providing CTFs for several FPBGAs, CSPs, and wafer level CSPs, the effects of heating/cooling rates were also clearly demonstrated. Assemblies cycled under a near thermal shock condition showed much lower number of CTFs similarly to those previously demonstrated for their BGA counterparts. However, the effect of die size that was clearly demonstrate by an extreme thermal cycling.e range (-55°C to 125°C), but a moderate ramp rates may not be distinguishable when the ramp rates also become nearly extreme. If this conclusion further verified, it may also implies that acceleration factors generally employed to project the life for the intended applications, may also vary depending on the types of technology.

CONCLUSIONS

These conclusions are based on the results limited to assembly failures to 1,000 thermal and 400 near shock cycles in the range of -55°C to 125°C. Addition thermal and mechanical cycling data with their failure analyses are being gathered to further define the effects of various parameters on assembly reliability.

- Cycles-to-failures for the fine pitch ball grid arrays (FPBGAs) with 0.8 mm pitch were in the range of 300 to 800 and 100 to 200 cycles for thermal cycle and near thermal shock conditions, respectively. These are significantly lower than their 1.27 mm pitch BGA counterparts with CTFs of more than 1,000 cycles for the near thermal shock condition [1].
- CTFs decreased as package die size increased under thermal cycle condition. The effect of die size decrease from 11.4 mm to 9.5 mm could not be clearly identified by the near thermal shock condition. Further tests and failure analyses are being performed to verify the latter test results.
- The 208 I/O FPBGA package with the largest relative die size to package dimension (11.4 mm die in 15x15 mm package) showed the lowest CTFs and the 180 I/O package with the lowest relative die size to package (6.3 mm die in 12x12 mm package) showed the highest CTFs under thermal cycle condition.

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ACKNOWLEDGEMENTS

The portion of research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Special thanks to A. Arreola at JPL and David Bowen and Kevin Griffith at Boeing for monitoring the environmental testing. The JPL author would like to acknowledge the in-kind contributions and cooperative efforts of the JPL CSP Consortium. Special thanks to M., Lam, D., Strudler, S., Umdekar, Hughes Network Systems (HNS), and package suppliers and other team members who have made contributions to the progress of this program.