A Library of Rad Hard Mixed-Voltage/Mixed-Signal Building Blocks for Integration of Avionics Systems for Deep Space., ,M. M. Mojarradi[1], B. Blaes[1], E. A. Kolawa[1],B.J. Blalock[2],H. W. Li[3], K. Buck[3] and Dave Houge[4], [1]Jet Propulsion Laboratory, 4800 Oak Grove, Pasadena, CA 91109,[2]Mississippi State University, Dept. of Electrical & Computer Engr., Box 9571, Mississippi State, MS 39762, [3]University of Idaho, Moscow, ID 83843, [4]Boeing Corporation Seattle WA.

Introduction: To build the sensor intensive system-on-a-chip for the next generation spacecrafts for deep space, Center for Integration of Space Microsystems at JPL (CISM) takes advantage of the lower power rating and inherent radiation resistance of Silicon on Insulator technology (SOI). We are developing a suite of mixed-voltage and mixed-signal building blocks in Honeywell's SOI process that can enable the rapid integration of the next generation avionics systems with lower power rating, higher reliability, longer life and enhanced radiation tolerance for spacecrafts such as the Europa Orbiter and Europa Lander.

The mixed-voltage building blocks are predominantly for design of adaptive power management systems. Their design centers around an LDMOS structure that is being developed by Honeywell, Boeing Corp, and the University of Idaho. The mixed-signal building blocks are designed to meet the low power, extreme radiation requirement of deep space applications. These building blocks are predominantly used to interface analog sensors to the digital CPU of the next generation avionics system on a chip.

LDMOS in Honeywell SOI Processes: Traditional SOI CMOS technologies only support low voltage transistors in their suite of devices. However, it is possible to create lateral high voltage transistors in the SOI CMOS process without any changes to the fabrication sequence. Fig. 1 shows a cross section of such a high voltage MOSFET in an SOI CMOS process. A drift region made of lightly doped material (already exists in the SOI CMOS process) is added to the drain terminal to sustain the high voltage. These transistors have several limitations. For on-chip integration of high voltage functions in radiation hard SOI CMOS technologies we have had to develop new non-traditional circuit topologies.

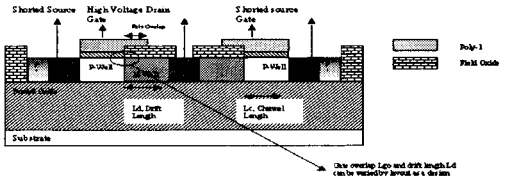

Fig. 1: A high voltage MOSFETs in SOI CMOS

A Space Rated Mixed-Voltage Mixed-Signal Library: Fig. 2 shows the block diagram for the next generation avionics system-on-a-chip for deep space applications. This SOAC requires a complex library of mixed-signal functions. Table-1 lists the typical cells that are part of this library. There are several limitations in the performance of SOI-based mixed-signal building blocks. For example, the input offset voltage in a single stage differential amplifier is much higher

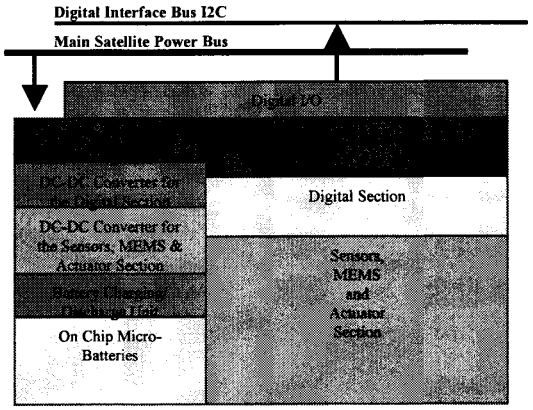

Fig. 2: Next Generation Avionic SOAC.

in the SOI CMOS process due to mismatch of the input transistors. Current mirror circuits also suffer from transistor mismatch, in addition to thermal gradient induced offset. Finally, a traditionally designed bandgap reference generator primitive develops a large output offset due to mismatch between the bipolar elements. For certain applications, however, the unique isolation features of the SOI CMOS process allows circuits that are normally available only in discrete form and not easily realizable in bulk CMOS to be fabricated.

Table-1: Library integrated building blocks .

Cell Type	
Low Voltage	Precision References
Low Voltage	Analog to Digital Converter
Low Voltage	Digital to Analog Converter
Low Voltage	High-Speed Differential Amp
Low Voltage	Comparators
Low Voltage	Operational Amplifiers
Low Voltage	Analog Buffers
Low Voltage	Phase/Frequency Detectors
High Voltage	Rectifiers
High Voltage	Switching Inductor Drivers
High Voltage	Voltage Regulator
High Voltage	Analog Level Translator
High Voltage	Zero Crossing Detector
High Voltage	High Side Gate Pre-Driver

References:

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