Extreme Temperature (-170C to +125C) Electronics for Nanorover Operation

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Problem Statement

- Goal: make electronics that control mobility operation and optical bench science gathering of in a 1.3kg, 1660 cm^3 nanorover.
- Nanorover will operate on either mars or a small body asteroid.

Nanospacecraft Trends, Implications, Constraints and Conclusions

Summary of Constraints for nano S/C

- So small volume implies:
  - Need for miniaturized electronics
  - Low power availability
  - Not a lot of excess self heat generated
  - Wider temperature swings of parts of the S/C due to lower thermal mass
  - S/C temperature essentially determined by environment and external interconnects

Electronics Miniaturization Solutions

- Miniaturization of electronics circuits gives small circuits that run on very little power.
  - This is a win for solving the power availability problem.
  - Less power implies less excess power for heat.
  - Generates a desire not to diminish the volume, mass and power gains of miniature electronics by adding heaters.

Problem of Keeping Things Warm

- Wires
  - On sojourner wire length was increased, diameter was decrease, and circuitous path use to reduce heat loss between internal electronics and external actuators and sensors
  - On the muses-CN rover, number of wires connecting to top solar panel was limited to about 6 wires which were made out of tungsten to reduce heat transfer

Enabling Technology: Cold Electronics

- Since nano-sciencecraft will primarily track the external temperature, being able to operate cold would allow existing components and packaging to be used.
- Cost benefits from being able to use existing flight and commercial parts.

A Possible Alternative for Keeping Heat in

- Put electronics in a thermos
- Again wires are a path for heat transfer
- Possible use of mostly /all optical interfaces
- If any electronics are going to be outside of thermos they still need ability to work cold

Rover Electronics Constraints

- Low mass: 180 grams.
- Low power: 2.56 watts from solar cells.
- Low volume: 226.8 cm^3.
  - (12 cm x 12.6 cm x 1.7 cm).
- Large temperature range:
  - -180C to +125C survival range.
  - -170C to +110C operation range.
- Mass and volume drives the packaging to chip on board.

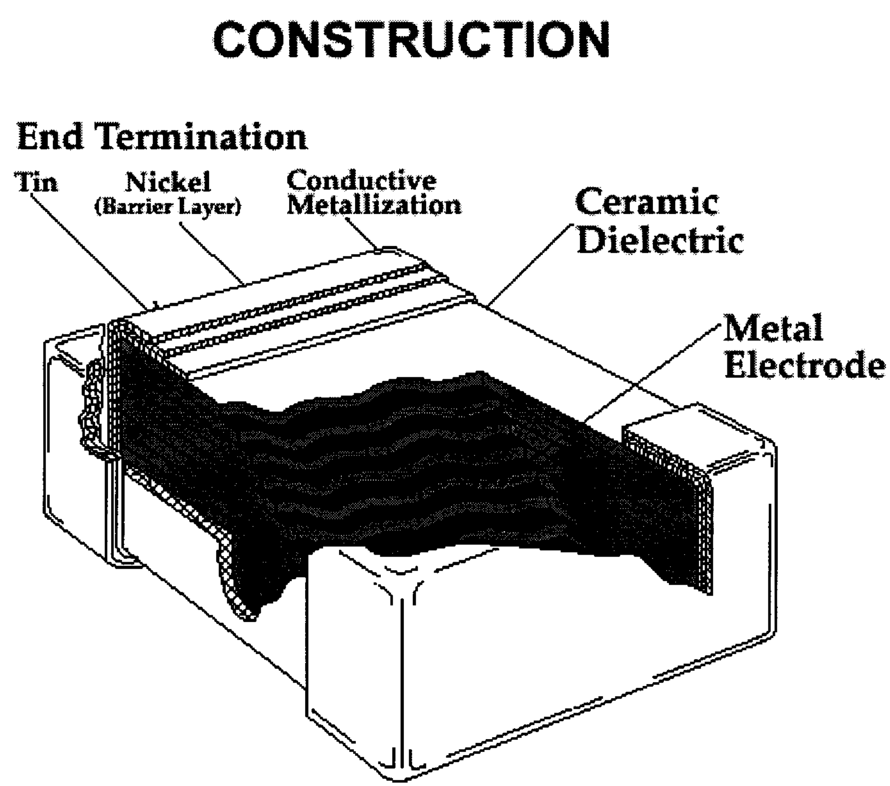
Passive Electronics Component Operation at Extreme Cold Temperatures (-170C)

Passive Parts – Resistors, Capacitors, Inductors

- Resistors work great cold
  - Thermal noise goes down (surprise!!)
  - Seem to follow their temperature coefficients into the cold temperature regime, does not vary significantly
- Capacitors work cold but vary
  - Capacitance does vary as a function of temperature
  - Choice of capacitor is important
- Inductors work cold but vary
  - Inductance does vary with temperature due to changes in core permeability

Multi-layered Capacitor (MLC) Body

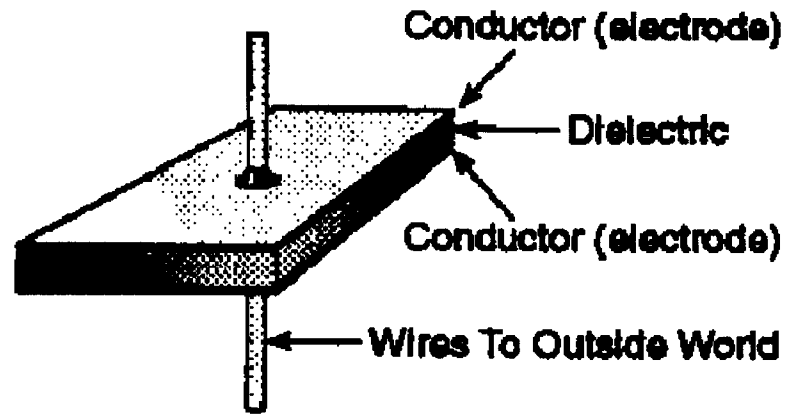
- Parallel plate capacitor folded in an accordion
- Each layer is considered a small parallel plate capacitor in parallel with the next layer



Capacitors Physics

Capacitance

$$C = \frac{\kappa' N A}{d}$$



The Parallel - Plate Capacitor

$\kappa' = e_R/\varepsilon_0$ is the ratio of the permittivities of dielectric material e_R and a vacuum e_0

N is the number of layers within a multi-layer capacitor

A is the area $A = lw$, where l is the length and w is width

d is the distance between each electrode plate

BP Capacitors

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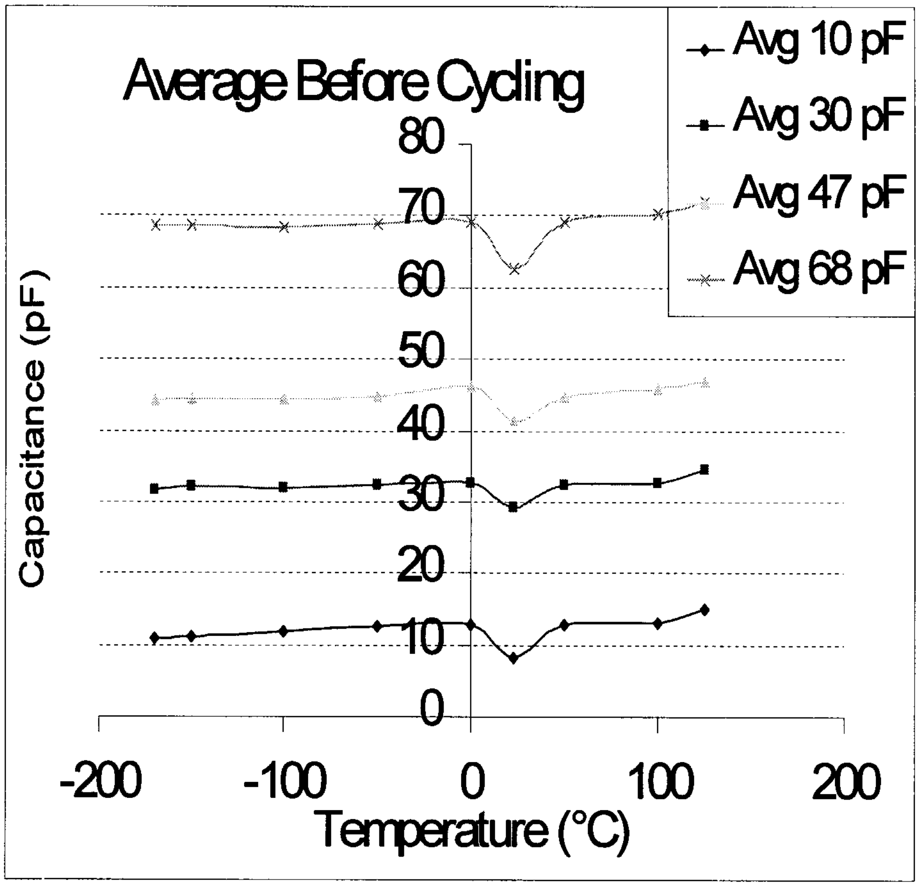

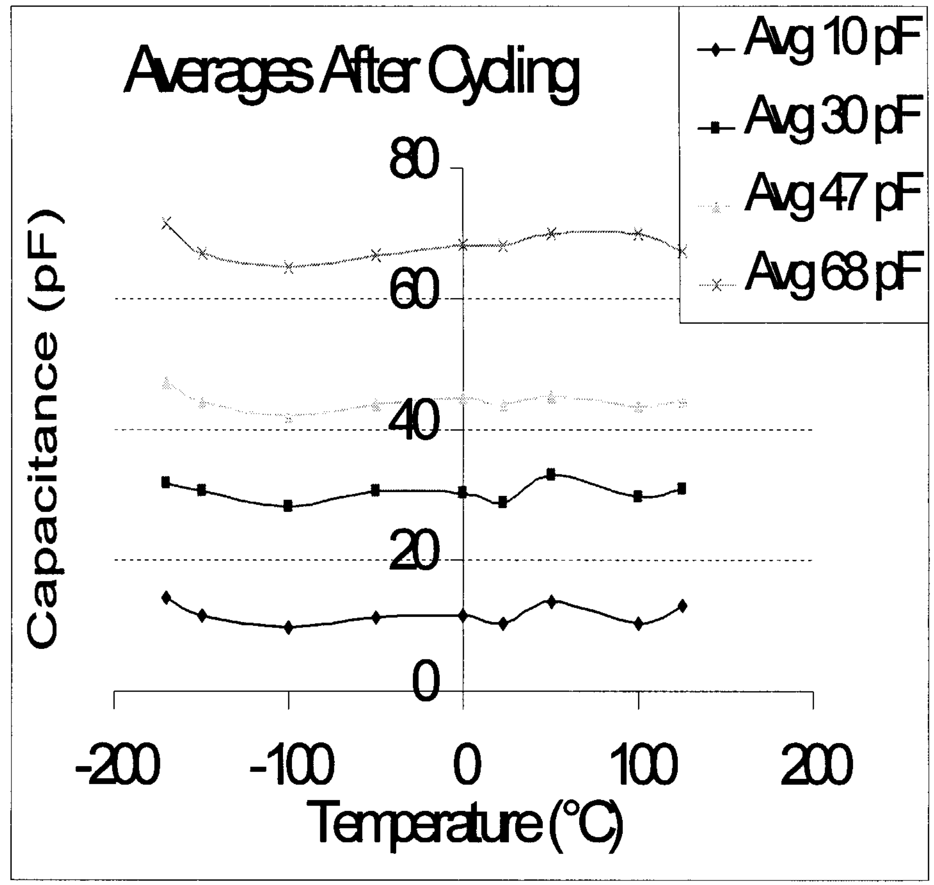

BX Capacitors

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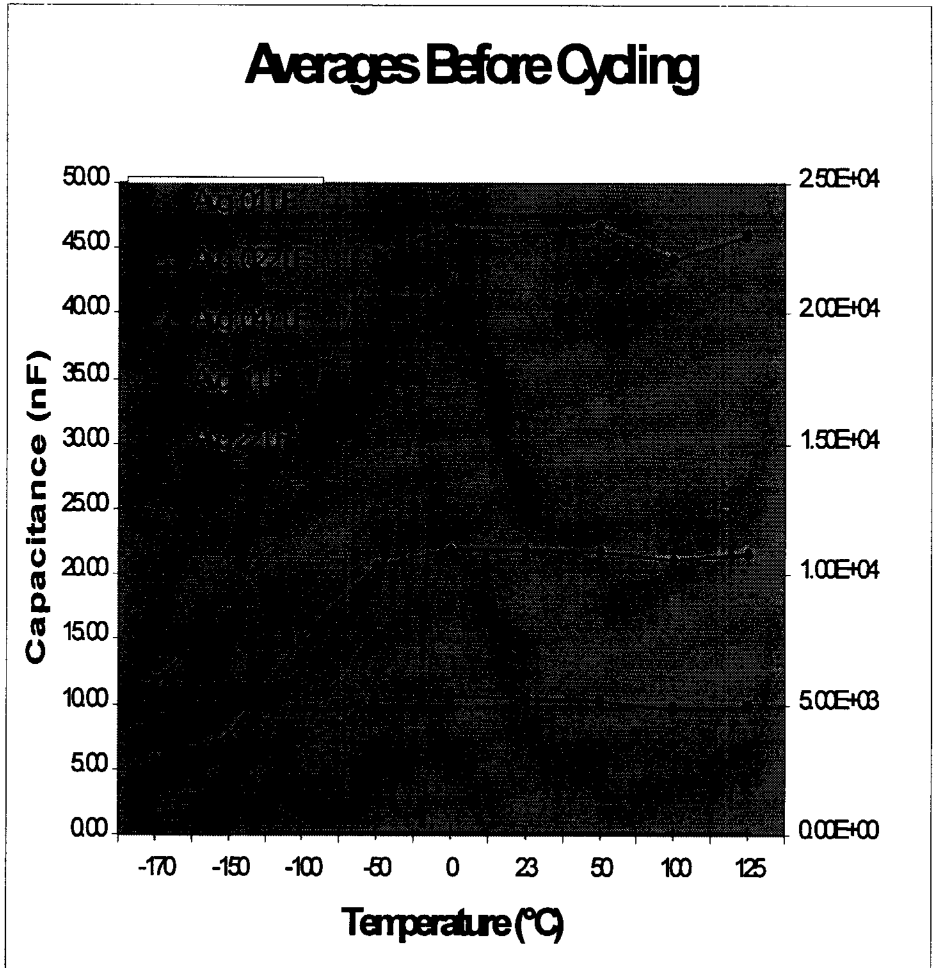

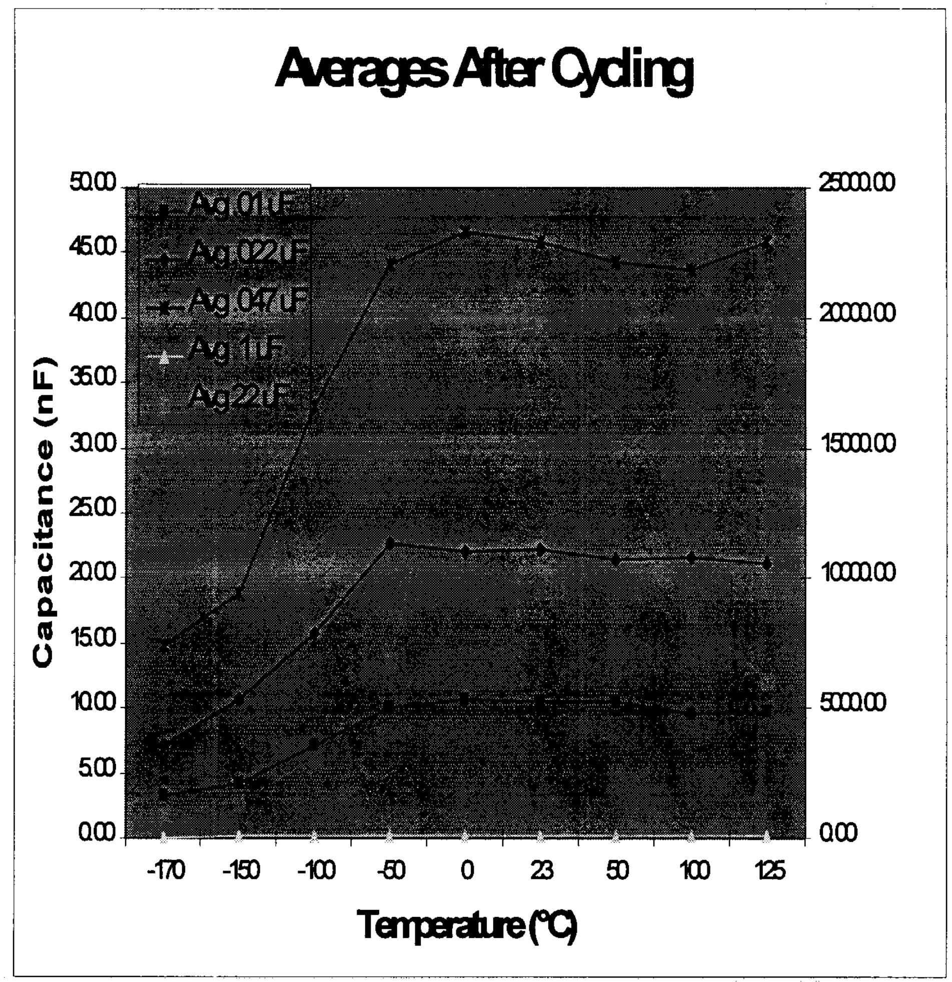

Active Electronics Component Operation at Extreme Cold Temperatures (-170C and Lower)

Changes in Active Devices at Cold Temperatures

- Electrical parameter changes.
  - Bipolar components suffer from carrier freeze out due to ε^{-kt} component in gain equations of BJTs.
  - MOSFETs gain is a function of electric field inversion due to voltage across the gate and channel mobility. The electric field is NOT a function of temperature, and mobility increases as temperature decreases.
  - In MOSFETS hot carrier injection is an issue.
    - Looks like a 2 to 3 reduction in lifetime due to this.
    - This can be mitigated to some extent by geometry changes.
    - We will be running hot carrier degradation tests this summer.

MOSFET Gain Equation

- MOSFET Gain Equation:
  - $I_{DS} = \mu_n C_{OX}/2 W/L (V_{GS} - V_{TH})^2$
- Two parameters changing here as temp lowers
  - Mobility, μ_n which increases
  - Threshold voltage V_{TH} which increases also
  - Higher I_{DS} for same operating and gate voltages
- Net Gain increase as temperature decreases down to liquid nitrogen temperatures since mobility increase dominates $(V_{GS} - V_{TH})^2$ term

Mobility As a Function of Temperature

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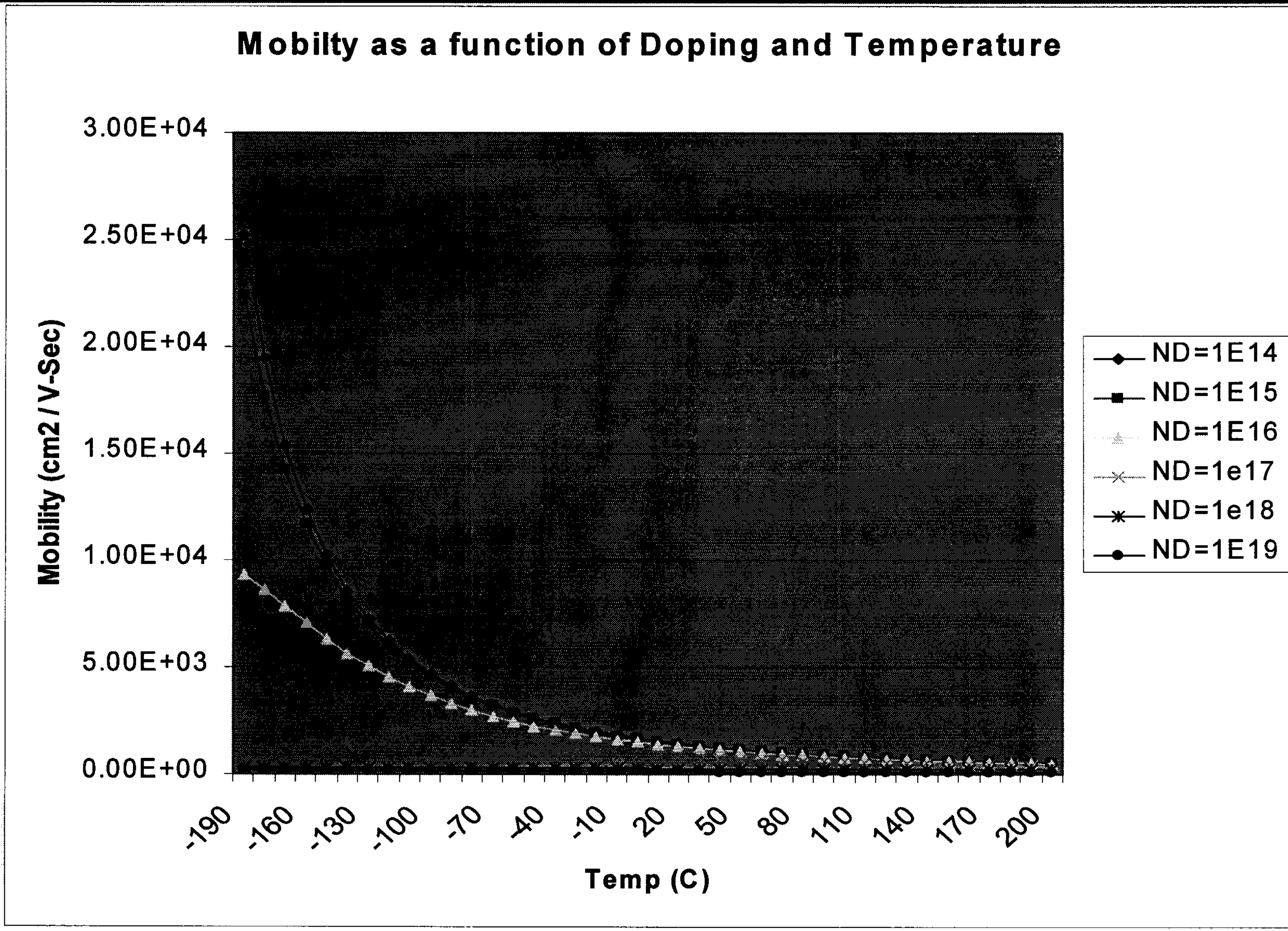

Threshold Voltage Shift

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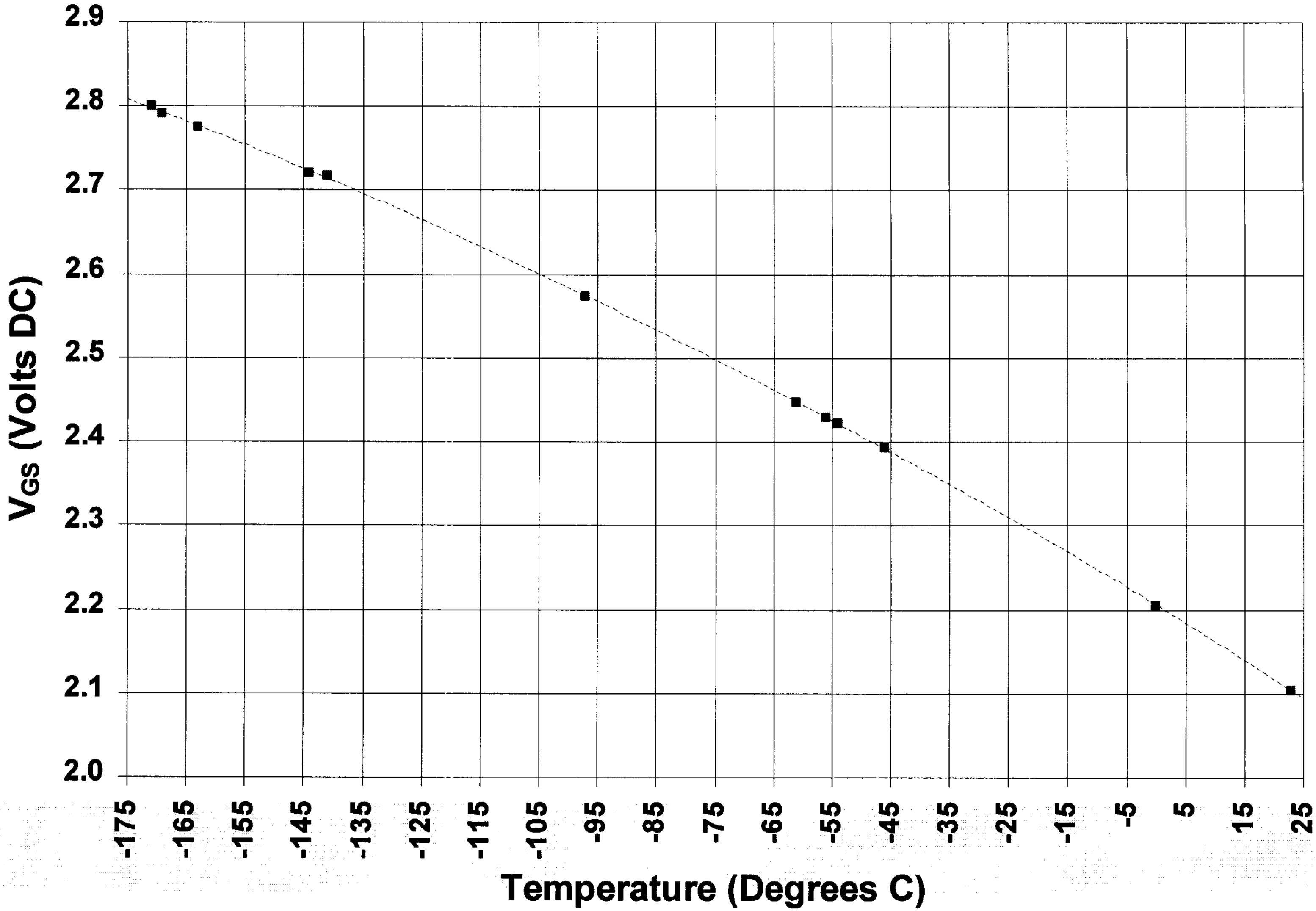

I_{DS} Increase As a Function of Temperature

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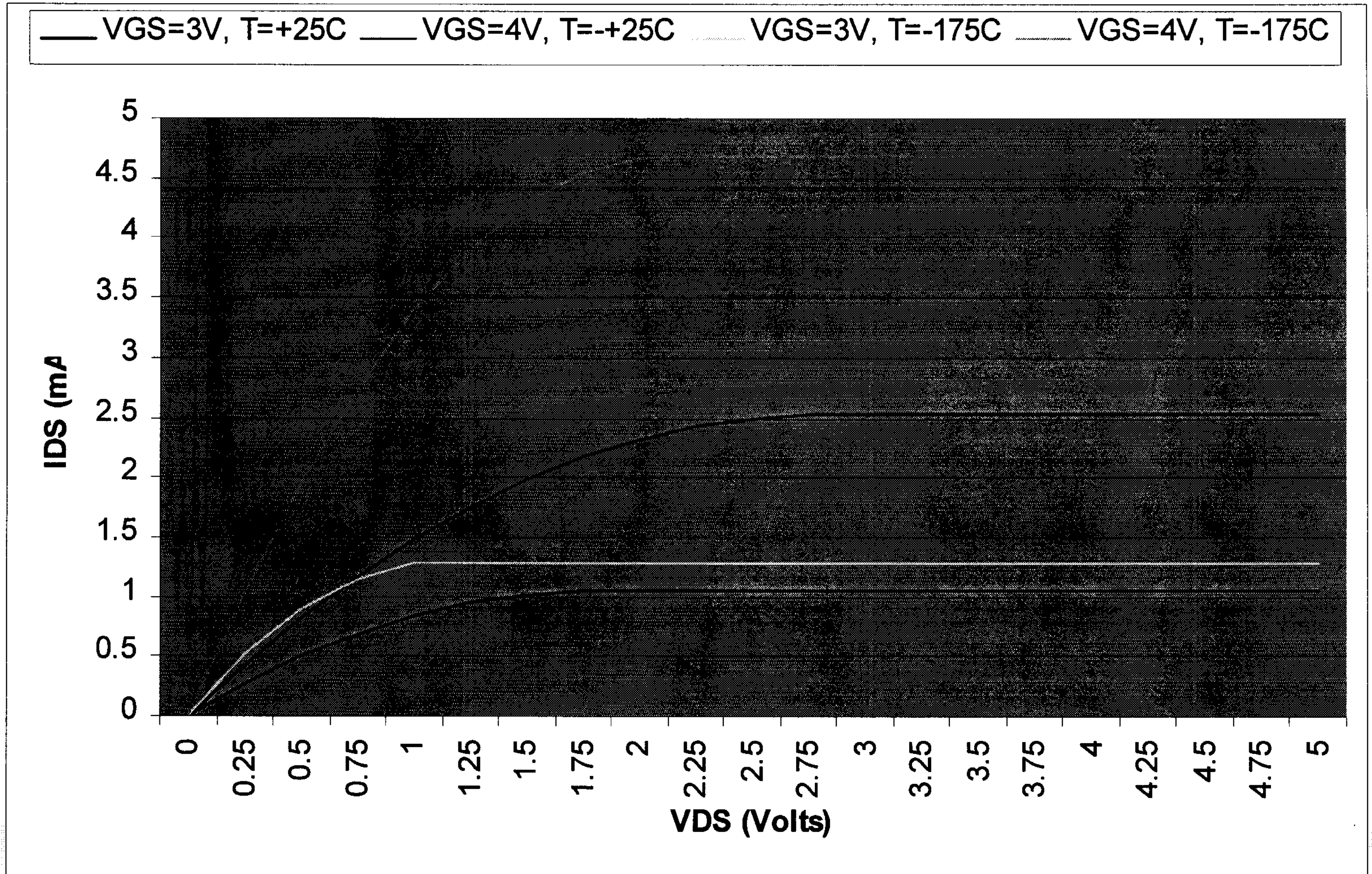
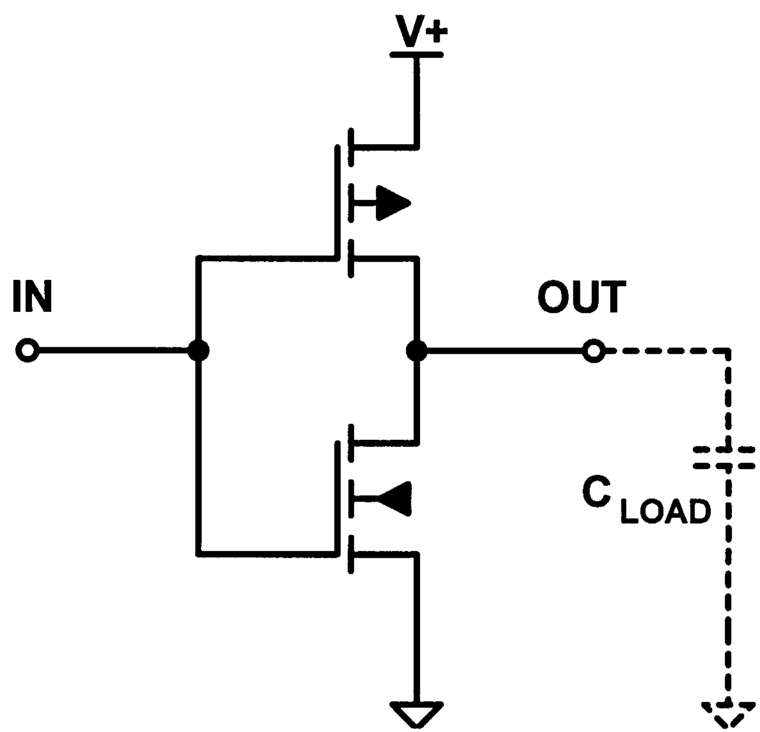


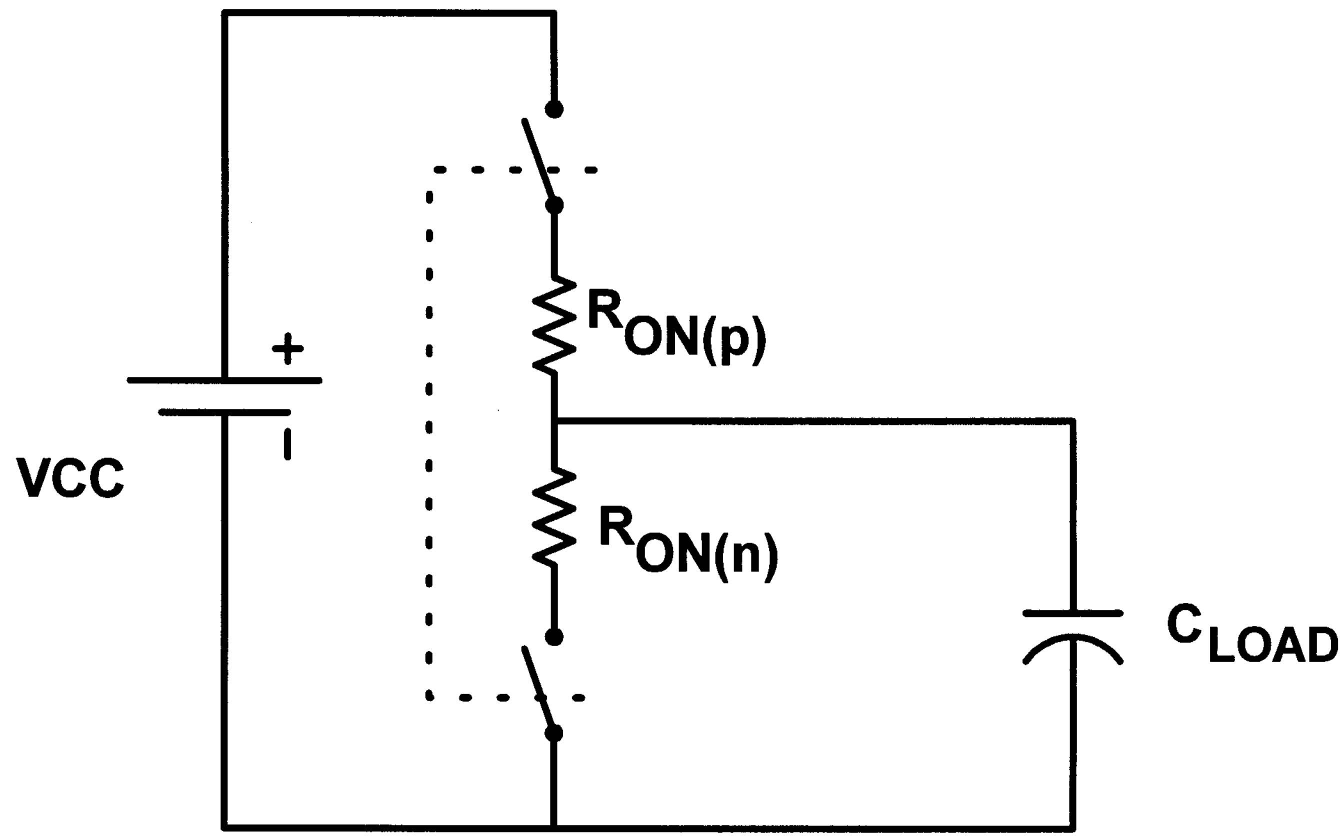
Effects of Temperature on Digital Logic

- CMOS, made of complementary MOSFETS inherit these cold temperature effects.
- Propagation delay decreases.
- Lower propagation delay has the possibility to cause hold time violations.

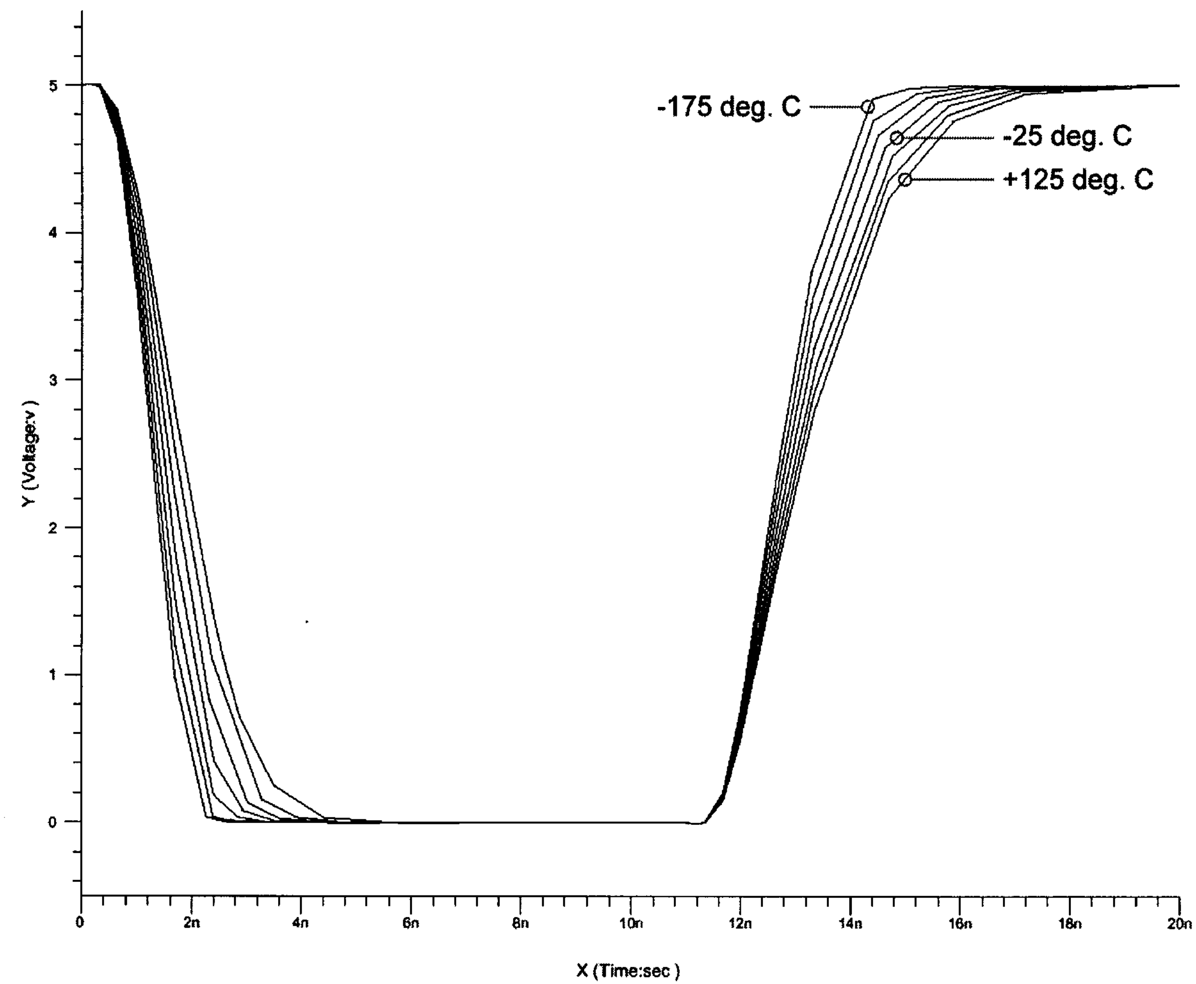
CMOS Inverter



CMOS Inverter Model



Simulation of Propagation Delay on Temperature



Cold Temperature Digital Component Tests

- Testing of 74C04 and 74HC245 at 23C and -193C to see if propagation delay can be recovered by lowering the logic supply.
- Shows the Variance of CMOS logic Propagation delay when changing Voltage and Temperature

Propagation Delay
74C04 5 Volts, 23C

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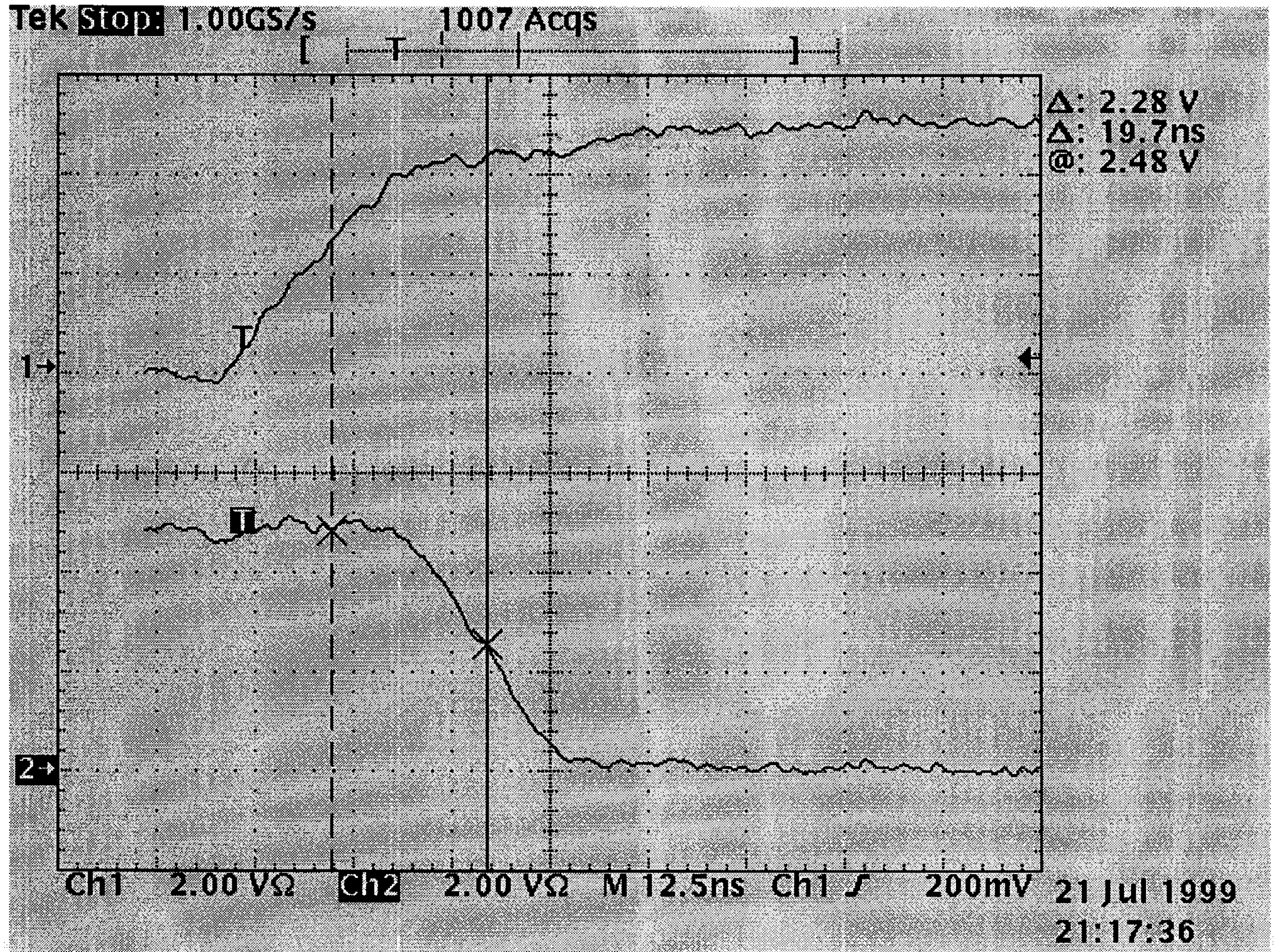

PROPOGATION DELAY: 19.7 nS

Propagation Delay
74C04 5 Volts, -193C

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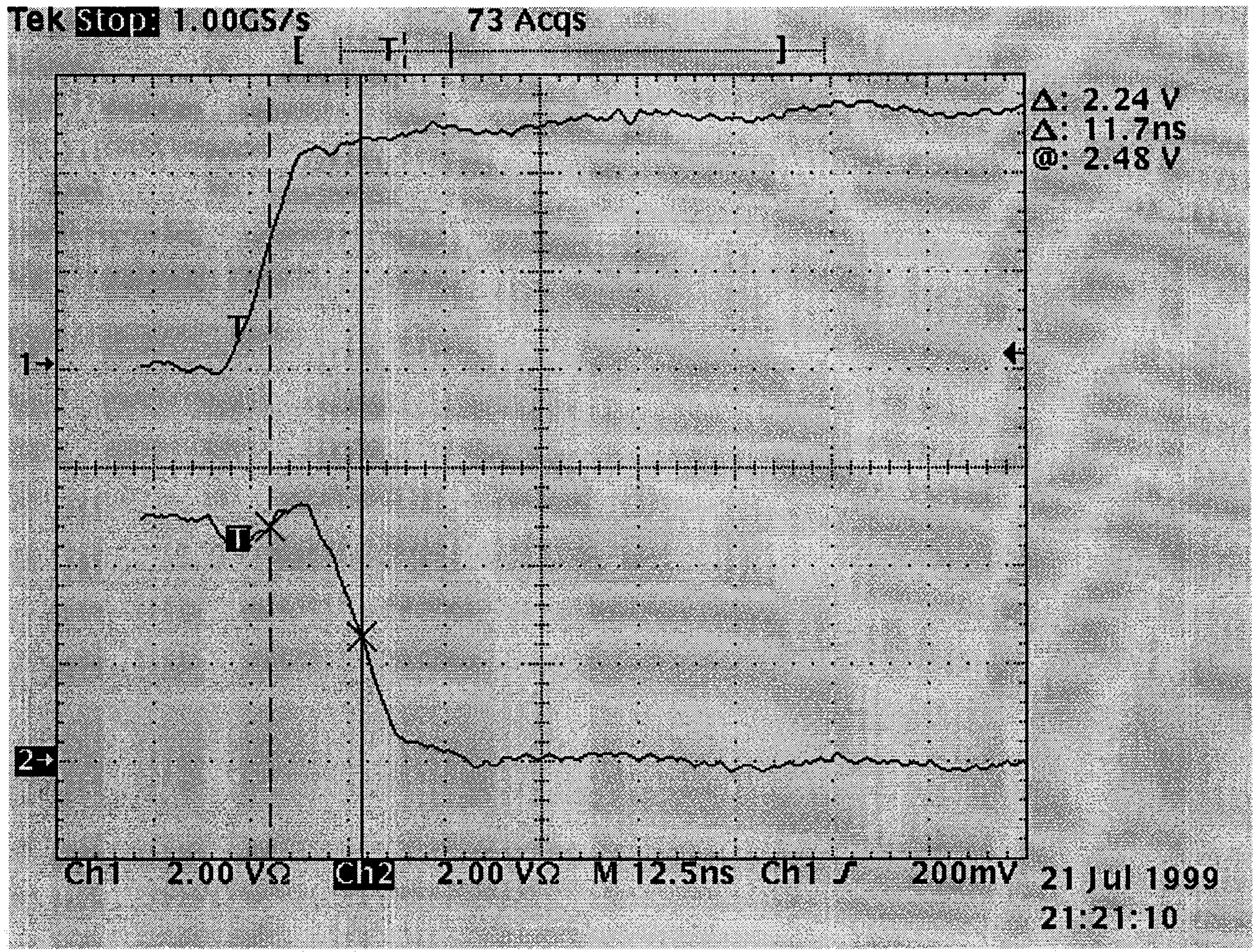

PROPOGATION DELAY: 11.7 nS

Propagation Delay
74C04 3.8 Volts, -193C

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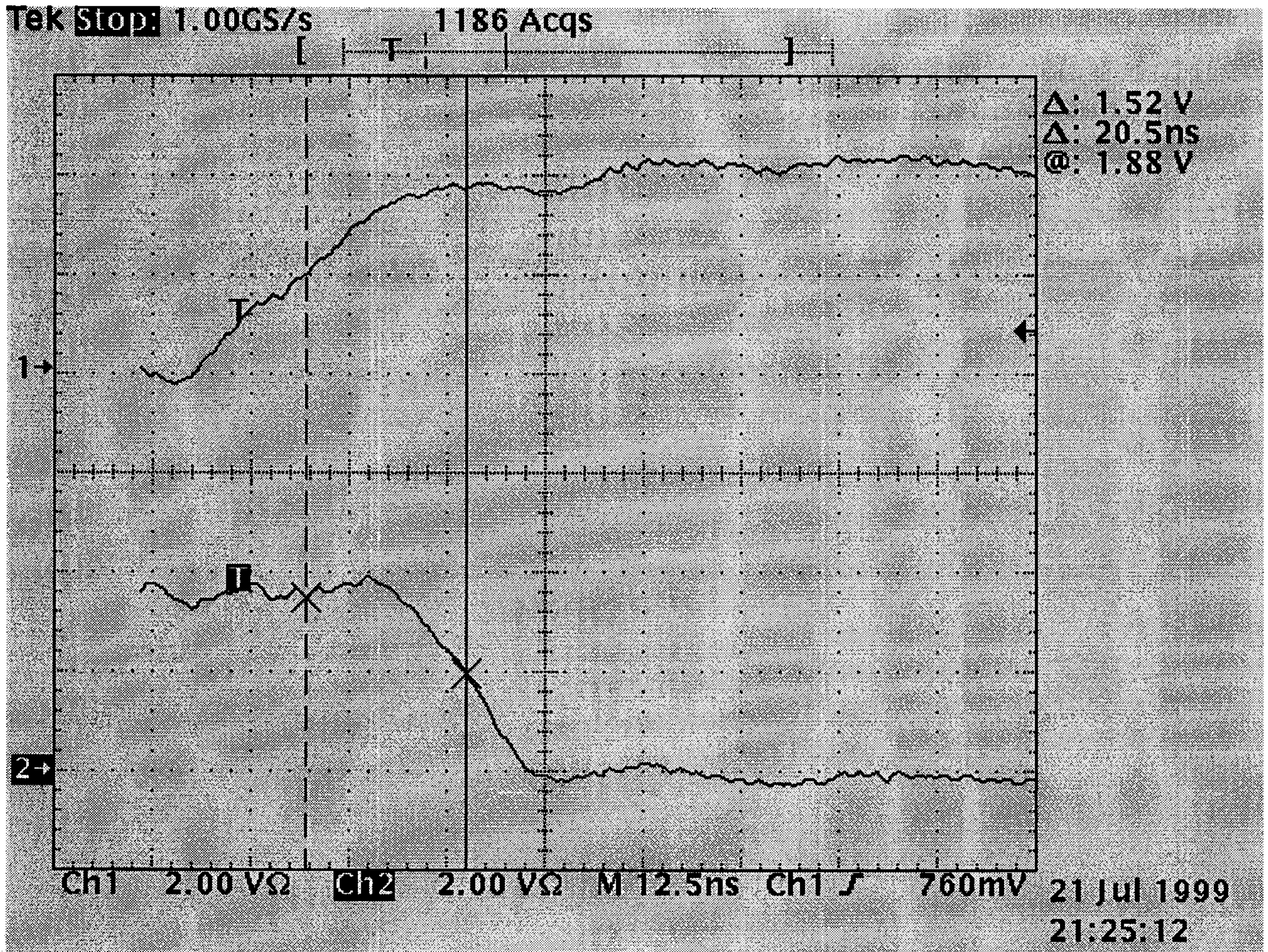

PROPOGATION DELAY: 20.5 nS

Cold Temperature Digital Component Analysis

- With propagation delay decreasing, hold time violations are a risk.
  - Design system so that hold time is not an issue at a system level.
  - If hold time errors occur internal to a device at cold temperature, the voltage of the device can be lowered to regain timing margin.

Hold Time Conundrum

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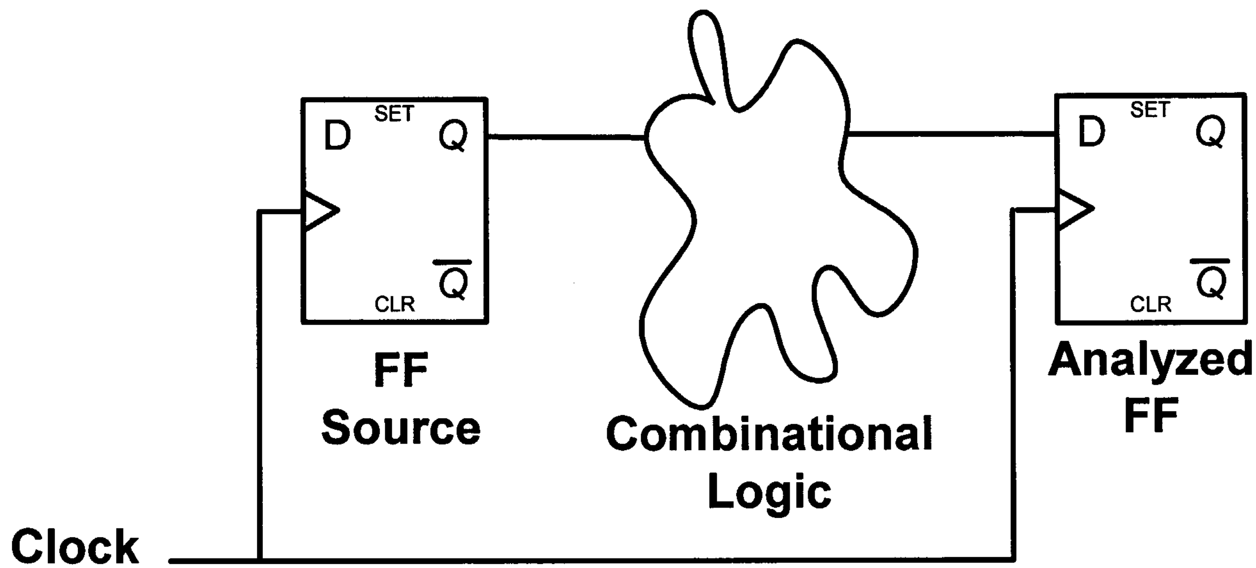

Digital Component Types Tested

- Mongoose V and LSI R3000 processors
- Honeywell SRAM
- BAE SRAM
- Honeywell ASICs
- Northrup Grumman EEPROM
- Standard logic
- Various DRAMs on our prototype

Analog Component Types Tested

- CMOS/MOS multiplexors tested
  - All worked well, make before break maintained
- CMOS op-amps tested
  - CMOS op-amps with "standard" class AB output amp stages failed routinely in the -100C range
  - A non standard national part worked great cold, but had to be shielded for radiation (8krad due to gate oxide)
- Power MOSFETs were use as analog circuit components quite effectively

The Nanorover Implementation

Constraints on the Rover Electronics

- Low Mass: 180 grams
- Low Power: 2.56 Watts from Solar Cells
- Low Volume: 226.8 cm^3
  - (12 cm x 12.6 cm x 1.7 cm)
- Large Temperature range:
  - -180C to +125C Survival Range
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- Mass and Volume drives the packaging to chip on board.

Rover Interfaces

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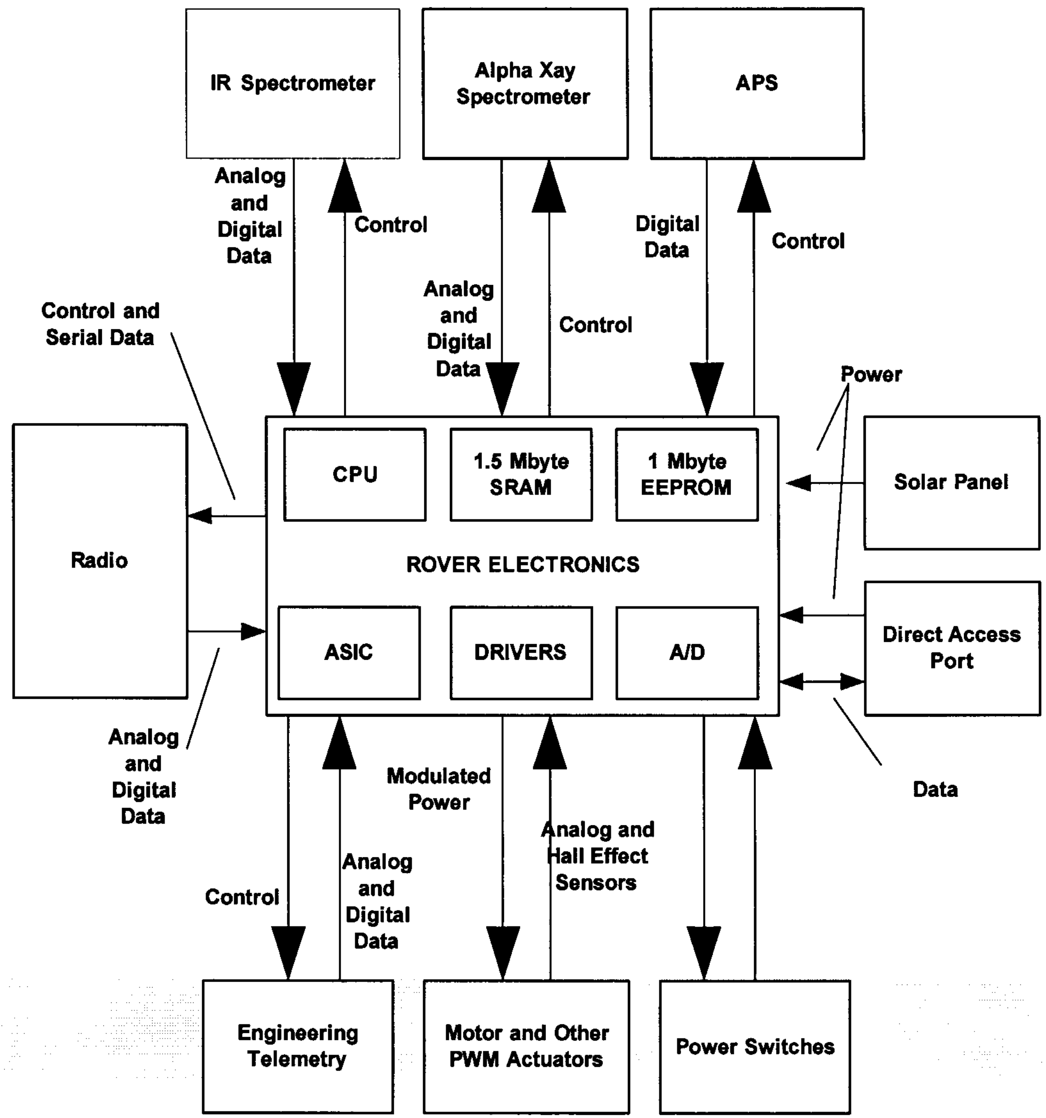

Rover Electronics Block Diagram

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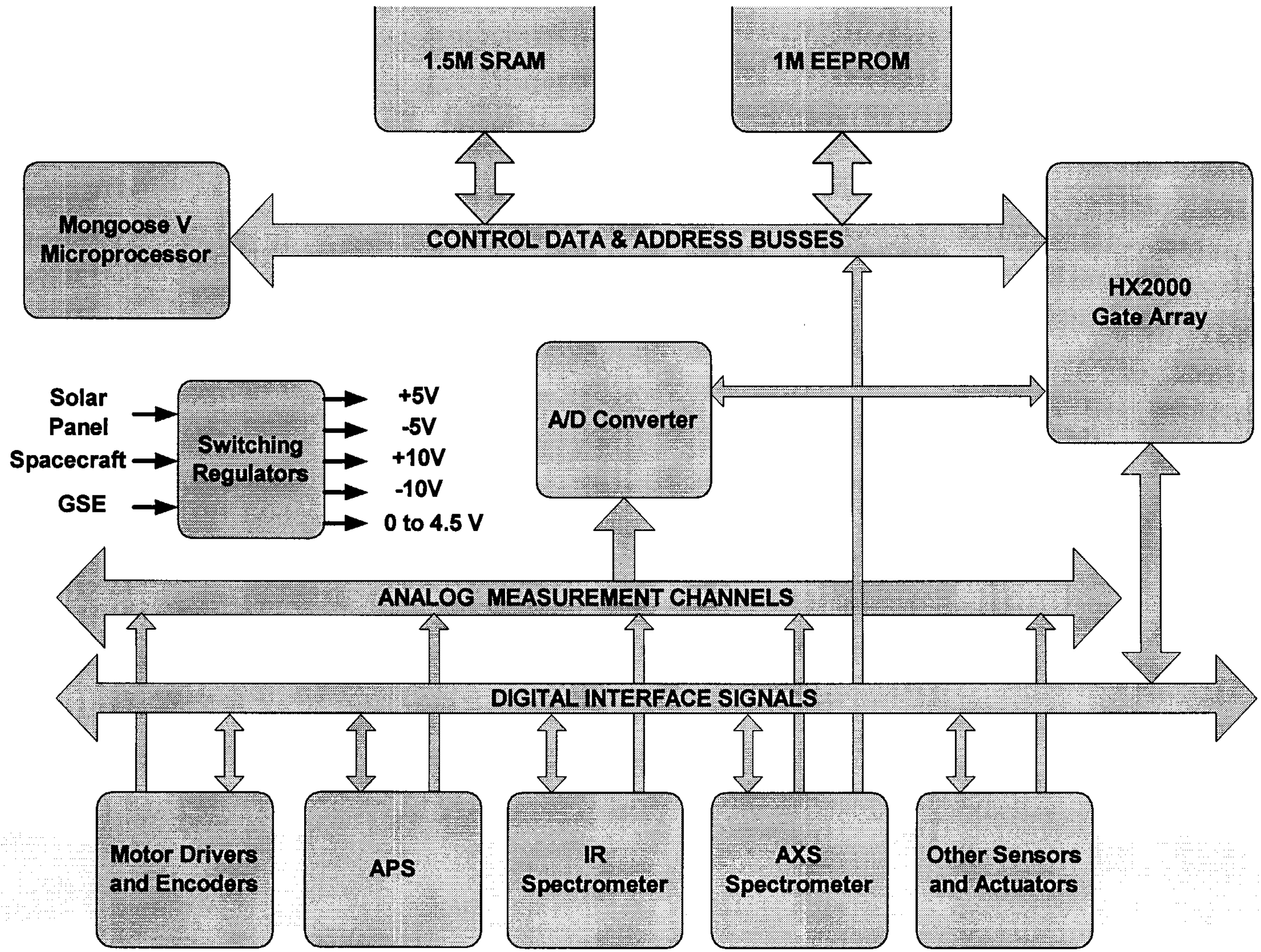

Board Footprint

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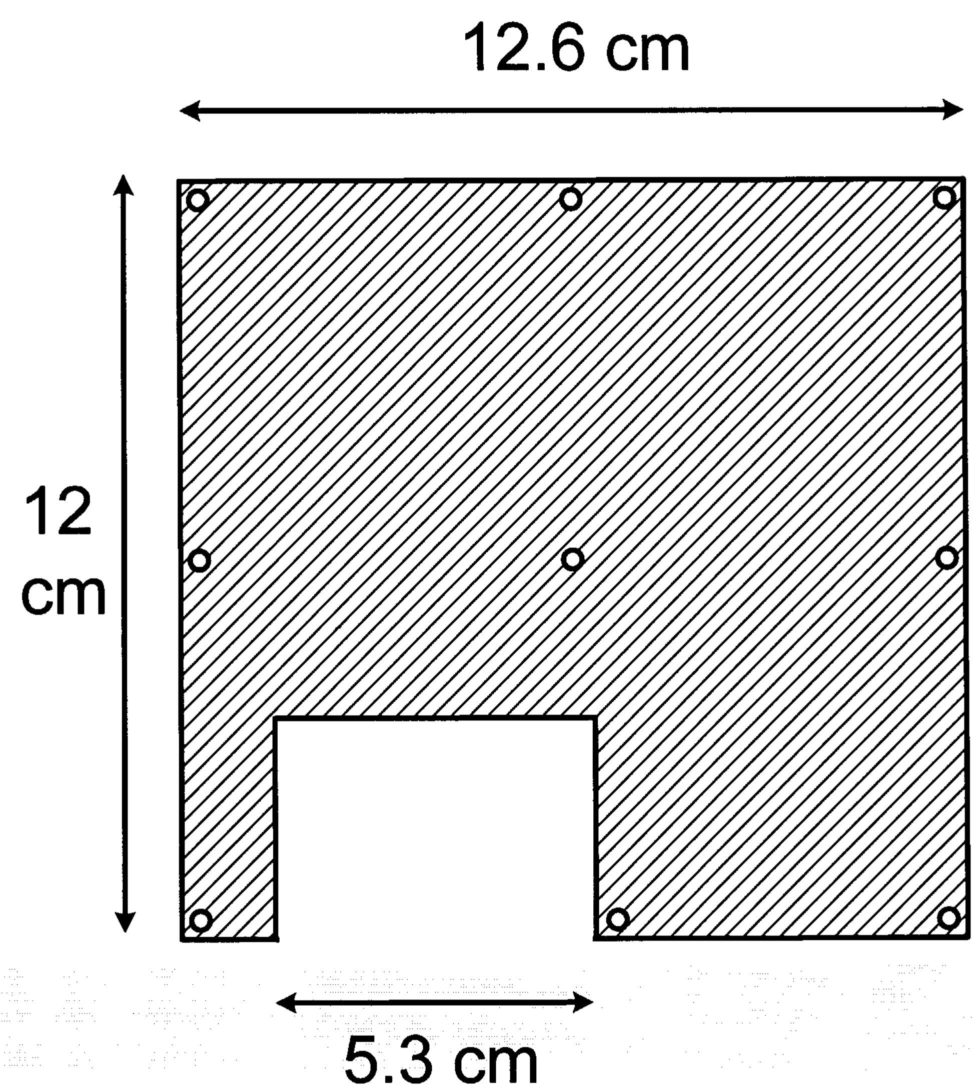

Board Footprint

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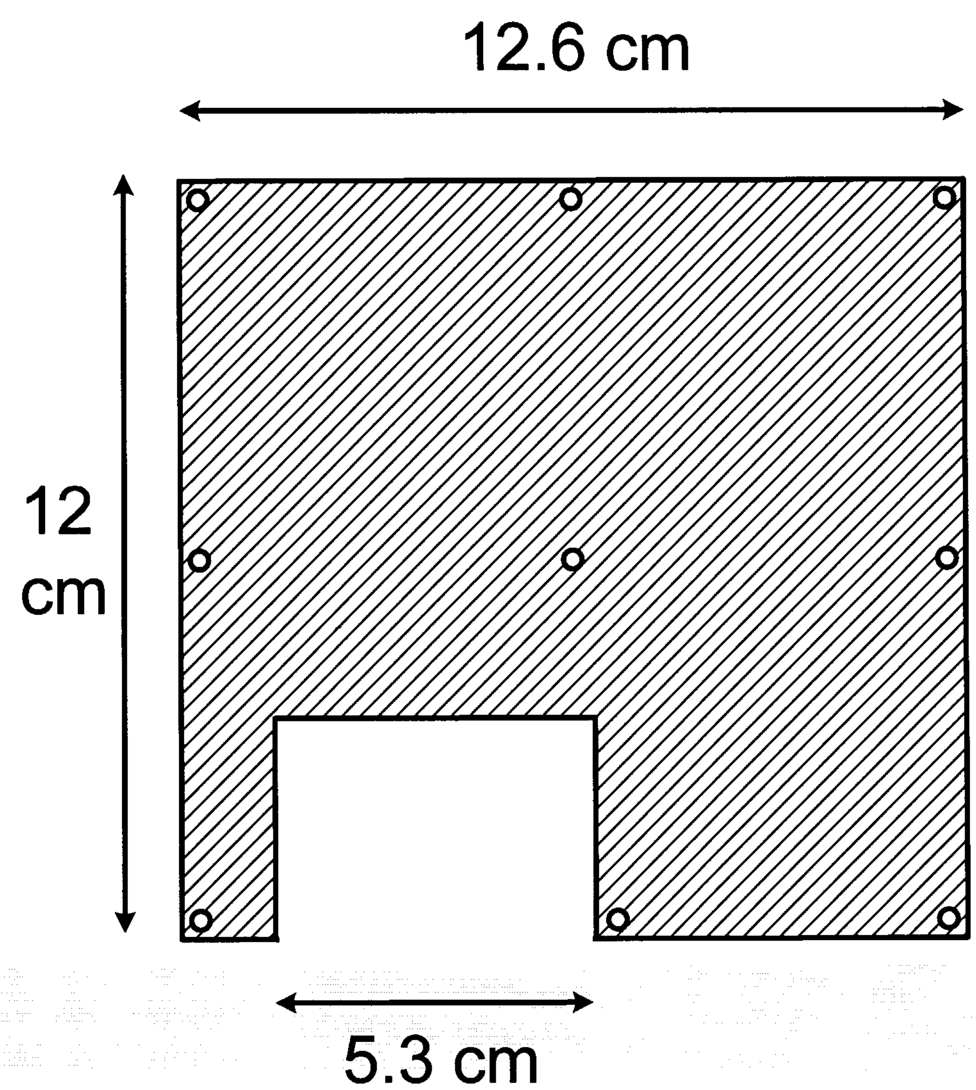
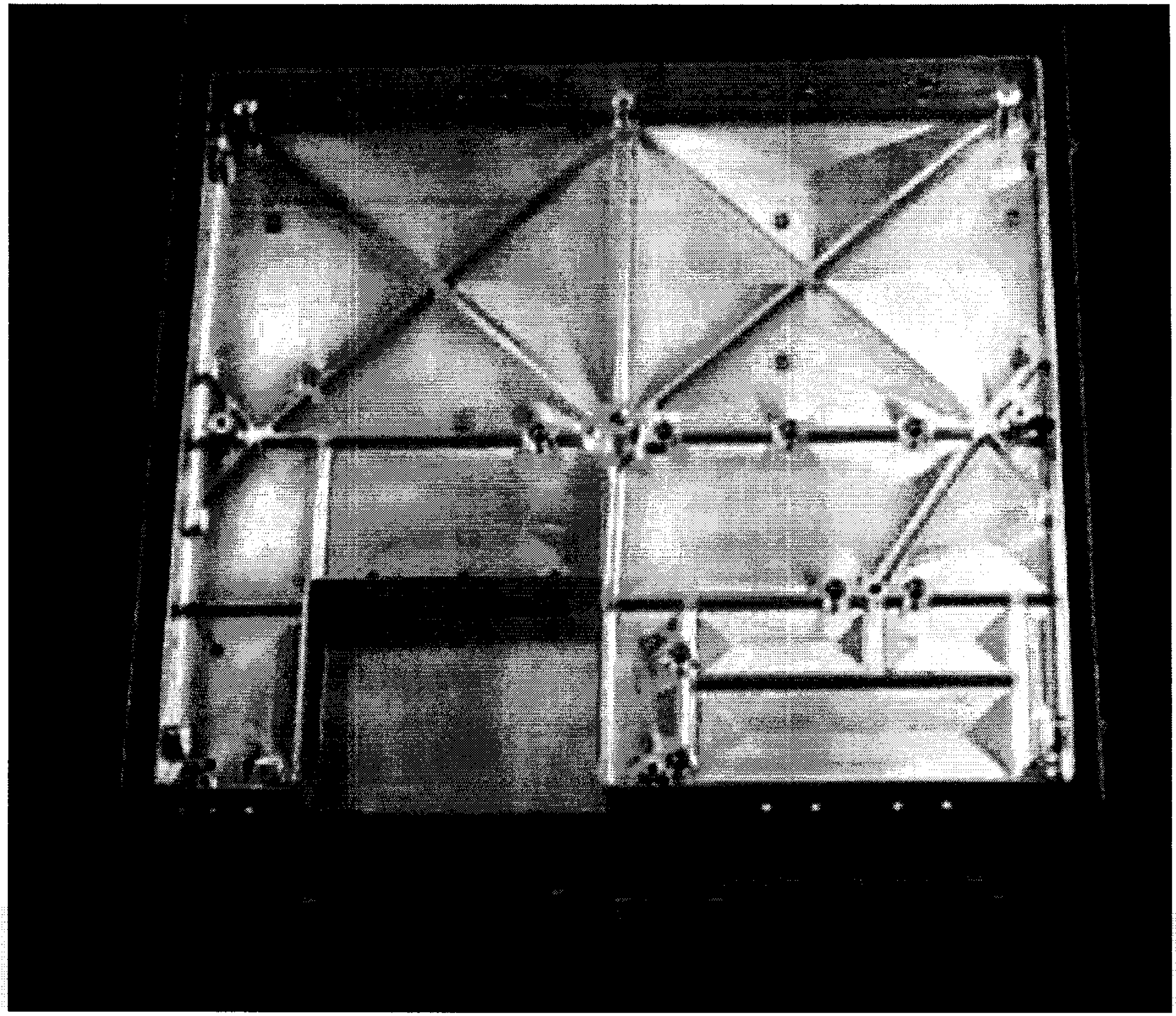


Optical Bench With Board Attach Points



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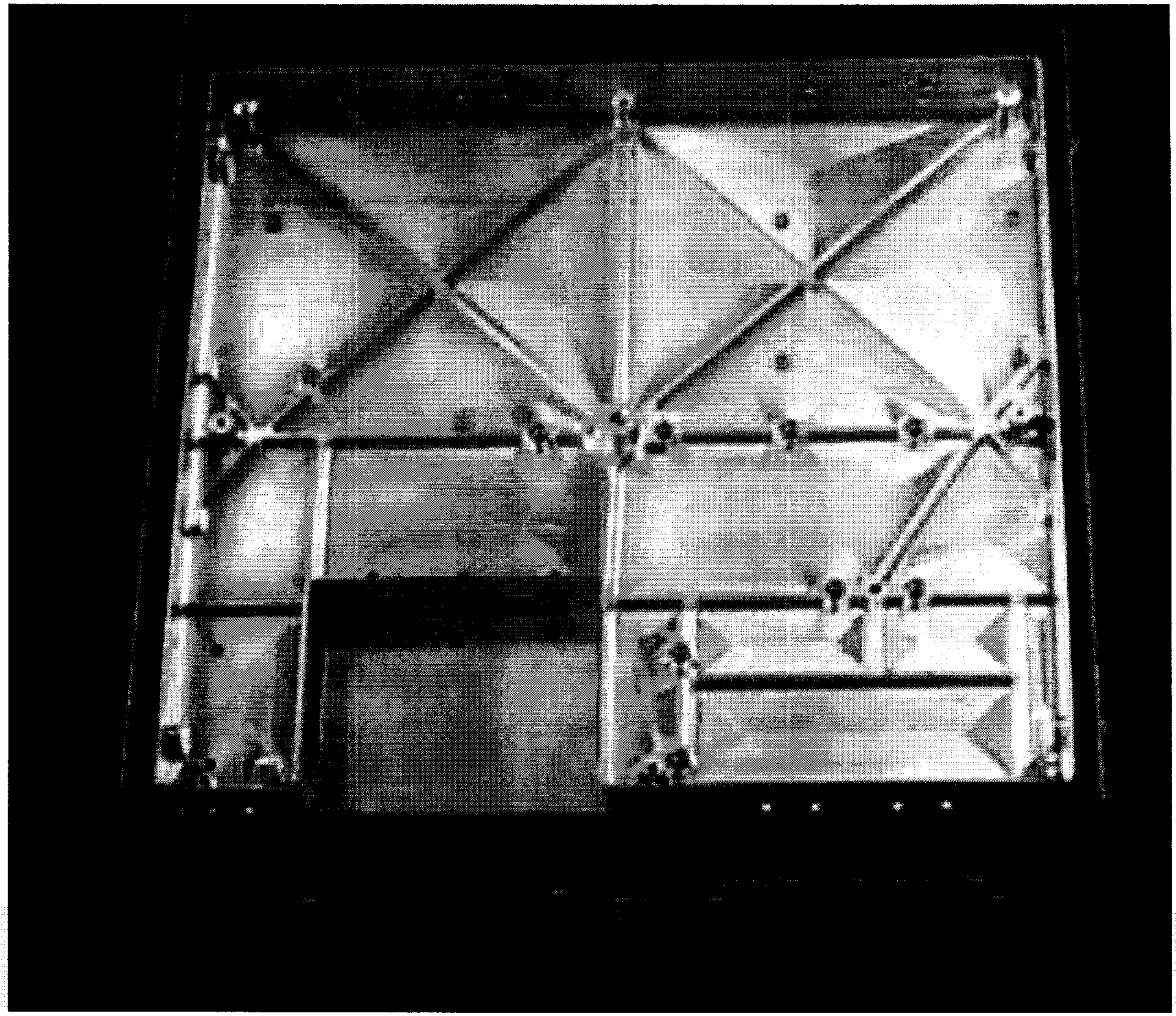

Side View of Boards

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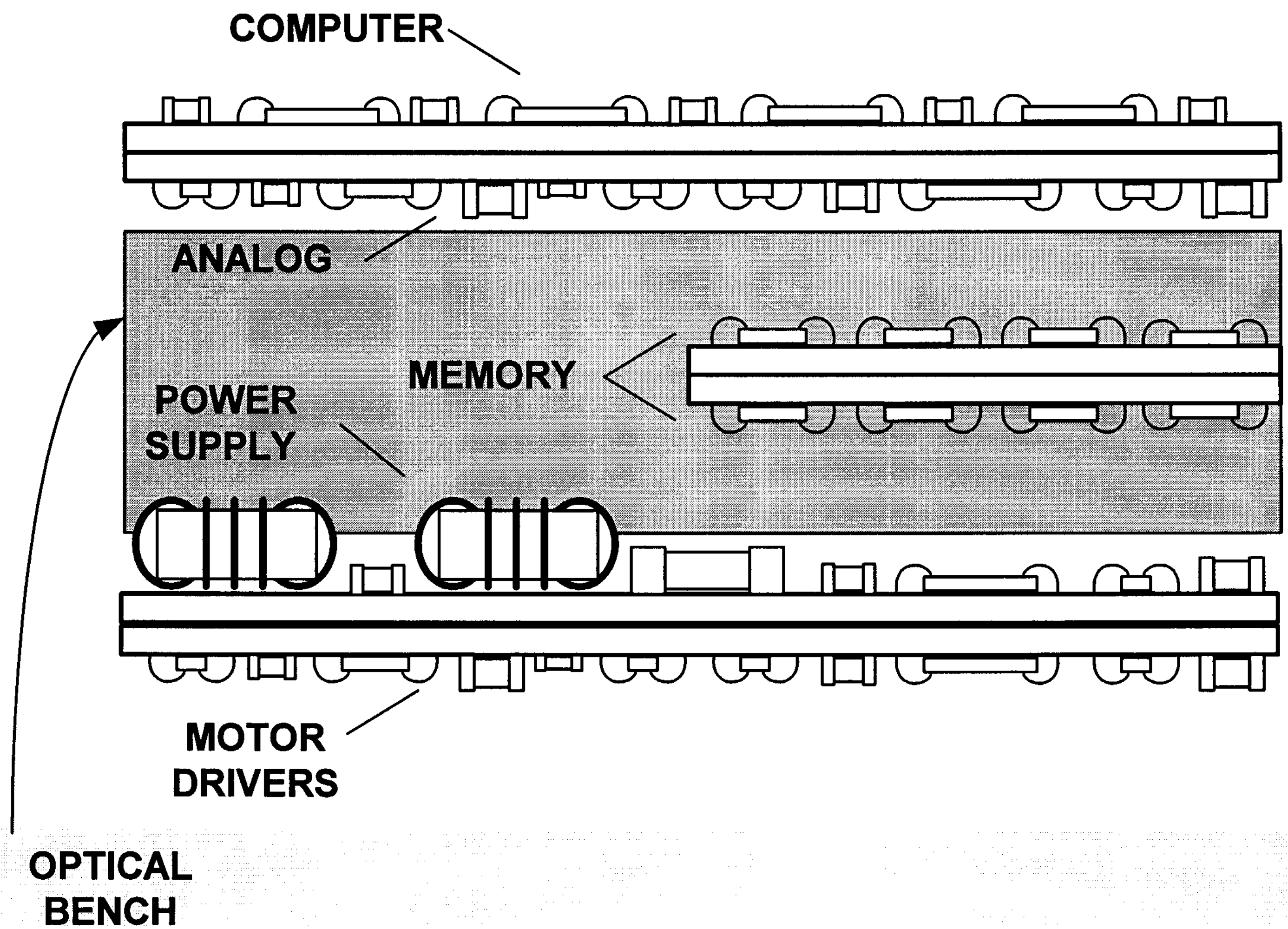
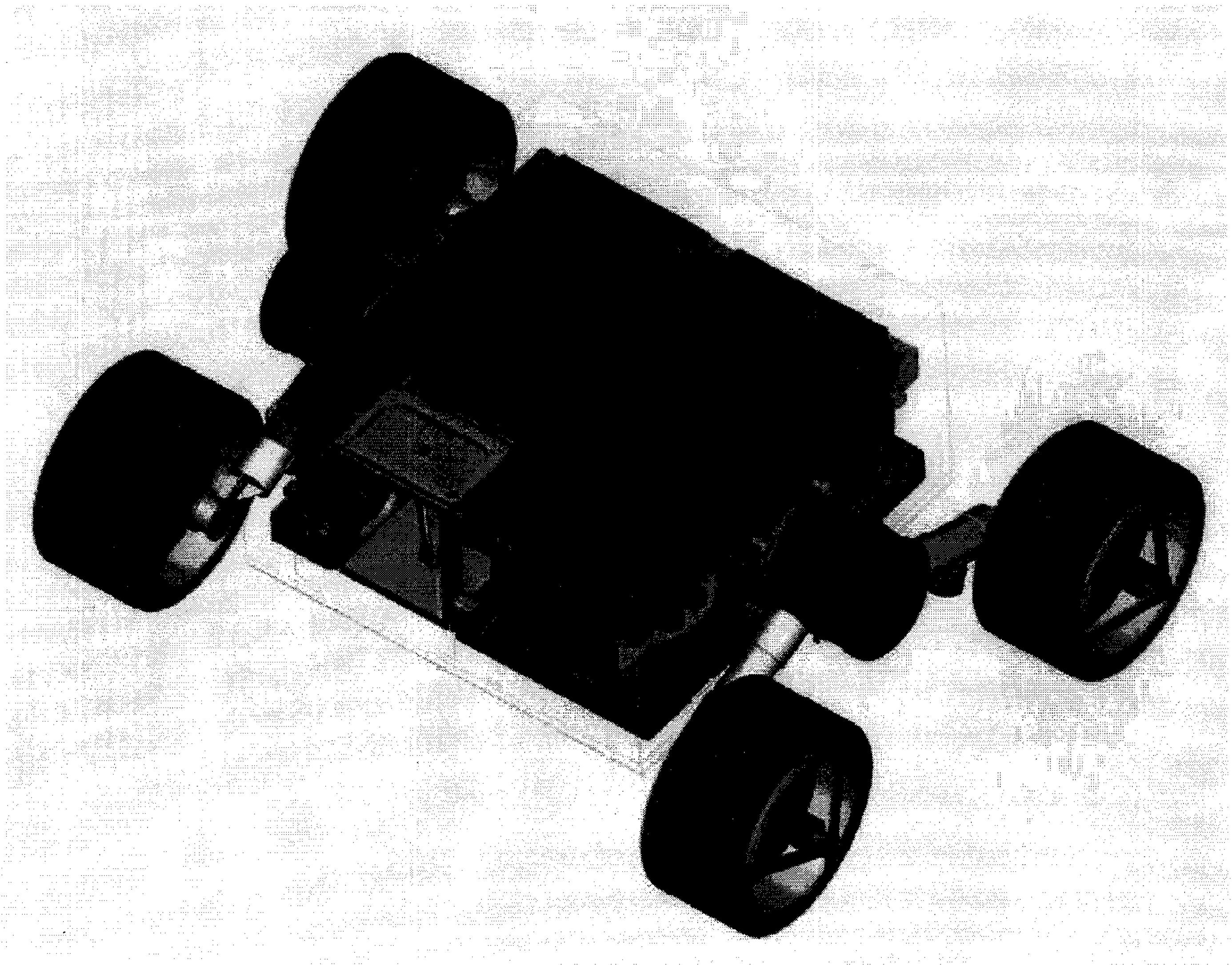
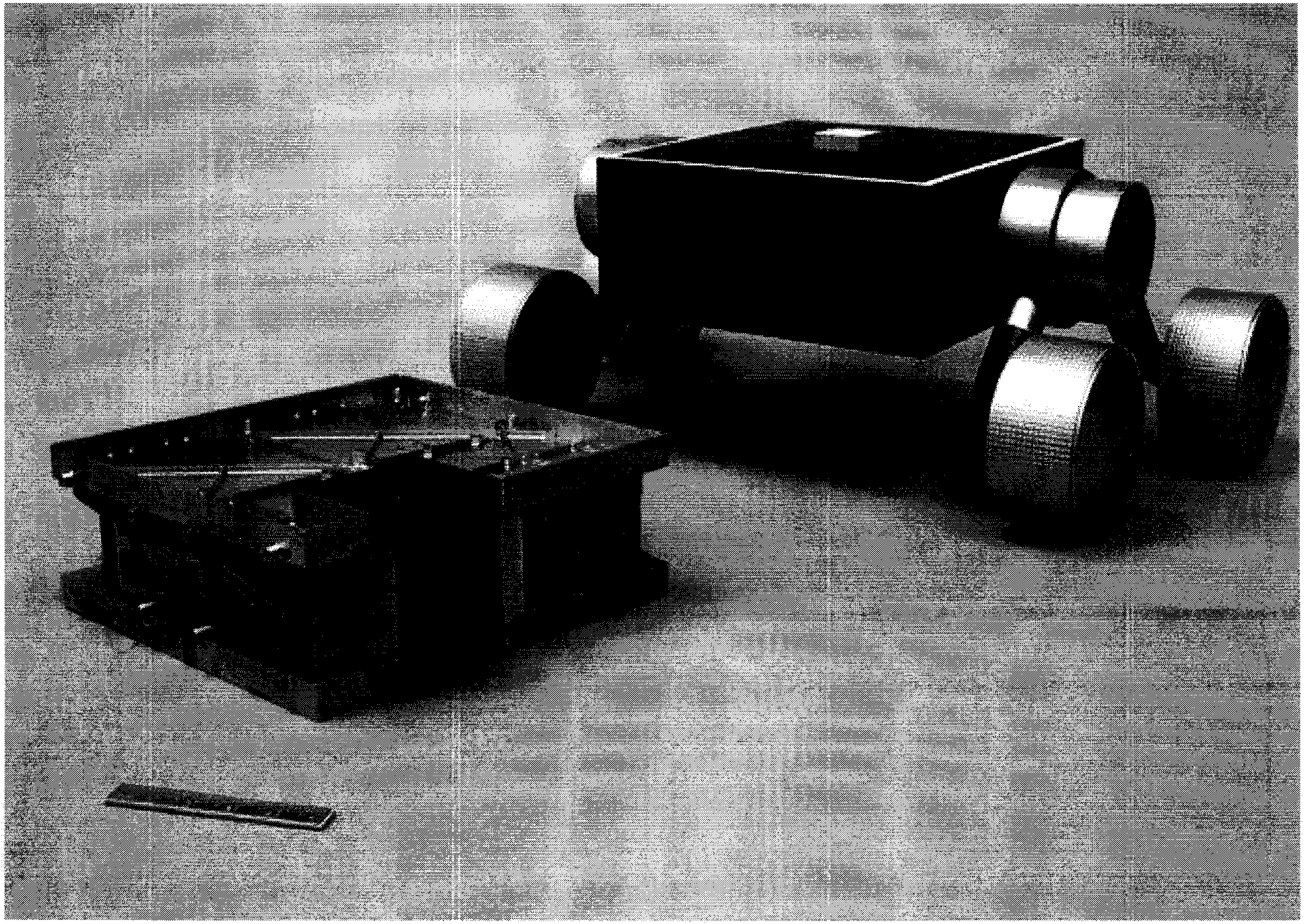


Rover Overview



Optical Bench Relative to Body



Summary

- Operation at temperature ranges extended into the extreme cold temperature region works.
- Functionality is reliable at extreme cold temperatures
- Lifetime of active devices is limited to Hot Carrier Injection in active devices at cold temperature and is a reliability issue.
- Existing parts can be used
- The length of missions using existing parts is a function of HCI degradation and mechanical cycling fatigue mitigation.

Questions

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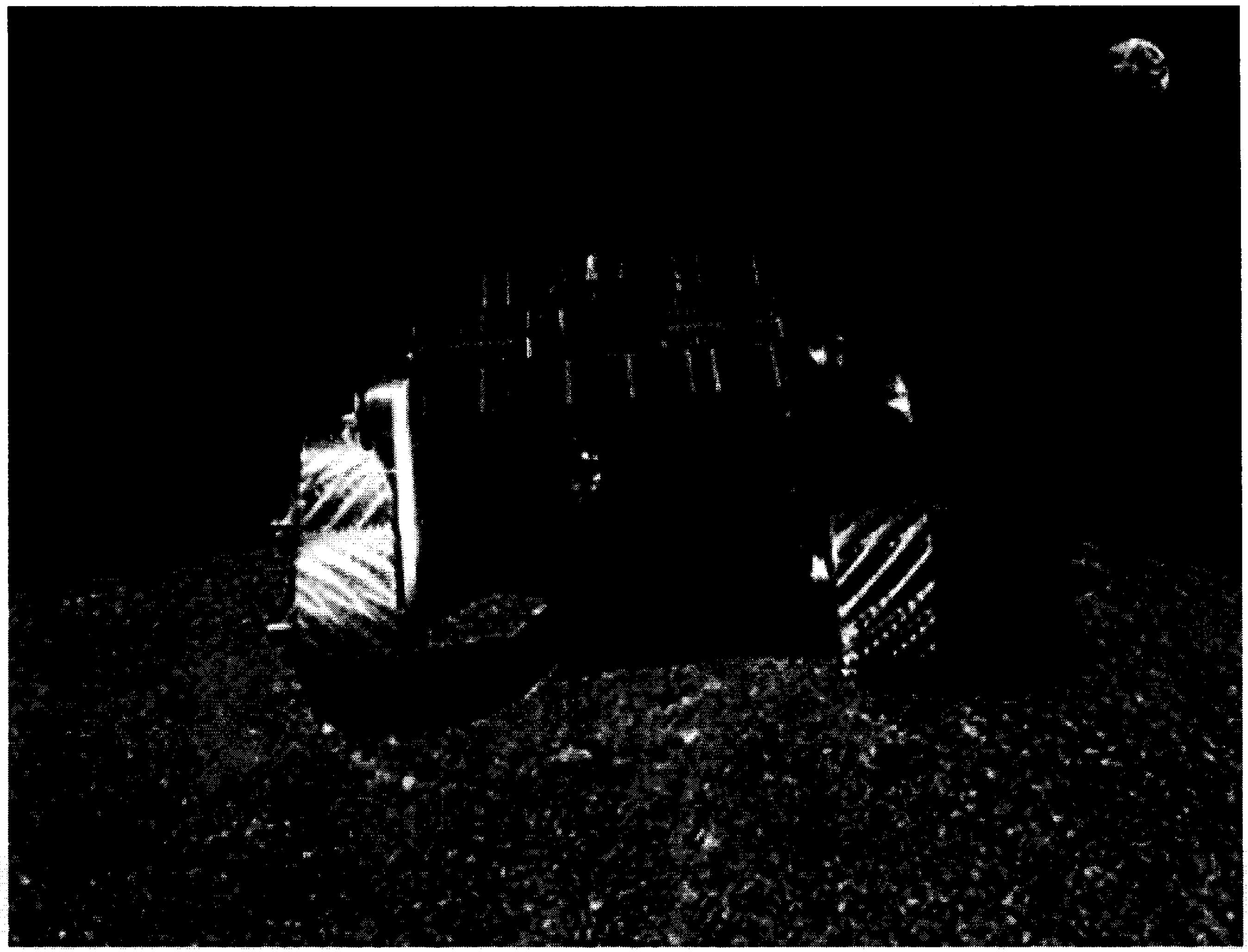

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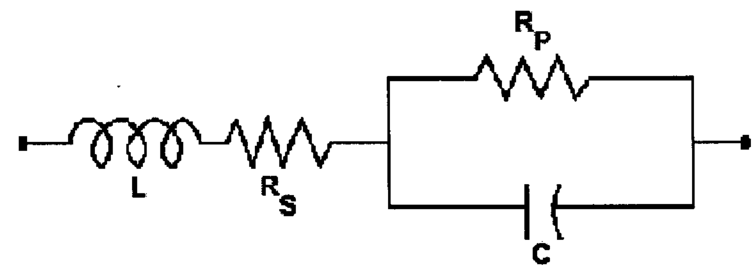
Additional Slides

Impedance

$$Z=\sqrt{[(R_S^2 + (X_C-X_L)^2]}$$

Z = Total Impedance
R_S = Series Resistance
X_C = Capacitance Reactance
f = Frequency
C = Capacitance
X_L = Inductive Reactance
L = Inductance

Equivalent Circuit for MLC



C = Capacitance
R_S = Equivalent Series Resistance (ESR)
L = Inductance
R_P = Insulation Resistance (IR)

$$X_C = \frac{1}{2\pi f C}$$

$$X_L = 2\pi f L$$

Effects of Frequency

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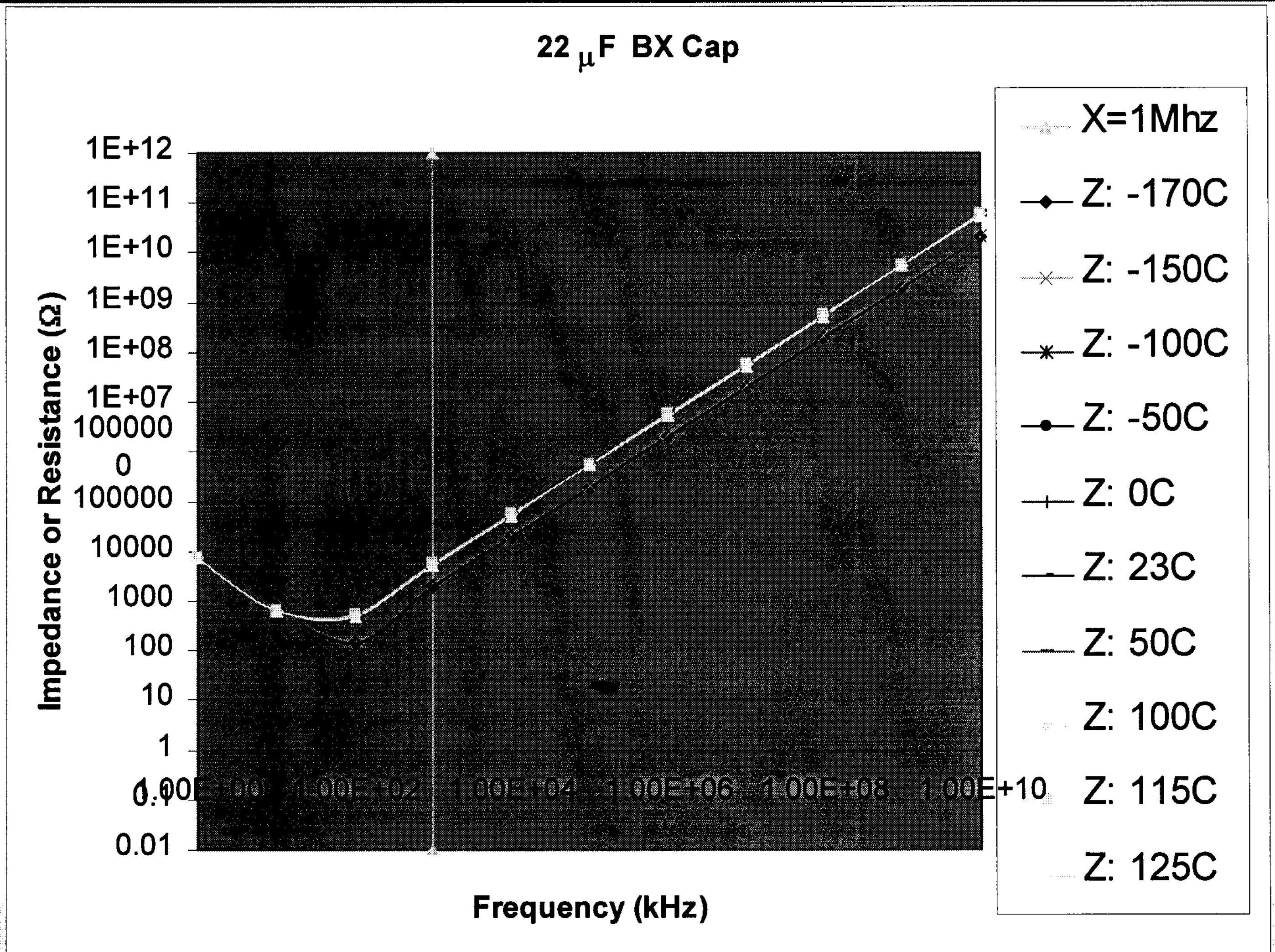
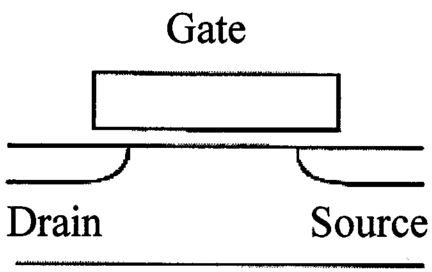
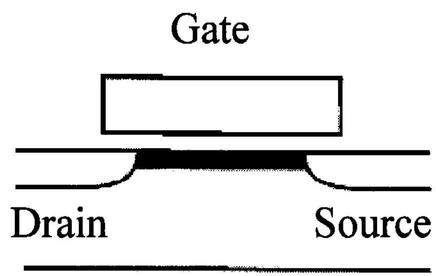


MOSFET Diagram



MOSFET

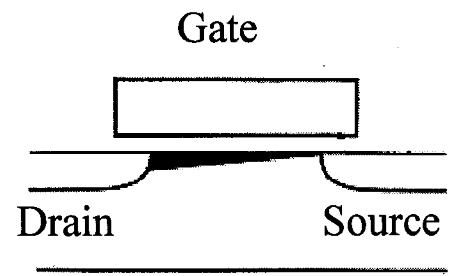
No Voltages Applied



MOSFET

Gate Voltage Applied

No Drain-Source Voltage Applied



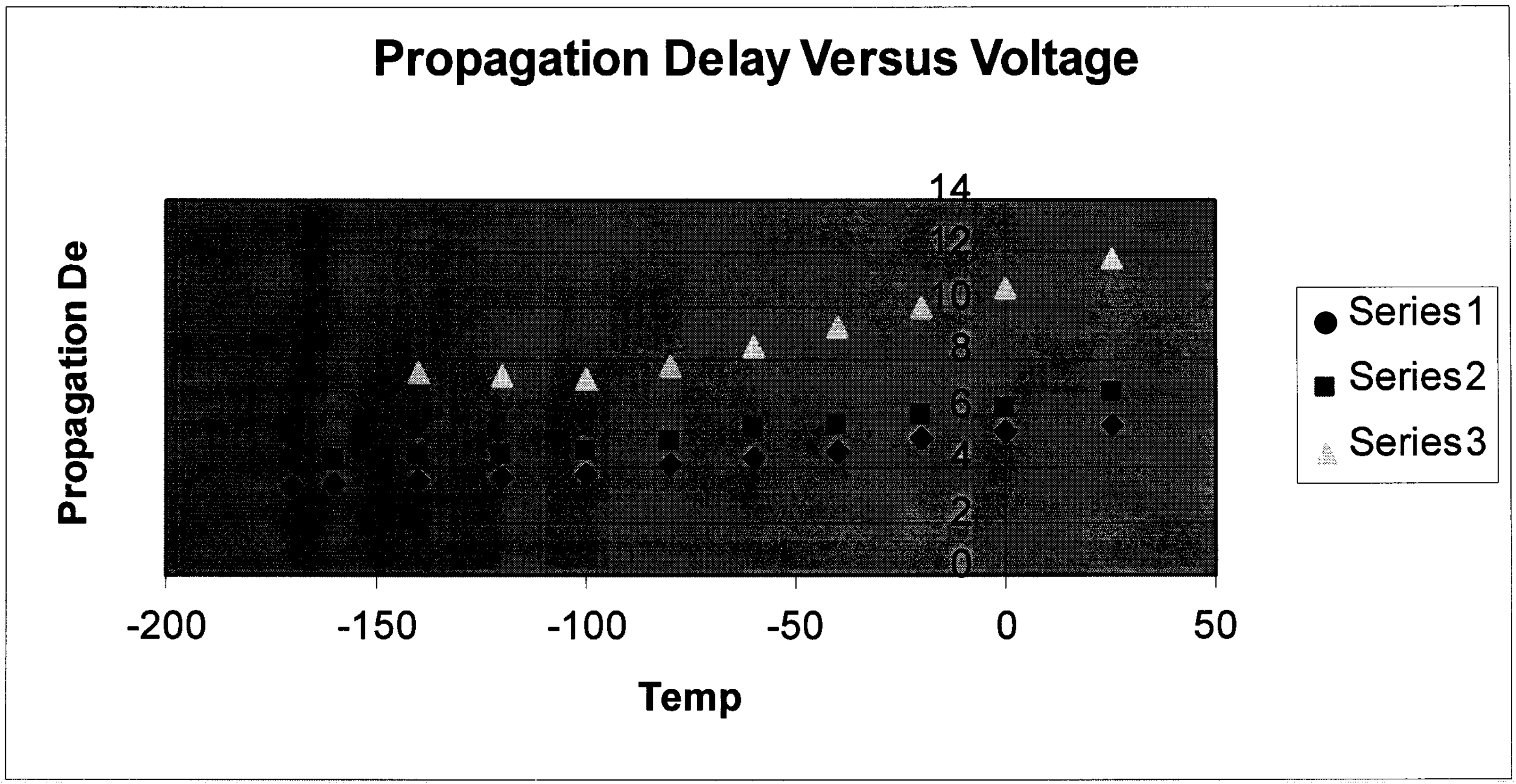
MOSFET

Gate Voltage Applied

Drain-Source Voltage Applied

Temperature and Voltage Variations of a 70C04

Update series titles



Summary

- Variation of the dielectric constant κ′ with temperature describes the linear decline in capacitance in cold temperatures for ceramic capacitors
- Temperature cycling has no effect ($p>.05$)

Trends

ELECTRICAL AND MECHANICAL COMPONENTS ARE GETTING EASY TO MINITURIZE

IMPLIES

ABILITY TO BUILD SMALLER SPACECRAFT AND SCIENCECRAFT

Trends

SMALLER S/C — IMPLIES → ENABLES MISSION OPPORTUNITIES OTHERWISE NOT POSSIBLE

SMALLER S/C — IMPLIES → POSSIBILITY FOR MULTIPLE S/C TO INCREASE COVERAGE / RELIABILITY

Implications

SMALLER S/C → IMPLIES → LOWER VOLUME

LOWER VOLUME → IMPLIES → LOWER SURFACE AREA

LOWER VOLUME → IMPLIES → LOWER MASS → IMPLIES → LOWER THERMAL MASS

Second Level Implications

LOWER THERMAL MASS → IMPLIES → LARGER THERMAL SWINGS OF S/C

LOWER SURFACE AREA → IMPLIES → LESS SOLAR RADIATION HITTING THE S/C

Implications Ad Nausea

LESS SOLAR RADIATION HITTING THE S/C

IMPLIES

LESS ELECTRICAL ENERGY AVAILABLE FROM SOLAR CELLS

LESS ELECTRICAL ENERGY AVAILABLE FROM SOLAR CELLS

IMPLIES

LESS POWER AVAILABLE FOR ELECTRONICS

Implications Ad Nausea

LOWER VOLUME	IMPLIES	ELECTRONICS COMPONENTS ARE CLOSER TO EACH OTHER
ELECTRONICS COMPONENTS ARE CLOSER TO EACH OTHER	IMPLIES	NOISE ISSUES BECOME HARDER TO ISOLATE
ELECTRONICS COMPONENTS ARE CLOSER TO EACH OTHER	IMPLIES	RTHs AND RTGs WILL IRRADIATE ELECTRONICS OR CAUSE HUGE MASS INCREASE

Discussion Overview

- Micro and Nano science craft trends and implications and constraints
  - Discussion of temperature effects
    - In most cases everything gets cold
  - One possible paradigm: design electronics to work at cold temperatures