Long-life Reliability of CSP Assemblies With and Without Underfill

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
818-354-2059, Reza.Ghaffarian@jpl.nasa.gov

ABSTRACT

The test results for numerous chip scale package assembly performed under MicrotypeBGA Consortium led by the Jet Propulsion Laboratory have been published previously. The cycles-to-failure (CTF) under different thermal cycle conditions including –30 to 100°C revealed early failures of most assemblies, even a few with underfills.

However, a few CSP configurations with and without underfills did not failed early in this temperature range. These assemblies were further thermal cycled to establish their long-life failure behavior. Thermal cycling for most test vehicles (TVs) were stopped at 3,000 cycles except for four assemblies with underfills that survived such a long environmental exposure. To accelerate failure even further, the underfilled assemblies were subjected to a higher temperature delta in the range of –55 to 125°C. Additional failures were observe to 887 cycles in this temperature range. Reliability test results to 3,887 combined cycles along with optical and SEM cross-sectional micrographs performed are presented.

Introduction

Chip Scale Packages (CSPs) have their own unique form factor not seen in SMT and many of them may not be able to meet traditional reliability test requirements. Also, because of their wide usage in portable electronics, additional emphasizes have been placed on new specific tests such as bend and drop tests to meet reliability requirements for such products. The small form factor with large functionality necessitate use of area array package with small balls rigid balls not having the resistance to thermal and mechanical exposure required for these products[1-3]. However, rapidly changes in electronics have reduced life thermal cycle expectancy in favor of CSP implementation. Requirements for dynamic loading may be resolved by use of underfill even though knowing its drawbacks imposing additional costly process steps and introducing reworkability in most cases.

Although the expression "CSP" is widely used by both suppliers and users, its definition had evolved as the technology has matured. At the start of the package's introduction into the market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package, namely, the ball grid array (BGA).

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers had difficulty in building such packages whereas the users had difficulties in accommodating the need for the new microvia printed circuit board (PWB), chiefly, because of routing requirements and its increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design rather than a microvia build to avoid the elevated cost of the latter.

Thus in reality, CSPs are miniature new packages that industry has already implemented, and there are many unresolved technical issues associated with the implementation of their new version as they become available. Technical issues themselves also change as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. Now, packages with 0.4 mm pitch become available. In addition to finer pitch PWB design/assembly challenge, new package configuration including the use of flip chip die rather than wire bond and stack of die within packages will add additional complexity when the package reliability is being addressed. New unknown potential failure mechanism will add to such challenges.

CSP RELIABILITY

CSPs have their own unique form factor not seen in SMT and many of them may not be able to meet the traditional reliability test requirements. There is a paradigm shift on reliability for CSP, and new specific tests such as bend and drop tests are being adopted to especially meet consumer requirements for portable electronic products. The shift is further motivated by several factors, including the following:

- Reduction in life expectancy for consumer electronics;
- Rapid changes in electronic technology

For surface mount, solder joints have both electrical and mechanical functions, and they have traditionally been the weakest link in assembly reliability. This means that damage to the solder joints could readily affect functional integrity of the microelectronics system. Therefore, defects that cause changes either in mechanical or electrical system characteristics and understanding their reasons for failure are critical. The most common damage to solder joints are those induced by thermal cycling. Creep and stress relaxation are the main causes of cycling damage. Creep for materials generally occurs at temperatures above half of the absolute melting temperature ($T/T_m > 0.5$). This value is 0.65 at room temperature for eutectic solder(63Sn/37Pb), which implies that some creep even occurs at room temperature for solder.

Key Assembly Reliability Factors

Thermal damage to solder joints are most often induced by the following:

- Global CTE (Coefficient of Thermal Expansion) mismatch between the package and board induces stresses. The package and board can also have temperature gradients through the thickness and at surface areas
- Local CTE mismatch between the solder attachments (i.e. solder joints) of the component and the PWB

Reducing the CTE mismatch between the component and the PWB reduces cycling damage. For leaded SM package, the CTE mismatch between the solder joints and the PWB was relieved by using compliant leads. Even though area array CSPs are robust in manufacturing, their rigidity is one of the main reliability concerns.

For the thermal cycling environment, reduction in package size and therefore die size and package thicknesses improve reliability whereas ball size/height reduction has negative effect. Innovative approaches had been developed aimed at absorbing the CTE mismatch between the die and board within the package or externally through strain absorbing mechanisms, and therefore reducing stresses on the solder interconnects. These innovative approaches could introduce their own unique damage mechanisms since the weakest link may now have been transferred from solder to some other area of the attachment system.

One innovative approach uses compliant TAB leads and elastomeric materials between the die and substrate to reduce the package CTE mismatch. Since the TABs absorb the majority of the stresses, they become the weakest link and possible failure site within package. This approach has been widely shown to be effective for low I/O CSPs, but yet to be proven for higher I/O CSPs. The other innovative approach, which is called "Floating Pad Design", has potential for absorbing the global CTE mismatch, and therefore it could theoretically handle a large I/O package.

Underfill Effects on Reliability & Purpose of This Investigation

Underfill has been widely used to improve by at least an order of magnitude solder joint reliability of area array flip chip die attachments both for use in internal packages and on the PWB. Underfill absorbs the CTE mismatch and therefore reduces stress significantly by distributing stress uniformly through the solder joints. Underfilling, however, is undesirable because of the additional process requirements of cost increase and the reduction in manufacturing throughputs. Another drawback of underfill is the inability to rework defective parts. Progress has been made to reduce the negative impact of underfilling by shortening the process time by the use of snap cure polymers and enabling reworkability by the development of reworkable underfills.

So, if we assume that underfill improves reliability, then one thought might be that if everything else failed to improve reliability of CSPs, underfilling might be the ultimate undesirable solution. This approach for CSPs was used by Sony when its passport size camera was first introduced in early 1997. Investigators have shown that underfill materials and process play key role on the assembly reliability. Literature reliability data on the effects of underfill on assembly reliability are limited, especially for the effect of package types including those modified for relieving stress mismatch between die and substrate. The paper is an attempt to answer some of the key questions on the interaction of package type and underfill on thermal cycle behavior. This paper presents cycles-to-failure data for three package assemblies with and without underfills showing different reliability effects.

CSP TEST MATRIX

The test vehicle describe here was built under JPL-led MicrotypeBGA Consortium. After numerous teleconferences, meetings, and workshops, the Consortium team members agreed to concentrate on the following aspects of CSP technology and environmental testing[3].

Package I/O /PWB (printed wiring board) — Eleven packages from 28 to 275 I/Os as listed in Table 1 were used. The TSOP was used as control. The PWBs were

fabricated from FR-4 and BT (bismaleimide triazine) materials which were available in the resin copper coated form and a high temperature FR-4. The boards were double sided, standard and microvia. Four types of surface finishes were considered, the majority were organic solder preservative (OSP)

Solder Paste/Volume — Three types of solder pastes were included:

- no-clean;
- water soluble (WS);
- rosin mildly activated (RMA).

Three stencil thicknesses were included, but the majority of test vehicles had a 6 mil thickness.

Package/Test Vehicle Feature — All packages were daisy-chained, and they had up to two internal chain patterns. Packages had different pitches, solder ball volumes and compositions, and daisy-chain patterns. In most cases, these patterns were irregular and much time and effort was required for the PWB design.

The test vehicle (TV-1) was 4.5″ by 4.5″. The PWBs (TV-1) were double-sided (microvia and standard); several boards with packages on both sides were assembled. This allowed a direct reliability comparison between the standard and microvia technologies, single- and double-sided processing issues, and single- versus double-sided solder joint reliability. In designing daisy-chains, it became apparent that the standard PWB technology could not be used for routing the majority of the packages.

Underfill — Several assemblies had underfilled packages even though it was known that the packages may not require underfilling. This was done in order to better understand the impact of underfill on solder joint reliability for different CSP styles. Package O required underfill, and of these packages, the majority were underfilled. Several were not underfilled in order to better understand the reliability consequence of not using underfill for this package.

Table 1 CSP Package Configurations Matrix

Package ID	Package Style	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package. Thickness (mm)	Ball Dia (mm)
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	99	1.75	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

* All measurements are in mm unless otherwise specified

Environmental testing — Data for three different thermal cycle profiles were presented here even though additional profiles were also used. The three profiles were:

- Cycle A: The cycle A condition ranged from –30° to 100°C and had an increase/decrease heating rate of 2° to 5°C/min and dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.
- Cycle B: The cycle B condition ranged from –55° to 125°C, with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.
- Cycle C condition ranged from –55°C to 125°C, same as B range, except with a much lower ram rates of heating and cooling rates. These were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time at the minimum temperature. Each cycle lasted 159 minutes.

Monitoring — The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC 9701, Table 4-3.3.3, were used to interpret electrical interruptions [4]. In this specification, failure is defined "as the first interruption for a period of one microsecond or less and increase in daisy chain resistance of 1,000 Ω or more, and afirmation of the failure for nine or more additional events within 10% of the cycles to initial failure." In general, it is expected that once the first interruption is observed, there will be a large number of additional interruptions within the 10% of the cycle life. Failures detected by continuous monitoring

were verified manually at room temperature (RT) after subsequent removal from the chamber for failures verification..

ENVIRONMENTAL TEST RESULTS

A large number of assemblies have already failed, and their cycles to failure have been documented. Out of these, cycles to failure data for a few under four thermal cycling conditions are reviewed. Results for two chip-on-flex, leadless with and without underfill, and leaded TSOP assemblies are presented.

Cycles-to-failure Cummulative and Weibull Plots for B 28I/O, Leadless without underfill

Figure 1-2 show cycles to first failures for three package types. To generate the plots, the CTFs were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$.

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull equation is[5]

$$F(N) = 1 - \exp(-(N/No)^m)$$

where

F(N)	is the cumulative failure distribution function
N	is the number of thermal cycles
No	is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63.2% failure occurrence.
m	is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by 1.2/CV; that is, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line defines the Weibull shape parameter. The cycles-to-failure data in log-log can be fitted to a straight line to calculate the two Weibull parameters.

Cycles-to-Failure for Assemblies w/wo Underfill to Combined 3,00 A and 1,500 B conditions

CTFs test results for assemblies with underfill were analyzed and compared to standard assemblies without underfill. Three categories based on their impact on reliability were identified: (1) improvement by underfilling, (2) minimal effect, and (3) degradation due to underfilling. Test results to 3,000 cycles under A condition (-30/100°C) are summarized in Table 2 and presented in Figures 3-4. These are further discussed in the following.

(1) Degradation by underfilling

CTFs for package F, TAB CSP-1, with 46 I/Os under A and B thermal cycle conditions are summarized in Table 2. Under both cycle conditions, assemblies with underfills showed much lower CTFs than those with no underfills. Assemblies showed no failure to 3,000 under A condition, whereas the assemblies with underfills failed at 996, 1385, 1727, and <2000 cycles. Note that the TAB CSP package decouples the die CTE mismatch by use of a stress dampening elastomeric materials layer and flexible TAB lead interconnects.

(2) Minimal impact by underfilling

CTFs for package G, chip-on-flex, with 99 and package M with 206 I/Os with and without underfill under B condition were less than 200 cycles, shown in Figure 1. Three datum points for assemblies with underfill are also plotted. These limited data indicate that improvement due to underfilling for this package with two I/Os is almost insignificant when cycled under a near thermal shock condition.

(3) Improvement by underfilling

CTFs for package B, leadless, 28 I/O without underfill under A (-30° to 100°C) and B (-55 to 125°C) thermal conditions are shown in Figure 2.

As expected, cycles to failure increased as temperature cycling range decreased. CTFs for B condition ranged from 372 to 546 with an $N_{63.2\%}$ (No) of 465 and an m Weibull value of 7.2. For A condition, it ranged from 641 to 1007 cycles with an $N_{63.2\%}$of 839 cycles and an m value of 7.5.

Results for four (4) test vehicles with underfills are also shown in Figure. Under B thermal cycle condition, underfilled assemblies showed only one failure at 1374 cycles when they were subjected to a total of 1,500 cycles. Under condition A, no failure was observed for the underfilled assemblies to a total of 3,000 cycles. These limited test results clearly indicate significant improvement that can be achieved by underfilling for this category of peripheral leadless package.

Thermal cycling under A and B condition for assemblies with no underfill stopped after completion of 3,000 and 1,500 cycles, respectively. For the four assemblies with underfills, however, further thermal cycling were performed to establish their long-life behavior. A more severe temperature cycling, condition C, was used to accelerate failures. Results are summarize below.

Table 2 Assemblies with and without underfill comparison

Package & thermal cycle condition	No Underfill Number and cycles to failure	With Underfill Number and cycles to failure
Package F, TAB CSP, -55°C to 125°C, B, 1,500 Cycles	3 out of 10 failure at 709, 896, and 1,380 cycles	3 out of 3 failures at 32 (?), 142, 710 cycles
Package F, TAB CSP-1, -30°C to 100°C, A, 3,000 cycles	No failure (15 assemblies)	4 out of 4 failure at 996, 1385, 1727 , and <2000 cycles

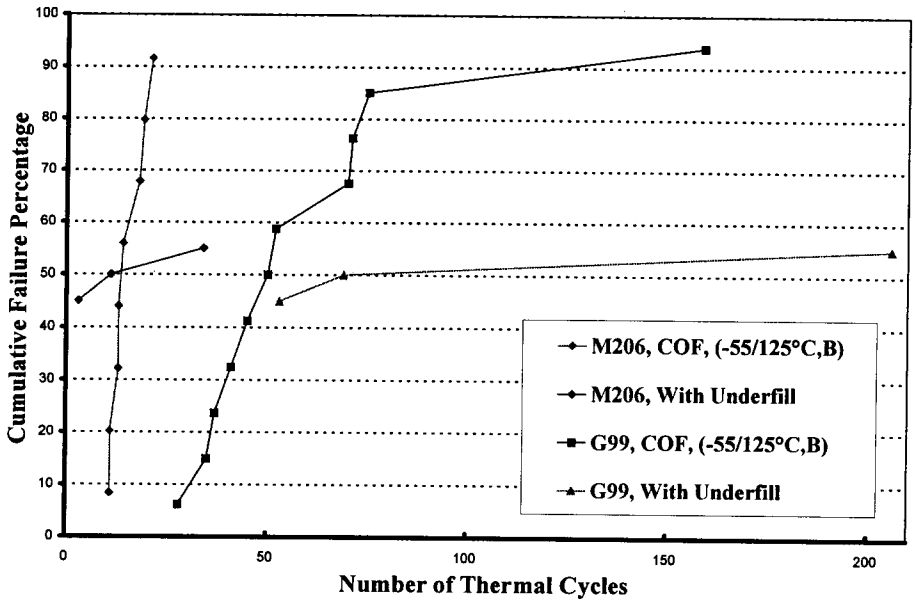

Figure 1 Cycles-to-failure for chip-on-flex assemblies with and without underfill

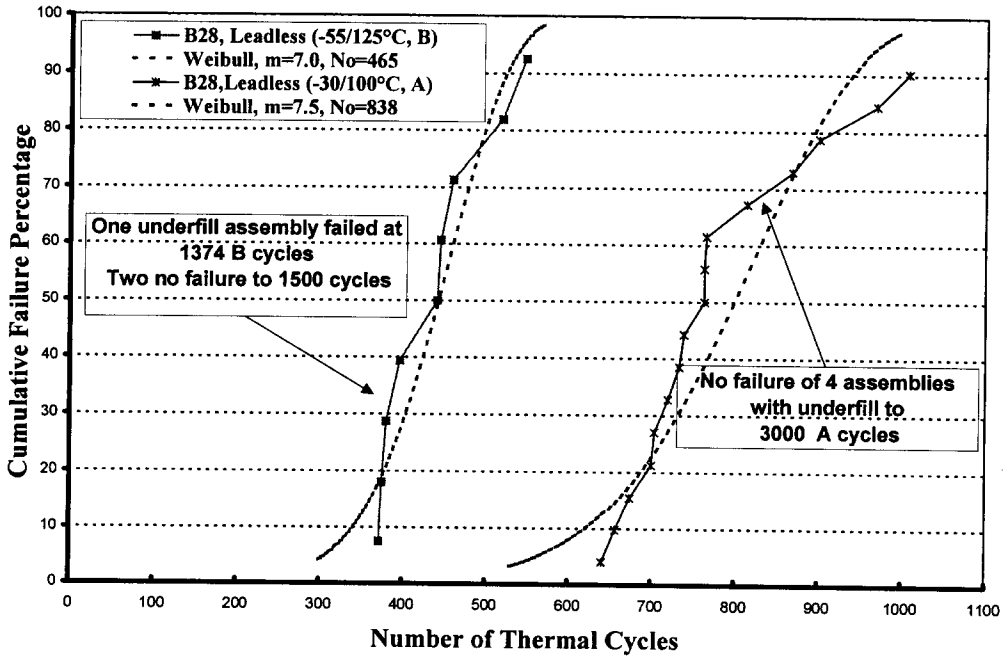

Figure 2 Cycles-to-failure for a 28 I/O leadless package without and with underfill and their Weibull distribution parameters

CTFs for Assemblies with Underfill to 3887 Combined Cycles (3,000 A plus 887 C conditions)
Thermal cycling for four underfilled assemblies that mostly showed no signs of failures were continued to 887 additional cycles. CTFs for these were documented and data for two leaded and leadless package assemblies are presented below.

CTFs for B28 I/Os, Leadless — For B28I/O, one of assembly showed signs of first interruption at 3443 cycles, when it was checked at RT at 3,500 cycles a resistance value of 7.1 Ω, slightly higher than it original value of 2.8 Ω. The number of interruptions for this assembly become significantly large at 3545 cycles and an open was registered at 3887 cycles at RT, checked by a meter. So, based on the IPC definition, the failed cycle for this part assumed to be 3443 cycles. Microsectionning was performed to determine the failure mechanisms. The resistances for the other three were 2.6, 5.9, and 2.6 ohms at RT after a total of 3887 combined cycles. The one with a higher resistance value is expected to fail next if thermal cycling was further continued.

CTFs for TSOP 44 I/Os — For TSOPs, the fist assembly was underfilled as a control sample to determine the effect of underfilling on leaded package even though generally these packages are not underfilled for most benign commercial application. Large leaded packages may be required to be underfilled (staking) for high reliability applications when resistance to dynamic loading also is required. The underfilled TSOP was one of a few TSOPs out of more than 100 assemblies that showed signs of failure relatively early. The first open was observed at 1501 cycles at 89°C and failure established. The sluggish interruptions were continued to 3417 cycles with a complete failure establishment at 3,500 cycles at RT. The other 3 TSOP assemblies with no underfills showed resistance of 6.8,75.4, and 6.8 ohms at RT after 3887 combined cycles. The one with high resistance value assumed to be near its failure. Visual observation and cross-sectioning was performed to establish failure mechanisms in comparison to the underfilled one.

Cycling Damage Inspection at 3887 Combined cycles (3,000 A plus 887 C conditions)
Inspection was performed by visual and scanning electron microscopy (SEM) prior to and after destructive cross-sectioning to better characterize failure mechanisms.

Inspection TSOP 44 I/Os W/WO Underfill — Visual inspection was performed only for the TSOPs without underfill. The SEM photo prior to and after cross-sectional microscopy for this TSOP is shown in Figure 5. Even for this assembly, no clear signs of failure could be identified when it was inspection by SEM prior to destructive testing because damages were covered by no-clean residual fluxes. Destructive microsection photographs show that the corned solder joints are almost fully cracked with no complete failure yet. Signs of grain growth in the areas of cracking is also apparent. Resistance value for this assembly was 6.8 Ω prior to destructive test.

SEM cross-sectional microscopy for a TSOP with underfill is shown in Figure 6. Solder joint grain quality of corner leads were almost untouched by a long-time cycle exposure. Except for a slight grain growth in the vicinity of lead hill and under the lead, there are no signs of microcraking damage in solder joint materials. So, electrical failure observed in early cycles could not be explained by solder joint failure.

Failure however is apparent for the microvia shown in Figure 7. Microvia failure at both corner lead sites were shown in this Figure. Failure is a separation of RCC layer of microvia from the board. Also, it appears that solder filled vias show identical failure mechanism to those with no solder fill

Inspection for B 28 I/Os with underfill — SEM cross-sectional photographs are shown in Figure 8. Except for a slight solder grain growth similar to the TSOP with underfill, no signs of damage are apparent. Figure 9 shows photos at much higher magnification focusing on the two microvia sites. Similar to the TSOP with underfill, microvias show clear signs of failure for both vias with and without solder fills.

CONCLUSIONS

- Cycles to failure for the same assembly under four different environments were different, but the trends were as expected, i.e., as temperature cycling ranges increased, cycles to failure decreased.
- Underfill effects on cycles to failure may be positive, neutral, or negative depending on package types. It improved the reliability of leadless package, was neutral for chip-on-flex, and had negative effects on the TAB CSP reliability.
- Failure mechanisms may shift to the weakest package assembly (PWB/solder/package internal) sites when the solder failure prevented by underfilling. The TAB CSP failure shift to internal package and TSOP and Leadless package assembly failed from in-pad microvias, filled or unfilled with solder.

ACKNOWLEDGMENTS

The majority of research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to acknowledge the in-kind contributions and cooperative efforts of the JPL MicrotypeBGA/CSP consortia. Special thanks to Anarosa Arreola, Faisal Masood, and Ken Evans at JPL for environmental test and SEM support; E. Siméus, S. Stegura, R. Smedley, Raytheon (retired); N. Kim, Boeing; A. Chen, Celestica; and other team members who have made contributions to the progress of this program.

REFERENCES

1. Fjelstad, J., Ghaffarian, R., Kim, YG., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002)
2. Ghaffarian, R.,"Chip Scale Package Assembly Reliabity", Chapter 23rd in *Area Array Interconnect Handbook* (Kluwer Academic Publishers, edited by Karl Puttlitz, Paul Totta, 2002)
3. Ghaffarian, R, et al. "CSP Consortia Activities: Program Objectives and Status," Surface Mount International Proceedings, August 23-27, 1998, pp. 203-230
4. IPC 9701,"Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments". Published by IPC, Association Connecting Electronics Industries
5. O'Connor, Patrick D. T., "Practical Reliability Engineering, Third Edition, John Wiley & Son, Chichester, Great Britain, 1996

Figure 3 Optical and SEM photomicrographs of a TSOP corner leads after 3, 887 combined cycles (3,000 cycles of A and 887 cycles of B conditions)

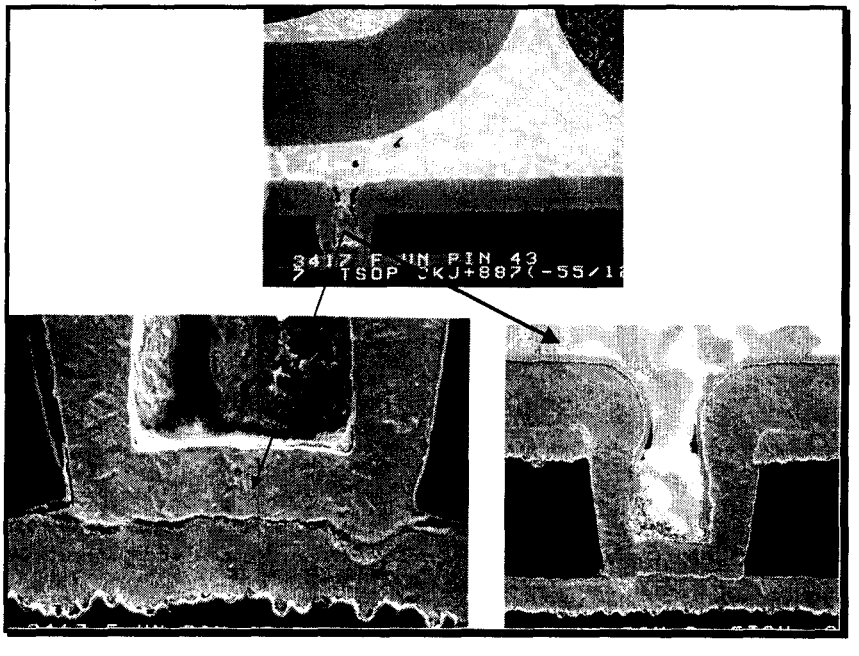

Figure 4 SEM photomicrographs of PWB microvia failures under TSOP corner leads after 3,887 combined cycles (3,000 cycles of A and 887 cycles of B conditions)

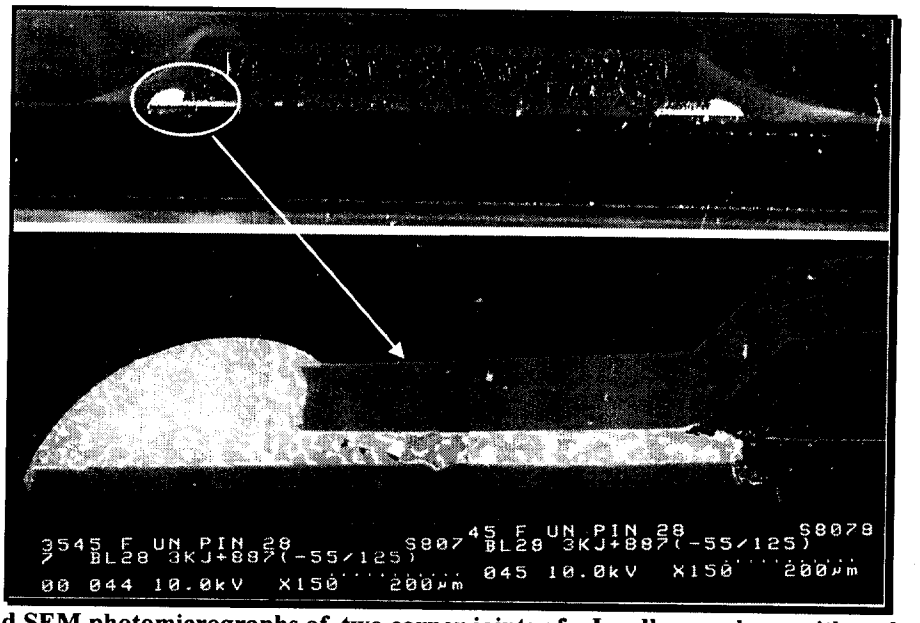

Figure 5 Optical and SEM photomicrographs of two corner joints of a Leadless package with underfill at 3, 887 combined cycles (3,000 cycles of A and 887 cycles of B conditions)

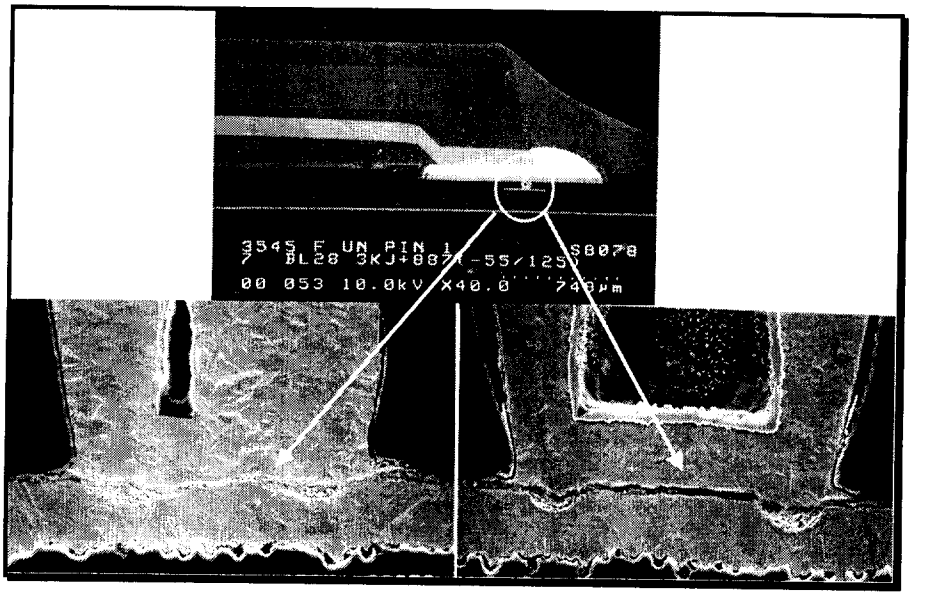

Figure 6 SEM photomicrographs of PWB microvia failures of corner solder joint for leadless package at 3,887 combined cycles (3,000 cycles of A and 887 cycles of B conditions)