

CSP and BGA Assembly Reliability in a Fast Ramp Rate Thermal Cycle Environment

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Abstract

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of team members representing government agencies and private companies, recently joined together to pool in-kind resources for developing the quality and reliability of mixed area array technology, chip scale packages (CSPs) and ball grid arrays (BGA), for a variety of projects.

The Consortium assembled fifteen different packages with I/Os from 48 to 784 and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring board (PWB). These test vehicles (TV-2) were subjected to numerous thermal cycling conditions including -55°C to 125°C with a near thermal shock condition. Cycles-to-failure (CTF) test results to 1,500 cycles under this condition are compared for 784 I/O FCBGA, 175 I/O FPBGA, and 313 I/O PBGA. Inspection results along with SEM and optical cross-sectional photos revealing damage and failure mechanisms will also be presented.

Introduction

Both BGAs and CSPs (fine pitch BGAs (FBGAs)) are now widely used for many electronic applications including portable and telecommunication products. Their usage, especially the BGA version now started to be implemented for high reliability applications with a more unique requirements. The BGA version of area array package introduced in late 80's and implement with great caution in early 90, was further evolved in mid 90's to CSP with much finer pitch. Now distinguish between size and pitches become blare for the array version and being categorized as area array package distinguishing the package category with the flip chip bare die version. The bare die has been around for a longer time and their associated issues especially direct attachment to printed wiring board (PWB) is yet to be fully resolved.

CSP definition has evolved as the technology has matured and refers to a package with 0.8mm pitch and lower, now as low as 0.4 mm pitch. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of microvia PWB which is costly and they may perform poorly when they are assembled onto boards. One approach has been to increase function through systems-in-package, i.e., stacking die/package in the height keeping the pitch with the board technology limitation.

Extensive work has been performed in understanding technology implementation and reliability issues from BGA to CSPs by the JPL Consortia. Lessons learned by the team have been continuously published and presented in previous SMTAI conferences and recently published in book chapters [1-5].

For the most recent test vehicle, TV-2, the Consortium team jointly concentrated their efforts on building the second test vehicle (TV-2) with fifteen (15) packages of low to high I/O counts (48 to 784) and pitches of 0.5 mm to 1.27 mm. In

addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. Some of the test results for these test vehicles published by the team previously [1-2]. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effects of PWB build and manufacturing variables.

The joint Consortium test vehicle, herein refers to TV-2, was assembled by three manufacturers in a high, medium, and low volume manufacturing environment. The printed wiring Board for these assemblies were also came from two sources. circuit board for these assemblies. Second level board reliability characteristics of these assemblies were investigated to understand the effects of package types as well as many manufacturing parameters on solder joint reliability.

This paper presents the thermal cycling test results to 1,500 cycles (-55 to 125°C) under a fast rates for a number of TV-2 assemblies that were exposed to such environment. Failure results are compared to those performed under the same temperature range, but slower rate. Failure analysis by destructive and non-destructive performed to verify failure and understand their mechanisms will also be presented.

CSP TEST MATRIX

Test Vehicle Package I/O /PWB

TV-2 Test Vehicle/Package types and I/Os /PWBs — Fifteen packages from 48 to 784 I/O as listed in Figure of an assembly photo were used. The TSOP (U3) was used as a control for both assembly robustness and environmental reliability comparison to BGAs and CSPs. The PWBs were fabricated from FR-4 materials with 6 layers. Microvia design with 3 mil vias was considered for all packages except for the 784 I/O flip chip BGA (U14) in one design. In another design, estimated optimized PWB pads with 3 mil microvias were used. PWBs were made at two facilities, one with large production capability (PWB-A), and the other one at that time

with a more concentrated supplier capability (PWB-B). The boards build from the latter company included organic solder preservative (OSP) surface finish as well as a very limited number of other surface finishes including hot air solder level (HASL), immersion Au/Ni, and immersion silver.

PWB/Package/Test Vehicle Features — Figure 2 shows a section of PWB with microvia and pad configuration for package with different pad sizes. This photo include design for packages with 0.5, 0.8, 1.0, and 1.27 mm. Pad sizes varied between 0.25 mm to 0.66 mm for pitches from 0.5 to 1.27. Note also the calibration traces with close proximity to the package pads. These traces were designed to be used as reference surfaces for the automatic solder paste measurement a requirement for a 3D laser solder paste volume measurement system. Pad covered with solder paste could not be used as reference for such measurement when they are covered with paste to be characterized. In addition, two series of microvias similar to those for pad packages were designed on PWB. These microvias formed in two daisy chains with probing pads for manuall monitoring.

Packages had different pitches, solder ball volumes and compositions, and daisy-chain patterns. All packages were daisy-chained, and they were divided into several internal chain patterns. In a few cases, the daisy chain patterns were irregular and much time and effort was required for the PWBs design to match package patterns. The daisy chain pattern on PWB complete the chain loop into the package through solder joints. Several probing pads connected to daisy chain loops were added for failure site diagnostic testing. The package and PWB daisy chains for a 60 I/O wafer level redistributed CSP (U6) and a 208 I/Os FPBGA (U13) are shown in Figure 3.

The test vehicle (TV-2) was 4.5" by 4.5" and divided into four independent regions. For single-sided assembly, most packages can be cut out for failure analysis without affecting the daisy chains of other packages.

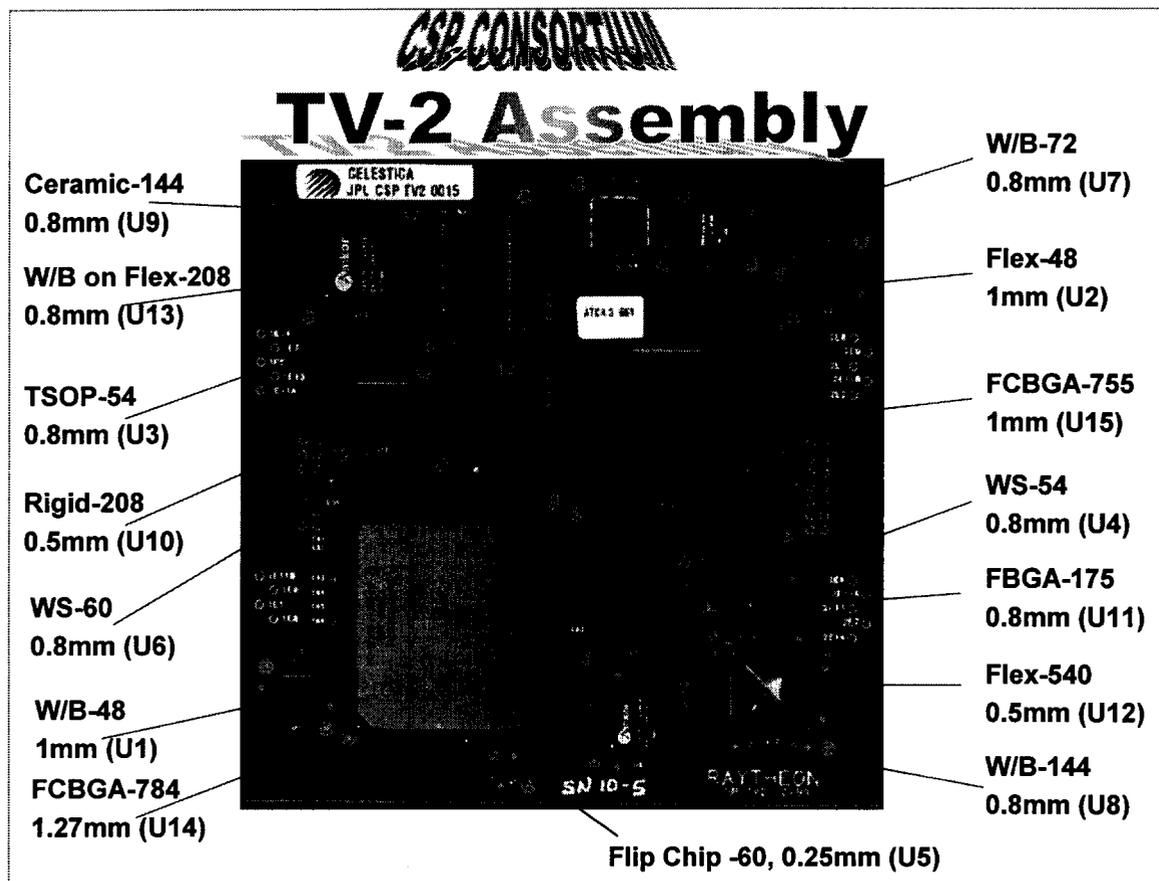


Figure 1 JPL Consortium second test vehicle design (TV-2) with flip chip BGA packages (U14) to flip chip die (U5), all in one board

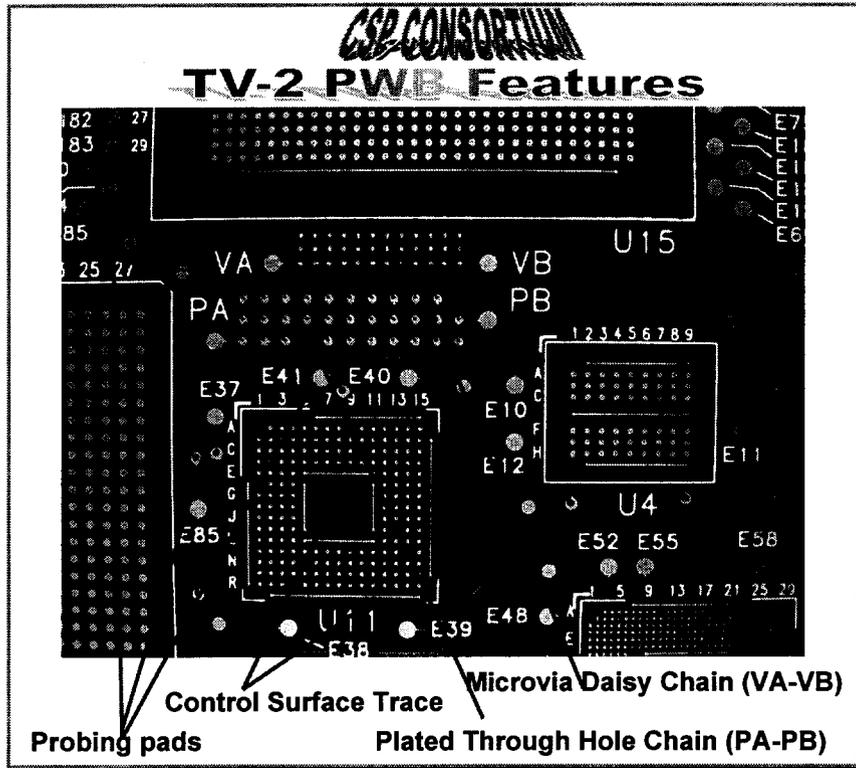


Figure 3 Printed Wiring Board (PWB) showing representative control surface trace for solder volume measurement, probing pads for failure diagnostic, PTH and microvia daisy chain patterns

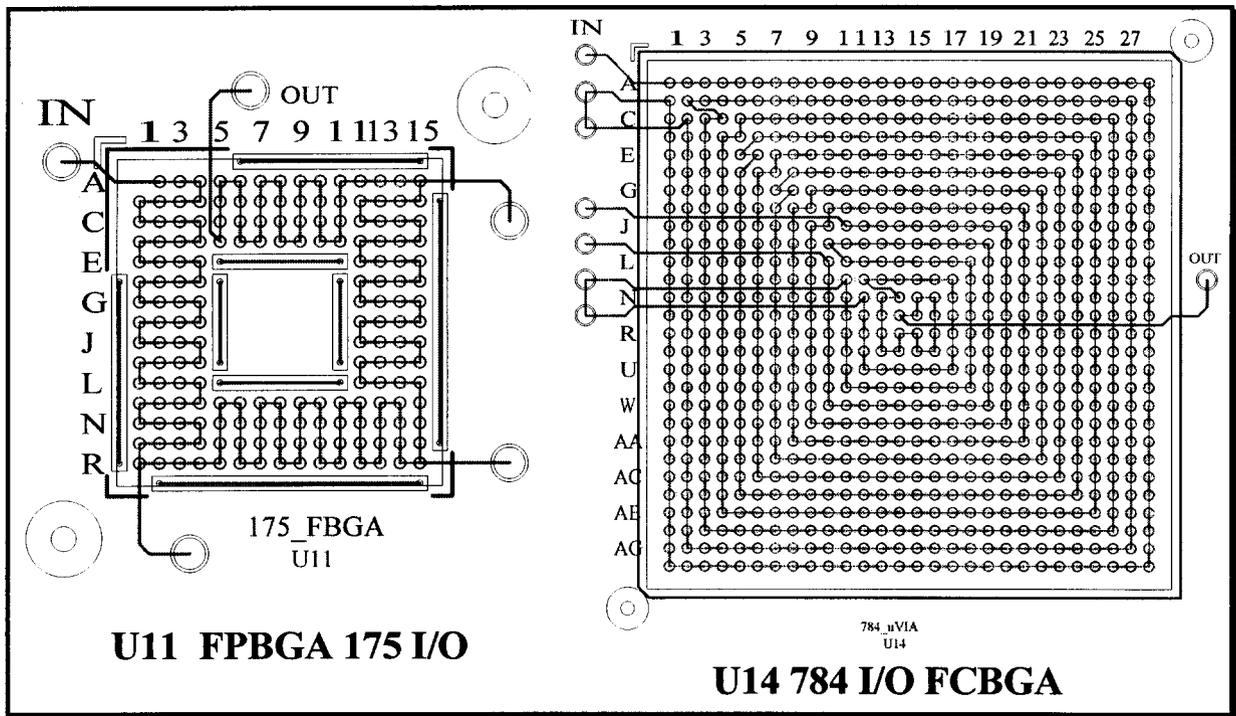


Figure 3 Package and board daisy chain patterns for a TV-2 flip chip BGA (FCBGA) and fine pitch BGA (FPBGA) with probing pads for failure diagnostics

Run	Assembly ID	PWB ID	PWB Level	Stencil Type	Stencil Thickness	Build Time	Cycle Profile	U1	U5	U14 Inner	U14 Outer	U3	U6	U13	U9	U7	U8	U11	Microvia and PTH Daisy Chain
1	SN/002	203-01	P1A	Laser Efab	6 mil	10-Feb	B	OPEN	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OK	V & P OK
2	SN/007	204-08	P1A	Laser Efab	6 mil	10-Feb	B	OK	OK	OK	OK	OK	OPEN	OK	OK	OPEN	OK	OK	V = OPEN (1500 Cyl
3	S/N008	203-10	P1A	Laser Efab	6 mil	10-Feb	B	OK	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OK	V & P OK
4	S/N031	203-09	P1A	Laser Efab	6 mil	5-Apr	B	OK	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OK	V & P OK
5	SN/052	204-09	P1A	Laser Efab	5 mil	17-Apr	B	OK	NA	OK	OK	OK	OPEN	OK	OK	OK	OK	OK	V & P OK
6	SN/111	204-10	P1A	Laser Efab	5 mil	20-Sep	B	OK	OK	OK	OK	OK	OPEN	OK	OK	OPEN	OK	OK	V & P OK
7	S/N024	201-05	P1B	Laser Efab	6 mil	5-Apr	B	OK	OK	OPEN	OK	OPEN	OPEN	OK	OPEN	OK	OK	OK	V = OPEN (1500 Cyl) P=OK
8	S/N026	201-04	P1B	Laser Efab	6 mil	5-Apr	B	OK	OK	OK	OK	OK	OPEN	OK	OPEN	OK	OK	OK	V & P OK
9	S/N029	201-03	P1B	Laser Efab	6 mil	5-Apr	B	OK	OK	OPEN	OK	OPEN	OPEN	OK	OPEN	OK	OK	OK	V & P OK
10	S/N101	3-OSP	P2	Laser Efab	5 mil	20-Sept	B	OPEN	NA	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	V & P OK
11	S/N102	1-OSP	P2	Laser Efab	5 mil	20-Sept	B	OPEN	NA	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	V & P OK
12	S/N 001	199-07	P1A	Laser Efab	6 mil	10-Feb	A	OK	OK	OK	OPEN	OK	OPEN	OPEN	OPEN	OK	OPEN	OPEN	V & P OK
13	S/N 004	206-08	P1A	Laser Efab	6 mil	10-Feb	A	OK	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OPEN	V & P OK
14	S/N 005	204-11	P1A	Laser Efab	6 mil	10-Feb	A	OK	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OK	P = 23 Ohms (625 cycles)
16	S/N 006	209-01	P1A	Laser Efab	6 mil	10-Feb	A	OPEN	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OPEN	V & P OK
16	S/N0 22	209-11	P1A	Laser Efab	6 mil	5-Apr	A	OK	OK	OK	OK	OK	OPEN	OPEN	OPEN	OK	OPEN	OK	V & P OK
17	S/N027	201-11	P1B	Laser Efab	6 mil	5-Apr	A	OK	OK	OK	OK	OK	OPEN	OK	OPEN	OK	OPEN	OK	V & P OK
18	S/N0 28	201-06	P1B	Laser Efab	6 mil	5-Apr	A	OK	OPEN	OK	OK	OK	OPEN	OK	OK	OK	OPEN	OK	V & P OK
19	S/N 099	16-OSP	P2	Laser Efab	5 mil	20-Sept	A	OPEN	OPEN	OPEN	OPEN	OPEN	(Pkg-Mod) OK	OPEN	OPEN	OK	OPEN	OPEN	V & P OK
20	S/N 100	20-OSP	P2	Laser Efab	5 mil	20-Sept	A	OPEN	OPEN	OPEN	OPEN	OPEN	(Pkg-Mod) OK	OPEN	OPEN	OPEN	OPEN	OPEN	V & P OK
21	S/N 110	5-OSP	P2	Laser Efab	5 mil	20-Sept	A	OPEN	OPEN	OPEN	OPEN	OK	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	V & P OK

Table 1 A cross section of designed experiment matrix detailing the number of runs, levels, and package/assembly failures at 625 cycles for both A and B conditions The package/PWB daisy chain for the 280 I/O FPBGA is shown on the bottom right.

Run	Assembly ID	PWB ID	PWB Level	Stencil Type	Stencil Thickness	Via U14	Via U11	U14 Inner	U14 Outer	U11	S/N U14/U11	S/N U14	S/N U11
1	SN/002	203-01	P1A	Laser Efab	6 mil	PTH	Micro	1476	OK	1130			
2	SN/007	204-08	P1A	Laser Efab	6 mil	PTH	Micro	1489	OK	1231			
3	S/N008	203-10	P1A	Laser Efab	6 mil	PTH	Micro	1372	OK	1057			
4	S/N031	203-09	P1A	Laser Efab	6 mil	PTH	Micro	1400	OK	981			
5	SN/052	204-09	P1A	Laser Efab	5 mil	PTH	Micro	OK	1251	1220			
6	SN/111	204-10	P1A	Laser Efab	5 mil	PTH	Micro	1463	OK	1053			
7	S/N024	201-05	P1B	Laser Efab	6 mil	PTH	Micro	609	733	691			
8	S/N026	201-04	P1B	Laser Efab	6 mil	PTH	Micro	787	808	1003			
9	S/N029	201-03	P1B	Laser Efab	6 mil	PTH	Micro	829	607	1048			
10	S/N101	3-OSP	P2	Laser Efab	5 mil	Micro	Micro	96	37	96			
11	S/N102	1-OSP	P2	Laser Efab	5 mil	Micro	Micro	202	117	99			

Table 2 A cross section of Table 1 for flip chip BGA (U14) and fine pitch BGA (U11) with specific failure cycles under thermal cycle B condition to 1,500 cycles

Test Vehicle Build and Test Matrix

Design of experiment was used to toggle many variables including control packages and if they were modified in a later stage of assembly, board fabricator and build serials for the fabricator, board surface finish, manufacturing parameters including stencil type and solder volume, test vehicle assembler, single and double sided assembly, and temperature cycling ranges and monitoring performed at different team member facilities.

TEST CONDITIONS

Thermal Cycling test

Thermal cycling was performed in the range of -55°C to 125°C under two different conditions. Chamber setting and

thermal couple readings for conditions A and B are shown in Figure 4 and 5, respectively. For condition A, the heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time duration at the minimum temperature. Each cycle lasted 159 minutes.

The near thermal shock cycle, condition B, had the same temperature range performed in a chamber with three regions of hot, ambient, and cold. Heating and cooling rates were nonlinear and varied averaging between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

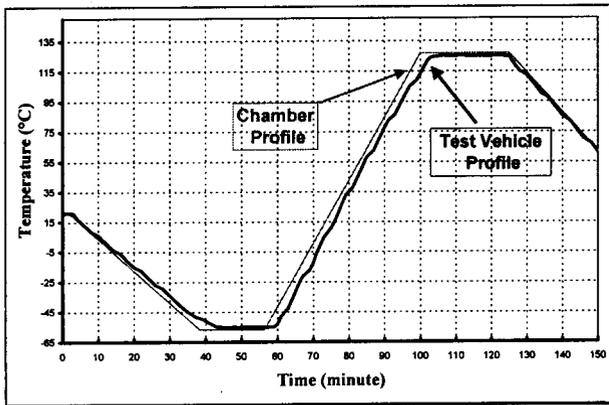


Figure 4 Thermal cycle profile in the range of -55°C to 125°C , condition A, 159 minutes/cycle

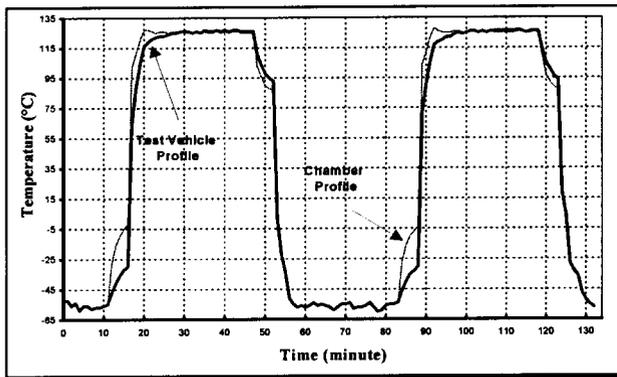


Figure 5 Near thermal shock profile in the range of -55°C to 125°C , condition B, 68 minutes/cycle

Monitoring

The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC 9701, Table 4-3.3.3, were used to interpret electrical interruptions. In this specification, failure is defined “as the first interruption for a period of one microsecond or less and increase in daisy chain resistance of $1,000\ \Omega$ or more, and a firmation of the failure by nine or more additional events within 10% of the cycles to initial failure.” In general, it is expected that once the first interruption is observed, there will be a large number of additional interruptions within the 10% of the cycle life. Failures detected by continuous monitoring were verified manually at room temperature after subsequent removal from the chamber for failures verification.

Thermal Cycling Results

Design of Experiment Test Matrix

Table 1 shows a small cross-section of design of experiment used in this evaluation for a limited number of experiment. Since the current accumulated thermal cycles data under condition A is continued only to 625, the failed condition for both profiles A & B (near thermal shock) were tabulated for this total number of cycles. Note however that the daisy chain values for microvia and plated through hole (V and P) are those measurement that were carried at room

temperature (RT) after 625 and 1,500 cycles of A and B conditions.

The first column of this table, provide the twenty (21) runs for ease of data comparison purpose and they do not represent the desing of experiment (DOE) runs. Assembly IDs, e.g. S/N001, are used for tracking systems documenting all PWBs, assembly process and defect identification, inspection, and thermal cycling test results. The internal vendor board identifications based on a panel build are listed under PWB ID column. Two PWB manufacturer were used, P1 and P2. For one case board identification further subdivided into A and B (eg., P1A and P1B) based on the trend observed after evaluating the thermal cycle test results under condition B. There was no specific DOE run for this purpose, this is a division level based on the observed trend after the test. The Run 1-6 used for thermal cycling under condition B and 17-18 for A condition are the rusns with P1B that hypothesised to have some anomaly associated with the PWBs. The second vendor identification is clerly different and they are under runs 10,11, 19, 20, and 21, shown in italic for clarity.

Manufacturing condition including time of assembly and stencil thickness and types are shown under the subsequest columns. The failed conditions were identified as Open for daisy chain open at 625 cycles and no-failure (OK) for U1, U3, U5-U8, U11, U13, and U14 (both inner and outer row daisy chains), are shown in the subsequent columns. Details package information and their relative sizes for the U sites are shown in test vehicle photo in Figure 1.

Discussion on Trends in Failure at 625 Cycles for Thermal Cycle Under A & B Conditions

Several trends identified based on the limited test results listed in Table 1 are noted below:

- There is an overall clear difference between the number of failures for those assembled using P1 or P2 manufacturing houses. Forty seven (47) out of 50 assemblies listed in Table 1 failed to 625 thermal cycles under both A and B conditions. Inspection prior to assembly of P2s, revealed that these boards were not as high quality as those generally observed for the P1 manufacturer.
- There is some indication that the P1s with the start of 201 serial number show a declined quality. This is to be further discussed when test results for B condition is discussed.
- Most microvias and plated through hole (PTH) vias included in daisy chains survived both 625 and 1,500 cycles of A and B conditions, respectively. Out of 21 boards, only two (Run 1 and 7) showed open microvia failures to 1,500 B condition and one plated through hole showed a slight increase in daisy chain resistance (Run 14). However, even this small number of failures are from the P1 fabricator with a better board quality rather than P2 with a declined quality. The cause for this discrepancy is yet to be verified for other test vehicles.

- The U6 is the package assembly with the most number of failures. The limited number of test results with its modified version (run 19 and 20), however, shows significant improvement. This is yet to be fully verified.
- The small form factor package U1 and U7 from the same package manufacturer showed excellent solder joint reliability.
- Even though there were significant challenges to produce a good PWB pad configuration for the flip chip die with 250 micron pitch (U5), however, they showed excellent reliability when they showed good via placement and mask definition and were also underfilled after assembly.
- Both BGAs and FPBGA from the same manufacturer (U14) and (U11), both showed good reliability. Other FPBGAs (U7, U8, U13) showed a declined CTFs
- Most TSOPs, used as control package, assembled on good quality board survived 625 cycles indicating consistency manufacturing control parameters.
- There is some indication that when stencil thickness decreased to 5 mil some improvement was observed for FPBGA package when comparing the test results for Run 1-4 to Runs 5-6 for U8, U9, and U13. This is yet to be further verified using statistical approach.
- Other trends may become apparent as further CTF data are gathered.

Cycles-to-failure Trend for FCBGA and FPBGA to 1,500 B condition and Signal-to-Noise Calculations

Table 2 lists cycles-to-failure (CTF) data for a smaller cross-section of Table 1. This table provides detail information on 784 I/O FCBGA, 1.27 mm pitch, and 175 I/O FPBGA, 0.8 mm pitch, including via type, PTH or microvia, and CTF to 1,500 cycles under B condition.

CTF test results markedly clarify the significant difference between PWB manufacturer one and two (P1 and P2). The signal-to-noise (S/N) ratio difference for P1 and P2 is equal to $P1-P2 = 27.47$ standard deviation. Difference between CTF for FCBGAs built on P1A and P1B are significant, a difference of 5.13 standard deviation. This difference, however, is not the case for FPBGA (U11). Only an S/N of 3.19 was calculated, not large enough to provide a high confidence that the two test results came from two different CTFs.

Cycles-to-failure Cumulative and Weibull Plots for FCBGA and FPBGA to 1,500 B condition

Figure 6 shows cycles to first failures for FCBGA 784 I/O and 175 I/O FPBGA of TV-2 assemblies. For comparison, data for a wire bond BGA is also plotted. To generate the plots, the CTFs were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$.

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull equation is [7]

$$F(N) = 1 - \exp(-(N/N_0)^m)$$

where

- F(N) is the cumulative failure distribution function
- N is the number of thermal cycles
- N_0 is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63.2% failure occurrence.
- m is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by $1.2/ CV$; that is, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line defines the Weibull shape parameter. The cycles-to-failure data in log-log can be fitted to a straight line to calculate the two Weibull parameters.

The Weibull cumulative failure distribution was used to fit the experimental CTF data for only for 175 FPBGA data since data for BGA showed two distinct distributions. Weibull parameters for nine FPBGA assemblies of FPBGA were 1126 for N_0 and 6 for m. Distribution became much more uniform with an increase in m value to 11 if one low data set for FPBGA was not considered in the Weibull calculation. For comparison, CTF data for a wire bond plastic BGA, investigated in a previous JPL Consortium under the same condition B also included in plots. The plastic package was a depopulated full array package.

Comparison of CTF (-55/125°C) to Literature CTFs (0/100°C)

Table 3 compares the above CTFs for 175 I/O FPBGA to CTF literature data generated for solder joint reliability in the range of 0°C to 100°C thermal cycle condition [8]. The paper provides an in-depth characterization of the effect of package configuration and rework on reliability for both single and double-sided test vehicles. Comparison was performed for only for their data on a new modified package that had a substrate thickness of 0.25 rather than the previous version with 0.11 mm thickness. An acceleration value of 3.8 was calculated when the two data sets are compared. This is a reasonable value since there are many differences including significant differences in the two thermal profiles as well as printed board design and thickness.

Cycling Damage Inspection

Visual and scanning electron microscopy (SEM) inspection prior to destructive cross-sectional characterization and after cross-sectioning were performed as much as possible to better define failure mechanisms. An example of SEM photos for FCBGA is shown in Figure 7.

Conclusions

These conclusions are based on a limited number of TV2 test vehicles subjected to 625 thermal and 1,500 A and B near shock cycles in the range of -55°C to 125°C. Addition thermal and mechanical cycling data with their failure analyses are being gathered to further define the effects of various parameters on assembly reliability.

- Cycles-to-failures data for a 784 I/O full array FCBGA were between 1251 to 1489 cycles (condition B) in the best case board and assembly condition. This range was reduced 607-829 cycles for another set of board from the same manufacturer. CTFs for this package were lower than a lower I/O (313 I/Os) depopulated full array wire bond BGA.

- The CTF data for a 175 I/O FPBGA were between 691 to 1231 cycles. The trend was the same to those reported in literature for the identical package with the new thick substrate.
- CTF data generate for these assemblies using a second board manufacturer were poor, statistically identified by signal-to-noise ratio, for both cycle A and B conditions. The trend data appears to be in agreement with qualitative inspection observation for warpages. No specific numerical surface distribution were gathered for distribution characterization for each board in order to correlate them with CTF results. This will be considered in future activities.

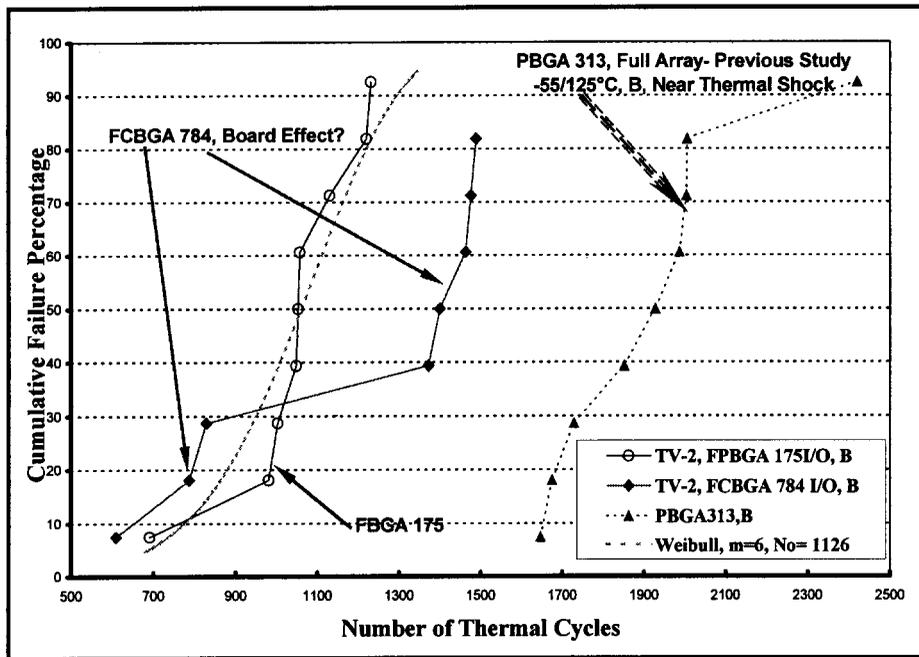


Figure 6 Cumulative Failure Distribution for FCBGA and FPBGA under thermal cycle B condition to 1,500 cycles. Data for wire bond BGA form a previous investigation also included for comparison

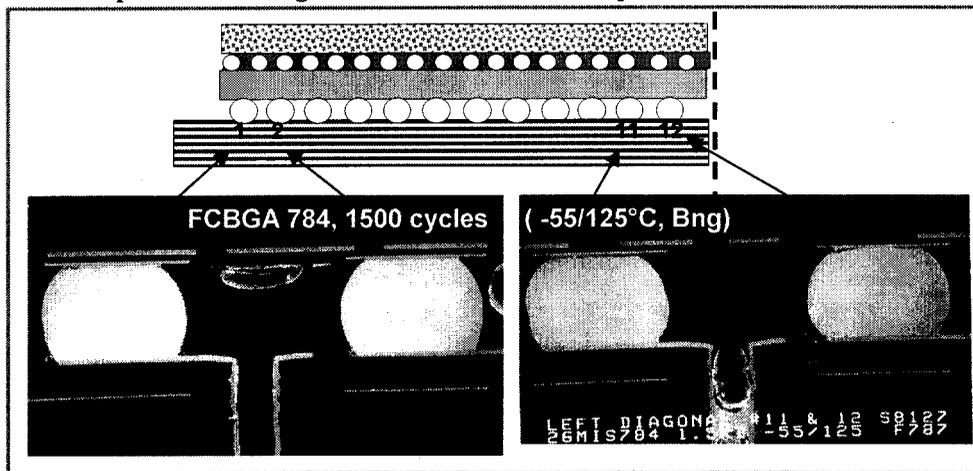


Figure 7 SEM photomicrographs of FCBGA 784 I/O (diagonal cross-section) after 1,500 thermal cycles B condition showing clear failure at the center locations (ball 11 and 12)

Table 3 Comparison of TV-2 FPBGA thermal cycle test results (-55/125°C, B) to literature data for 0 to 100°C thermal cycle range

TV ID	Board Thickness (NSMD Pad Size)	Via Location (diameter)	Thermal Cycle Rang (total time)	Weibull Scale (No)	Weibull Shape (m)	Acceleratrion Ratio
175 I/O FPBGA* Single-Side Condition 1 Condition 2	1.57 +/- 0.2 (300 μm) (400 μm)	On Pad (125 μm)	0°C to 100°C (32 min)	4331 3525	11.1 9.1	N/A
175 I/O FPBGA* Double-Side Condition 1 Condition 2	(300 μm) (400 μm)			1616 1163	17.6 10.5	N/A
TV-2 175 I/O FPBGA 9 data points 8 data points	1.27 (300 μm)	On Pad (100 μm)	-55°C to 125° (68 min)	1126 1134	6 11.9	3.8

Acknowledgments

The portion of research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

We express our special thanks to Faisal Masood and Ken Evans at JPL and Mark Chisa at Boeing for monitoring the environmental testing. The authors would like to acknowledge the in-kind contributions and cooperative efforts of the JPL CSP Consortium team members especially Steve Stegura for design and Chris Achong for assembly. Special thanks are also extended to package suppliers and board manufacturers as well as other and other team members who have made contributions to the progress of this program.

References

- Ghaffarian, R., Kim, N., Rose, D., Hunter, B., Devitt, K., Long, T., "Rapid Qualification of CSP Assemblies By Increase of Ramp Rates and Cycling Temperature Ranges", The Proceedings of Surface Mount International, Chicago, Sept. 30-Oct 4, 2001
- Ghaffarian, R., Nelson, G, Cooper, M., Lam, D., Strudler, S., Umdekar, A., Selk, K., BJORNDahl, B., Duprey, R., "Thermal Cycling Test Results of CSP and RF Package Assemblies", The Proceedings of Surface Mount International, Chicago, Sept. 25-28, 2000
- Fjelstad, J., Ghaffarian, R., Kim, YG., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002)
- Ghaffarian, R., "Chip Scale Package Assembly Reliability", Chapter 23rd in *Area Array Interconnect Handbook* (Kluwer Academic Publishers, edited by Karl Puttlitz, Paul Totta, 2002)
- Ghaffarian, R., "BGA Assembly Reliability", Chapter 20, *Area Array Packaging Handbook* (McGraw-Hill Publisher, Ken Gilleo, Editor)
- IPC 9701,"Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments". Published by IPC, Association Connecting Electronics Industries
- O'Connor, Patrick D. T., "Practical Reliability Engineering, Third Edition, John Wiley & Son, Chichester, Great Britain, 1996
- Newman, K., Freda, M., Ito, H., Yama, N., Nakanishi, E., "Enhancements in 175FPBGA Board-Level Solder Joint Reliability Through Package Constructions" ,The Proceedings of the 6th Pan Pacific Microelectronics Symposium, Kauai, HI, Jan, 2001
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